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THE UC3902 LOAD SHARE CONTROLLER AND ITS PERFORMANCE IN DISTRIBUTED POWER SYSTEMS

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UC3902 APPLICATIONS

The current demanded by large electronic systems continuously rises due to higher performance and increased functionality. At the same time, supply voltages, especially in digital circuits, are falling to previously unprecedented low levels. The combination of higher load currents and low supply voltages impose difficult requirements on the power distribution and in most cases, forces a higher voltage distribution bus with local voltage conversion.

Users of distributed power systems are seeking reliable and economic solutions to supply their loads. A modular approach, where stand alone power supplies are utilized for local power conversion, is widely accepted in these applications. The power rating of the individual converters are usually limited by the available height, board space and by the limitation on volumetric heat dissipation. High current loads are supplied by several parallel connected power supplies. In addition to higher currents, the parallel modules can also offer redundancy, an important factor to achieve reliable, uninterrupted operation and extended life expectancy in these systems.

Parallel connected power supplies require a dedicated control mechanism, called load share circuitry to assure full utilization of the system. The purpose of a load share controller, like Unitrode's UC3902, is to provide for equal distribution of the load current among the parallel connected power supplies. By equalizing the output currents, uniform thermal stress of the individual modules is also ensured which has the utmost importance for long term reliability of electronic components.

For the UC3902 to work properly, the modular power system has to consist of power supplies which possess their own feedback circuits. Furthermore, the stand alone modules have to be equipped with true remote sense capability or with an output voltage adjustment terminal. Each module must have its own load share controller. The operating principle of a load share mechanism is to measure the output current of each individual module and to be able to modify the output voltage of the units until all participating power supplies deliver equal output currents. It is accomplished by the UC3902 integrated circuits which are connected to the common load share bus and adjust the positive sense voltage (or the voltage of the output voltage adjust pin) of their respective modules to provide equal load current sharing.

UC3902 BLOCK DIAGRAM

The UC3902 is an 8-pin integrated circuit. Its sole purpose is to provide the load sharing function for existing power supplies. The chip incorporates only the building blocks required for load sharing. Tight regulation of the converters' output voltage is not anticipated with this circuit. In fact, the UC3902 performs just the opposite task by finely adjusting the regulated output voltage of the converters to match all output currents evenly.
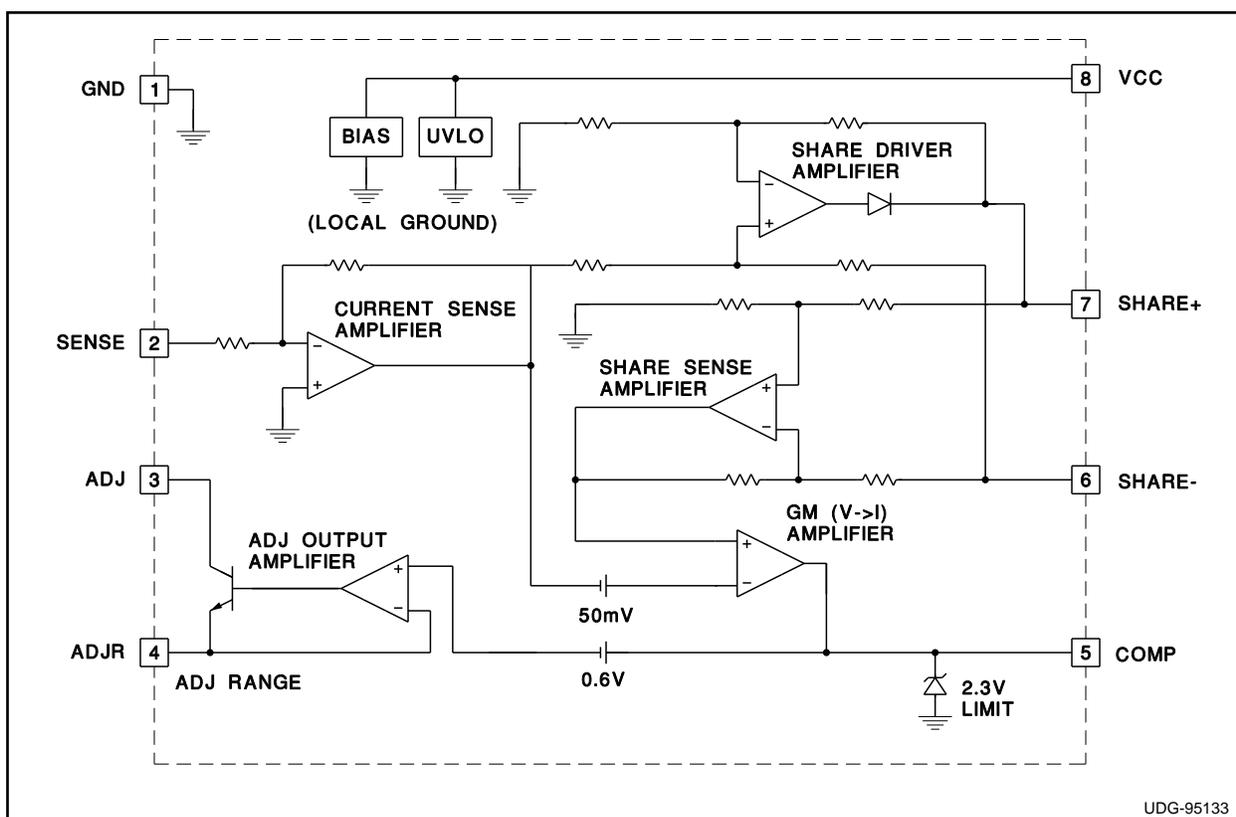
Figure 1. UC3902 Block Diagram

A unique advantage of the UC3902 is its differential load share bus. This architecture greatly enhances the noise immunity of the system. Figure 1 shows the block diagram of the load share controller.

The IC consists of a current sense amplifier, a share bus driver and sense amplifier pair, an error amplifier, a buffer stage called adjust amplifier, and housekeeping circuit which provides internal bias and the on-chip reference for the circuit.

The UC3902 has an inverting current sense amplifier with the gain of 40. The output of the current sense amplifier is proportional to the output current of the power supply it is connected to. It provides the input signals to the load share bus driver amplifier and to the inverting input of the error amplifier. Because the share driver amplifier is configured for unity gain, the voltage on the output of the share driver amplifier also equals the output voltage of the current sense amplifier. When this voltage is the highest potential among the parallel connected load share controllers, i.e. the unit delivers the highest output current, the module acts as the master unit. The output of the share driver amplifier of the master also determines the voltage on the share bus. In the case, where this voltage is lower then the share bus voltage, i.e. the module supplies less current than any one of the other units in the system, the share controller will behave as a slave. The output of the share driver amplifier of the slave controllers

is disconnected from the share bus by the diodes in series with their respective outputs.

The share sense amplifier measures the voltage on the differential share bus and provides the signal for the noninverting input of the error amplifier. Similar to the share driver amplifier, this circuit has a gain of 1 which is fixed internally. Consequently, the output voltage of the share sense amplifier always corresponds to the highest output current level, delivered by the master unit in the system.

A transconductance amplifier is utilized for the error amplifier function in the UC3902. If a feedback network were connected between the output and the inverting input of the error amplifier, the output current representation would be inaccurate. The transconductance amplifier allows the feedback network to be connected from the amplifier output to the ground which preserves the authenticity of the current signal at the inverting input of the error amplifier. Also note that this type of amplifier requires a voltage difference between its inverting and noninverting inputs. Furthermore, the transconductance amplifier has high input and output impedances. Instead of the usual low impedance voltage source output of operational amplifiers, this circuit has a high impedance current source output. Accordingly, the gain is defined as transconductance (A/V) but it can be converted back to the general V/V gain term by

multiplying the transconductance of the amplifier (Gm) with the impedance of the compensation network (X_{COMP}).

The steady state output voltage of the error amplifier is the function of the voltage difference between the outputs of the current sense and the share sense amplifiers. When a particular controller works as the master in the system this voltage difference is zero. To guarantee the correct state of the error amplifier, a 50mV offset is inserted in series with the inverting input. This artificial offset will ensure zero volts at the output of the error amplifier when the unit is the master module. All slave controllers will develop a non zero error voltage at the output of the transconductance amplifier which is proportional to the difference between the output current of the respective power supply and the output current value of the master module represented on the share bus.

The output voltage of the error amplifier is used to adjust the output voltage of the power converter to balance the load current among the parallel connected modules. This is done by the adjust amplifier and its companion NPN transistor. The adjust amplifier provides signal conditioning for the error signal and its output drives a NPN transistor which is configured as a programmable current source. A resistor from its emitter to ground and the error voltage defines the current, I_{ADJ}, which flows through a resistor connected between the ADJ pin of the load-share controller and the positive output terminal. The I_{ADJ} current causes a voltage drop across the resistor which requires the power supply

to increase its output voltage. The resulting higher power supply output voltage increases the output current of that particular module until the output current levels equal out among the units. At that point load sharing has been established.

UC3902 LOAD SHARE CONTROLLER DESIGN

The UC3902 load share controller requires only a few external components. Before the values of these components can be calculated, the DC/DC converter module parameters must be reviewed and some application specific limits have to be determined. There are three parameters which must be known; $V_{O,NOM}$ is the nominal output voltage of the converter, $I_{O,MAX}$ is the maximum current delivered by the unit and $\Delta V_{O,MAX}$ is the maximum adjustment range of the output voltage. The output voltage adjustment can be accomplished by using either the positive sense terminal or the adjust pin of the DC/DC converters and it is usually limited by the design of the modules. Depending on the output current level, the allocated voltage drop and the allowed power dissipation, the current sense resistor can be selected. Since the UC3902 is operational from 2.7V to 20V, in most cases the IC is powered directly from the output voltage of the system. If that is not possible because of an inappropriate value of the output voltage, the supply voltage, V_{CC}, has to be determined as well.

SETTING UP THE DC OPERATING POINT

Figure 2 shows a typical application of the UC3902 load share controller. This circuit must be repeated
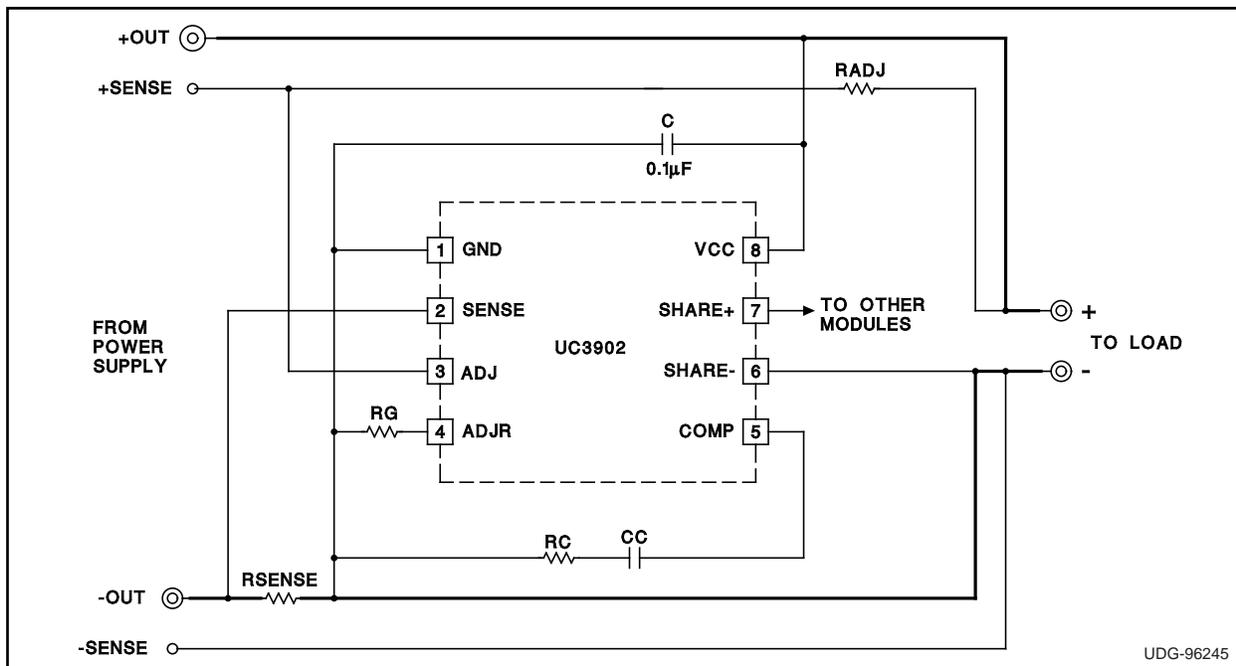

Figure 2. Typical Application

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for each power supply sharing the current for a common load in the system. The design process starts with calculating the component values for setting up the basic operating conditions for the IC.

In order to precisely share the load current among parallel connected modules, the output current of each individual power supply has to be measured. A current sense resistor, R_{SENSE} is placed in the negative return path of the units. Choosing R_{SENSE} is based on two factors; the maximum power dissipation and the maximum voltage drop across the sense resistor. While the power dissipation is only limited by practical considerations like efficiency and component ratings, the maximum voltage drop has to comply with internal signal level limits of the integrated circuit. Most important is to prevent the output of the current sense amplifier from saturation. The highest voltage of the amplifier output, V_{CSAO} is a function of V_{CC}. It equals either 10V or V_{CC} - 1.5V, whichever is lower. Consequently,

$$V_{SENSE, MAX} = \frac{V_{CSAO}}{A_{CSA}}$$

where $V_{SENSE,MAX}$ is the maximum voltage drop across the current sense resistor, V_{CSAO} is the maximum voltage of the current sense amplifier output and A_{CSA} is 40, the gain of the current sense amplifier.

Once $V_{SENSE,MAX}$ is determined, the current sense resistor value can be calculated by the following formula:

$$R_{SENSE} = \frac{V_{SENSE,MAX}}{I_{O,MAX}}$$

$I_{ADJ,MAX}$, the maximum current of the adjust amplifier is 10mA as specified in the datasheet. It is a good practice to keep the highest current of the adjust amplifier in the 5mA to 10mA range as lower values might increase the noise sensitivity of the system. This current is determined by the highest possible voltage on the ADJR pin which is 2.6V and by the resistor, R_G, between the ADJR pin and ground. Thus the resistor value can be calculated as:

$$R_G = \frac{2.6V}{I_{ADJ,MAX}}$$

R_{ADJ} is the impedance inserted in the positive sense line of the power supply. Its value is the function of the maximum adjustment range of the output voltage, $\Delta V_{O,MAX}$ and the previously selected $I_{ADJ,MAX}$ current value. Since the voltage drop across the current sense resistor reduces the range available for output voltage adjustment, that factor has to be accounted for as shown in the equation for R_{ADJ} below:

$$R_{ADJ} = \frac{\Delta V_{O,MAX} - I_{O,MAX} \bullet R_{SENSE}}{I_{ADJ,MAX}}$$

This relationship points out an important design constraint for the system. The sum of the voltage drops across the wiring impedances and the voltage drop across the current sense resistor must be significantly lower than $\Delta V_{O,MAX}$ or the load share mechanism has no headroom to adjust the output voltage of the modules to achieve proper distribution of the load current.

CLOSING THE SHARE LOOP

Balanced distribution of the load currents among the parallel connected units is accomplished by an additional control loop provided only for the load share function. Similarly to other control loops inside the power supplies, the current share loop is based on negative feedback. Such control loops must obey certain stability criteria in order to work properly. Although this Application Note does not cover the theoretical background of loop stability, some of the most critical conditions for successfully closing the load share loop will be pointed out.

Since the load share loop is added to existing power supplies, interaction between the existing voltage control loop and the share loop must be avoided. For that reason the crossover frequencies of the two loops must be well separated.

The voltage loop crossover frequency, $f_{0,V}$ is greatly dictated by the required transient response of the converter. In order to maintain the stability of the voltage control loop, the share loop has to be set up not to cause any excess phase shift at $f_{0,V}$. This is usually achieved by placing the crossover frequency of the share loop ($f_{0,S}$) at least one, but preferably two decades lower than the crossover frequency of the voltage loop. Also a zero should be placed in the transfer function at $f_{0,S}$. This way, the effect of the share loop is minimized at the crossover frequency of the voltage loop.

Closing the load share loop at low crossover frequency is acceptable, if the purpose of load sharing is clarified. The primary concern for load sharing is to extend the life expectancy of the system and to increase reliability. It is achieved in the system by paralleling several modules and

assuring that their thermal stresses are balanced during the life of the product. Another advantage in such systems is the possibility for redundancy. These goals can be completely fulfilled by slow acting corrective measures which allow $f_{0,S}$ to be significantly lower than $f_{0,V}$.

The first step is to determine the transfer functions of the individual building blocks for the frequency range from 0.1Hz to approximately 1kHz. The unity gain crossover frequency of the load share control loop is expected to be within these frequency limits. If off-the-shelf power supplies are being used, then a network analyzer should be used to measure the transfer function. This is also a good practice to confirm actual versus calculated performance as well.

The valid transfer functions for the range of our interest are:

- $A_{PWR}(s)$: the transfer function of the power supply, measured by injecting an AC signal between V_{SENSE+} and V_{OUT+} terminals.

- $A_{Vo \to Vis}$: this gain term describes the relationship between the output voltage and the voltage across the current sense resistor. It varies with the load impedance according to

$$A_{Vo \to Vis} = \frac{R_{SENSE}}{R_{LOAD}}$$

- A_{CSA}: the gain of the current sense amplifier. This term is a constant and equals 40.

- A_{SHA}: both amplifiers driving and sensing the signal on the differential share bus are configured for unity gain. ($A_{SHA} = 1$)

- $A_{EA}(s)$: the gain of the error amplifier defined as: $A_{EA}(s) = Gm \cdot X_{COMP}(s)$ where Gm is the transconductance of the error amplifier and $X_{COMP}(s)$ is the impedance of the compensation components as a function of complex frequency.

- A_{ADJ}: the adjust circuit gain depends only on the R_G and R_{ADJ} resistors because the adjust amplifier is configured as a unity gain buffer stage. Consequently,

$$A_{ADJ} = \frac{R_{ADJ}}{R_G}$$

The overall share loop characteristic is established by multiplying the gain terms of the individual blocks:

$$A_{SHARE-LOOP}(s) = A_{PWR}(s) \cdot A_{VO \to VIS} \cdot$$
$$\cdot A_{CS} \cdot A_{SHA} \cdot A_{EA}(s) \cdot A_{ADJ}$$

DESIGN EXAMPLE

Users experimenting with the UC3902 load share controller can utilize a demonstration board featured in Figure 3. This circuit provides a solution for paralleling three power supply modules. The performance of the system was measured using three off-the-shelf DC/DC converter modules, each rated for 100W delivering 8.4A to the load at 12V nominal output voltage.

The design process starts by measuring the transfer function of the power supplies between their positive voltage sense and power output terminals. The resulting Bode plot shown in Figure 4 reveals a 40Hz crossover frequency which will require a crossover frequency of 4Hz for the load share loop. The power stage has 10dB gain at this frequency.

In the demonstration board, the UC3902 is powered from the output voltage of the system. Note the 0.1µF local bypass capacitor connected to the VCC pin of the IC. Using 12V as VCC, the maximum output voltage of the internal amplifiers are approximately 10V. This voltage denotes the highest possible full scale voltage between SHARE+ and SHARE-, but the actual voltage on the load share bus at full load is determined by the designer. Noise sensitivity, accuracy and the number of units in parallel have to be taken into consideration when choosing the full scale bus voltage. The load share bus is driven by the master controller only and each slave module represents a 10kΩ load on the bus. This means that every unit will increase the supply current of the master module by 100µA/V on the load share bus.

The power supply's 8.4A output current rating allows the use of a higher shunt resistor value in favor of better load share accuracy with only a slight decrease in overall efficiency. The full scale bus voltage, V_{CSAO} is selected to be 6V. Accordingly,

$$R_{SENSE} = \frac{6V}{8.4A \cdot 40} = 0.0178\Omega$$

and a 20mΩ standard value had been selected.
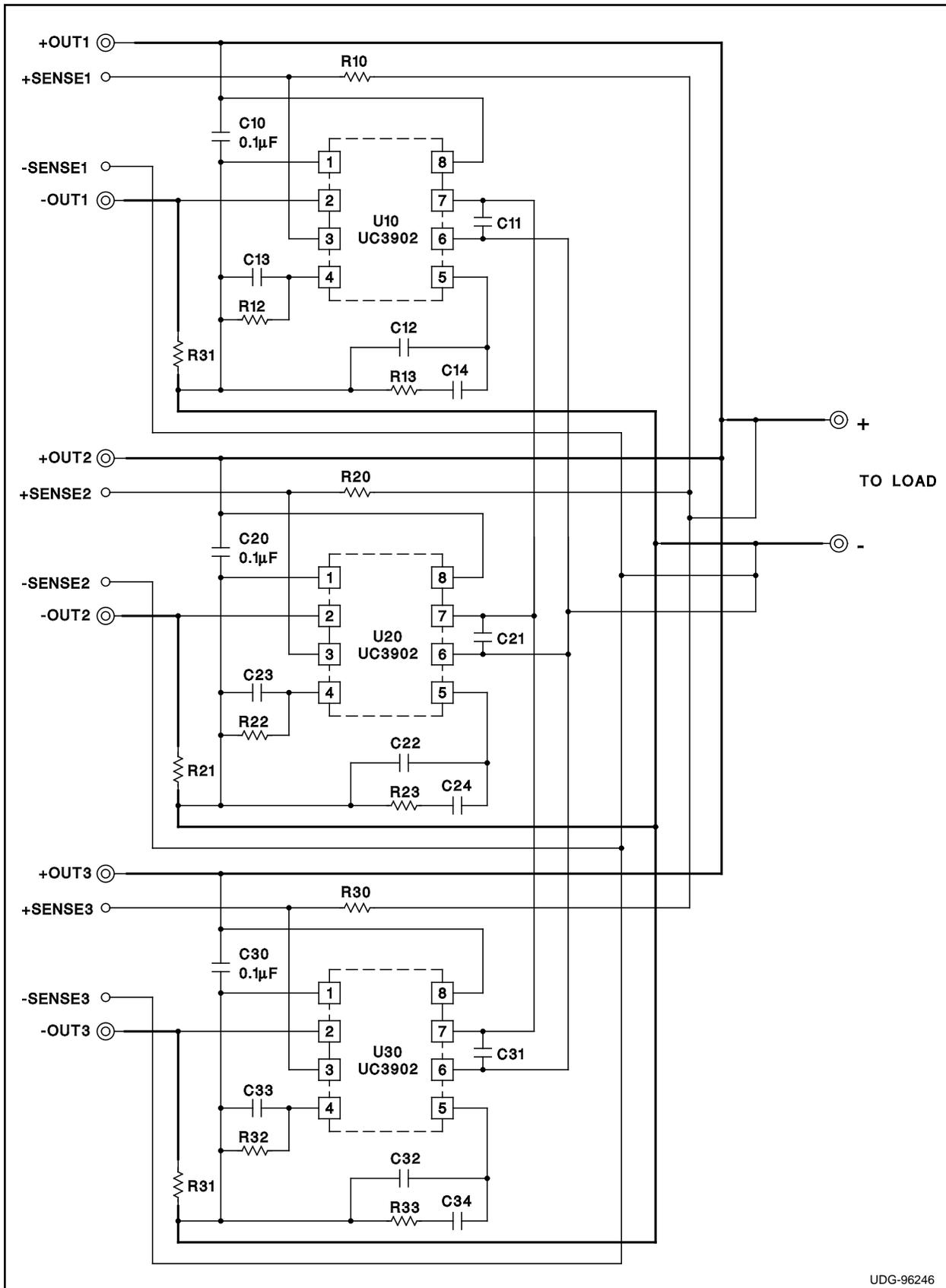
Figure 3. Demonstration Board Schematic

The R_G resistor value depends on the current flowing through the NPN buffer transistor of the adjust amplifier and in the R_{ADJ} resistor placed in the positive sense line of the converter. This current is selected by the designer but its value shall be smaller than 10mA according to the datasheet. For this application 5mA is chosen. Smaller values tend to increase the noise sensitivity of the solution while larger current values represent unnecessary power dissipation for the IC. Although this current does not show up in the I_{CC} current requirements, the power dissipation of the buffer transistor can be a significant part of the total power loss inside the integrated circuit. For instance, in this application, the voltage across the collector emitter terminals equals V_{CC} - 2.6V, approximately 10V. The power dissipated in this part of the circuit is 10V • 5mA= = 50mW. Once the maximum current for this part of the circuit is selected the value of R_G can be calculated as:

$$RG = \frac{2.6V}{5mA} = 520\Omega$$

The nearest standard value of 510Ω is used.

The R_{ADJ} resistor value is defined by the maximum adjustment range of the output voltage, the highest load current, the current sense resistor value and I_{ADJ} value. In this application, $\Delta V_{O,MAX}$ is 0.6V while the other parameters have been previously calculated. Thus,

$$R_{ADJ} = \frac{0.6V - 8.4A \cdot 20m\Omega}{5mA} = 86.4\Omega$$

Instead, an 82Ω standard value is chosen.

At this point, the steady state operating conditions of the system are defined. The compensation components C_C and R_C can be calculated from the loop gain equation.

$$A_{SHARE-LOOP}(s) = A_{PWR}(s) \cdot \frac{R_{SENSE}}{R_{LOAD}} \cdot$$

$$A_{CSA} \cdot Gm \cdot \left(\frac{1}{C_C \cdot s} + R_C\right) \cdot \frac{R_{ADJ}}{R_G}$$

Substituting the power stage gain of 10 at the load share loop crossover frequency and solving the equation for C_C, the compensation capacitor value can be calculated as:

$$C_C = A_{PWR}(s) \cdot \frac{R_{SENSE}}{R_{LOAD}} \cdot A_{CSA} \cdot$$

$$Gm \cdot \frac{1}{\pi \cdot f_{O,S}} \cdot \frac{R_{ADJ}}{R_G}$$

which gives

$$C_C = 10 \cdot \frac{20m\Omega}{1.43\Omega} \cdot 40 \cdot 4.5mS \cdot$$

$$\frac{1}{\pi \cdot 4Hz} \cdot \frac{82\Omega}{510\Omega} = 322\mu F$$

A 330μF capacitor is used. Note that the reason for the large capacitor value is the extremely low crossover frequency dictated by the transfer function characteristic of the DC/DC converter.

The value of R_C is determined by the selected crossover frequency and compensation capacitor value according to:

$$R_C = \frac{1}{2 \cdot \pi \cdot f_{O,S} \cdot C_C}$$

Using the previously calculated capacitor value results in a R_C value of 270Ω.

The resulting Bode plot of the load share control loop is displayed in Figure 4. The phase margin of the loop can be increased by separating the two crossover frequencies, $f_{0,V}$ and $f_{0,S}$ even further. In this particular design, moving $f_{0,S}$ to a lower frequency would have resulted in a very large capacitor value, thus this idea was not considered.
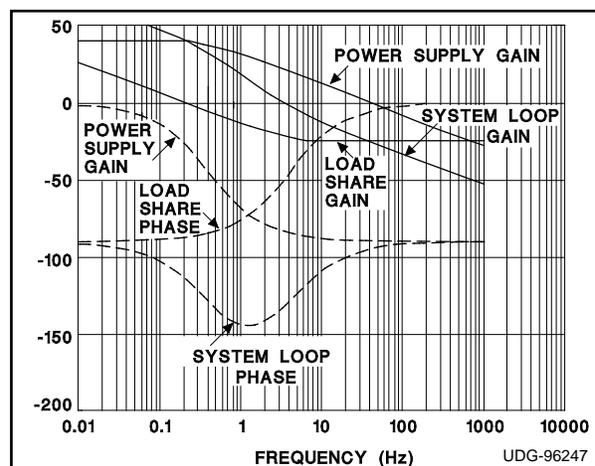

Figure 4. DC/DC Converter and Load Share Loop Bode Plots

PARTS LIST:

C = C10 = C20 = C30 = 0.1μF
    C11 = C21 = C31 = 0.01μF
    C12 = C22 = C32 = not used
    C13 = C23 = C33 = not used
C_C = C14 = C24 = C34 = 330μF
R_{ADJ} = R10 = R20 = R30 = 82Ω
R_{SENSE} = R11 = R21 = R31 = 0.02Ω
R_G = R12 = R22 = R32 = 510Ω
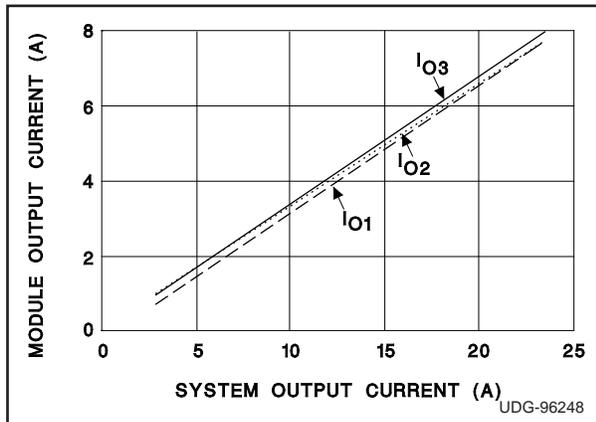R_C = R13 = R23 = R33 = 270Ω

Figure 5. Module vs. Total Output Current

EXPERIMENTAL RESULTS

The performance of the demonstration circuit was measured using the calculated component values and running three DC/DC converters in parallel. Figure 5 shows the output currents of the individual modules as a function of the total load current.

In Figure 6, the percentage of deviation from the calculated average module current is depicted. The
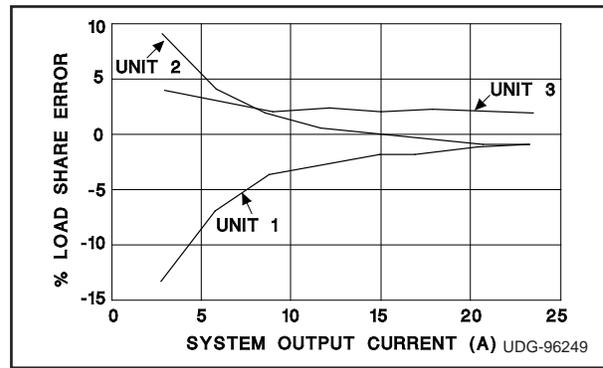

Figure 6. Load Share Accuracy

current distribution error is the largest at light load, as expected, because of the effects of internal offset voltages and the small current measurement signal level. At full load, where load sharing has the most impact, the three modules shared the load current evenly, within 1% of the ideal load current values.

Results similar to this can be obtained in other applications with the formulas contained within this Application Note.

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