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Jameco Part Number 1419680

## Rail-to-rail high output current dual operational amplifier

- Rail-to-rail input and output
- Low noise:  $9\text{nV}/\sqrt{\text{Hz}}$
- Low distortion
- High output current: 80mA (able to drive  $32\Omega$  loads)
- High-speed: 4MHz,  $1\text{V}/\mu\text{s}$
- Operating from 2.7V to 12V
- Low input offset voltage:  $900\mu\text{V}$  max (TS922A)
- ESD Internal protection: 2kV
- Latch-up immunity
- Macromodel included in this specification
- Dual version available in flip-chip package

### Description

The TS922 is a rail-to-rail dual BiCMOS operational amplifier optimized and fully specified for 3V and 5V operation.

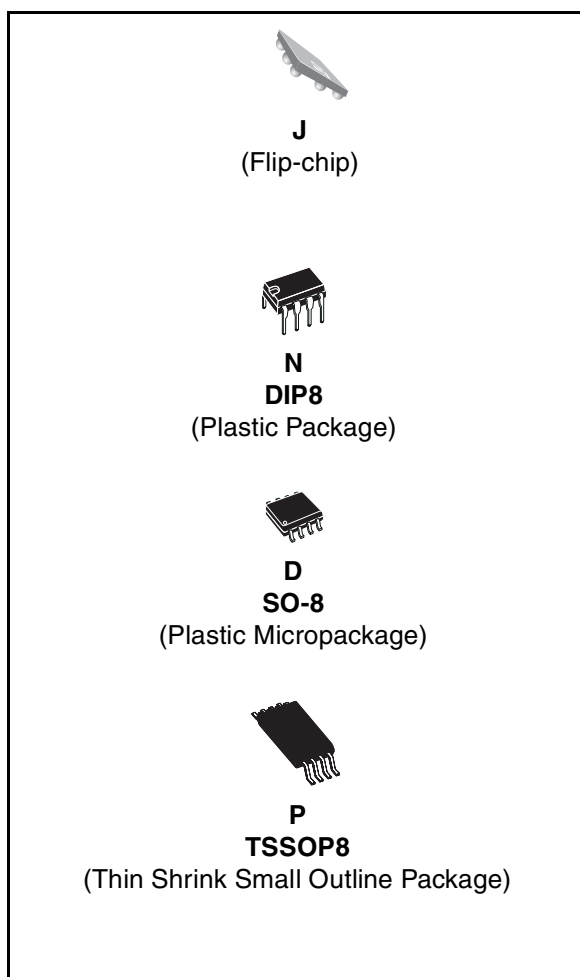
The device's high output current allows low-load impedances to be driven.

Very low noise, low distortion, low offset and a high output current capability make this device an excellent choice for high quality, low voltage or battery operated audio systems.

The device is stable for capacitive loads up to 500pF.

### Applications

- Headphone amplifier
- Sound cards, multimedia systems
- Line driver, actuator driver
- Servo amplifier
- Mobile phone and portable equipment
- Instrumentation with low noise as key factor
- Piezoelectric speaker driver



# 1 Order codes

Part Number	Temperature Range	Package	Packaging	Marking
TS922IN	-40°C, +125°C	DIP8	Tube	TS922IN
TS922AIN				TS922AIN
TS922ID/IDT		SO-8	Tube or Tape & Reel	922I
TS922AID/AIDT				922AI
TS922IPT		TSSOP8 (Thin shrink outline package)	Tape & Reel	922I
TS922AIPT				922AI
TS922IJT/EIJT		Flip-Chip	Tape & Reel	922
TS922IYD/IYDT		SO-8 (automotive grade level)	Tube or Tape & Reel	922IY
TS922AIYD/AIYDT				922AIY
TS922IYPT		TSSOP8 (automotive grade level)	Tape & Reel	922IY
TS922AIYPT				922AY

## 2 Pin diagrams

Figure 1. Pin connections (top view)

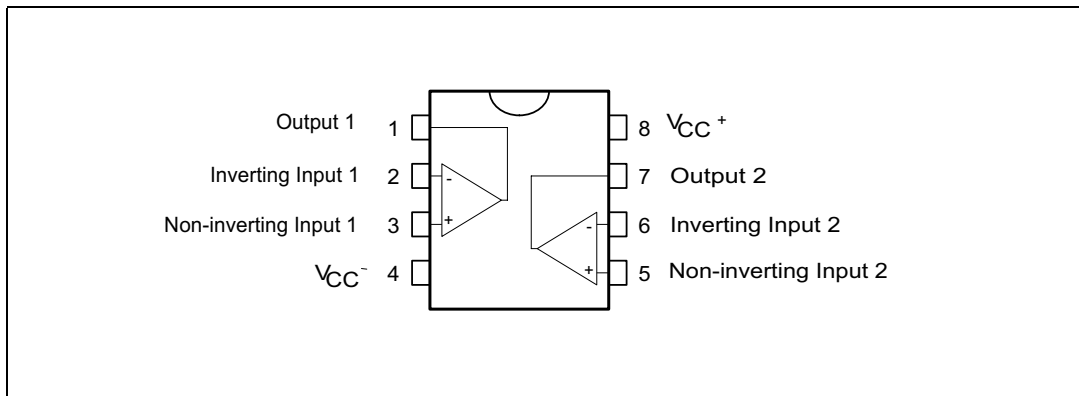
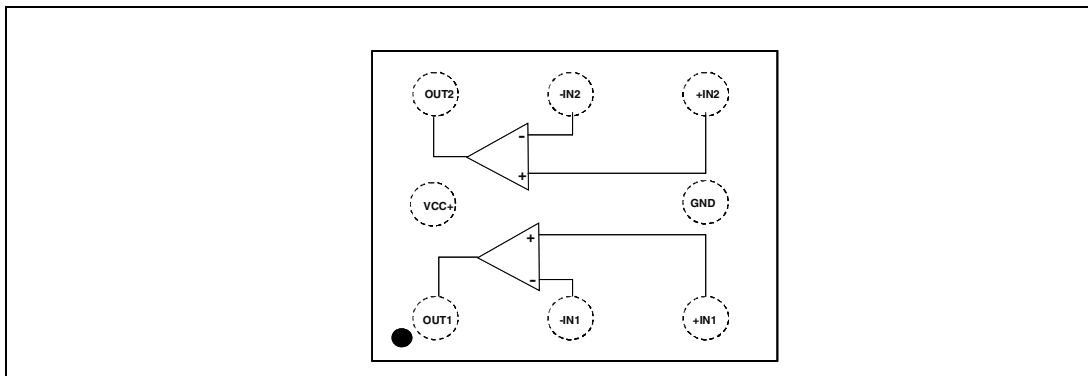


Figure 2. Pin-out for flip-chip package (top view)



### 3 Absolute maximum ratings & operating conditions

**Table 1. Absolute maximum ratings (AMR)**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage <sup>(1)</sup>	14	V
V <sub>id</sub>	Differential Input Voltage <sup>(2)</sup>	±1	V
V <sub>in</sub>	Input Voltage <sup>(3)</sup>	V <sub>DD</sub> -0.3 to V <sub>CC</sub> +0.3	V
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
R <sub>thja</sub>	Thermal Resistance Junction to Ambient SO8	125	°C/W
	TSSOP8	120	
	DIP8	85	
	Flip Chip	90	
T <sub>j</sub>	Maximum Junction Temperature	150	°C
ESD	HBM: Human Body Model <sup>(4)</sup>	2	kV
	MM: Machine Model <sup>(5)</sup>	100	V
	CDM: Charged Device Model	1.5	kV
	Output Short Circuit Duration	see note <sup>(6)</sup>	
	Latch-up Immunity	200	mA
	Soldering Temperature (10sec), leaded version	250	°C
	Soldering Temperature (10sec), unleaded version	260	°C

1. All voltages values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. If Vid > ±1V, the maximum input current must not exceed ±1mA. In this case (Vid > ±1V) an input serie resistor must be added to limit input current.
3. Do not exceed 14V.
4. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
5. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.
6. There is no short-circuit protection inside the device: short-circuits from the output to V<sub>CC</sub> can cause excessive heating. The maximum output current is approximately 80mA, independent of the magnitude of V<sub>CC</sub>. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

**Table 2. Operating conditions**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage	2.7 to 12	V
V <sub>icm</sub>	Common Mode Input Voltage Range	V <sub>DD</sub> -0.2 to V <sub>CC</sub> +0.2	V
T <sub>oper</sub>	Operating Free Air Temperature Range	-40 to +125	°C

## 4 Electrical characteristics

**Table 3.**  $V_{CC} = +3V$ ,  $V_{DD} = 0V$ ,  $V_{icm} = V_{CC}/2$ ,  $T_{amb} = 25^{\circ}C$ ,  $R_L$  connected to  $V_{CC}/2$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage TS922 Input Offset voltage TS922A Input Offset Voltage TS922IJ (Flip Chip) $T_{min.} \leq T_{amb} \leq T_{max.}$ TS922 $T_{min.} \leq T_{amb} \leq T_{max.}$ TS922A $T_{min.} \leq T_{amb} \leq T_{max.}$ TS922IJ (Flip Chip)			3 0.9 1.5 5 1.8 2.5	mV
$DV_{io}$	Input Offset Voltage Drift		2		$\mu V/^{\circ}C$
$I_{io}$	Input Offset Current - $V_{out} = V_{CC}/2$		1	30	nA
$I_{ib}$	Input Bias Current $V_{out} = V_{CC}/2$		15	100	nA
$V_{OH}$	High Level Output Voltage $R_L = 10k$ $R_L = 600\Omega$ $R_L = 32\Omega$	2.90 2.87	2.63		V
$V_{OL}$	Low Level Output Voltage $R_L = 10k$ $R_L = 600\Omega$ $R_L = 32\Omega$		180	50 100	mV
$A_{vd}$	Large Signal Voltage Gain ( $V_{out} = 2V_{pk-pk}$ ) $R_L = 10k$ $R_L = 600\Omega$ $R_L = 32\Omega$		200 35 16		V/mV
$I_{CC}$	Total Supply Current - no load, $V_{out} = V_{CC}/2$		2	3	mA
GBP	Gain Bandwidth Product - ( $R_L = 600\Omega$ )		4		MHz
CMR	Common Mode Rejection Ratio	60	80		dB
SVR	Supply Voltage Rejection Ratio - $V_{CC} = 2.7$ to $3.3V$	60	85		dB
$I_o$	Output Short Circuit Current	50	80		mA
SR	Slew Rate	0.7	1.3		V/ $\mu s$
$\phi_m$	Phase Margin at Unit Gain - $R_L = 600\Omega$ , $C_L = 100pF$		68		Degrees
$G_m$	Gain Margin - $R_L = 600\Omega$ , $C_L = 100pF$		12		dB
$e_n$	Equivalent Input Noise Voltage - $f = 1kHz$		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion $V_{out} = 2V_{pk-pk}$ , $F = 1kHz$ , $A_v = 1$ , $R_L = 600\Omega$		0.005		%
$C_s$	Channel Separation		120		dB

**Table 4. Electrical characteristics  $V_{CC} = 5V$ ,  $V_{DD} = 0V$ ,  $V_{icm} = V_{cc}/2$ ,  $T_{amb} = 25^{\circ}C$ ,  $R_L$  connected to  $V_{cc}/2$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input Offset Voltage TS922			3	mV
	Input Offset voltage TS922A			0.9	
	Input Offset Voltage TS922IJ (Flip Chip)			1.5	
	$T_{min.} \leq T_{amb} \leq T_{max.}$ TS922			5	
	TS922A			1.8	
	TS922IJ (Flip Chip)			2.5	
$V_{io}$	Input Offset Voltage TS922IJ (flip chip)			1.5	mV
	$T_{min.} \leq T_{amb} \leq T_{max.}$ TS922IJ			2.5	
$DV_{io}$	Input Offset Voltage Drift		2		$\mu V/^{\circ}C$
$I_{io}$	Input Offset Current - $V_{out} = V_{cc}/2$		1	30	nA
$I_{ib}$	Input Bias Current - $V_{out} = V_{cc}/2$		15	100	nA
$V_{OH}$	High Level Output Voltage	4.90 4.85	4.4		V
	$R_L = 10k$				
	$R_L = 600\Omega$				
	$R_L = 32\Omega$				
$V_{OL}$	Low Level Output Voltage		300	50 120	mV
	$R_L = 10k$				
	$R_L = 600\Omega$				
	$R_L = 32\Omega$				
$A_{vd}$	Large Signal Voltage Gain ( $V_{out} = 2V_{pk-pk}$ )		200 35 16		V/mV
	$R_L = 10k$				
	$R_L = 600\Omega$				
	$R_L = 32\Omega$				
$I_{cc}$	Total Supply Current - no load, $V_{out} = V_{cc}/2$		2	3	mA
GBP	Gain Bandwidth Product - ( $R_L = 600\Omega$ )		4		MHz
CMR	Common Mode Rejection Ratio	60	80		dB
SVR	Supply Voltage Rejection Ratio - $V_{cc} = 4.5$ to $5.5V$	60	85		dB
$I_o$	Output Short Circuit Current	50	80		mA
SR	Slew Rate	0.7	1.3		V/ $\mu s$
$\phi_m$	Phase Margin at Unit Gain - $R_L = 600\Omega$ , $C_L = 100pF$		68		Degrees
$G_m$	Gain Margin - $R_L = 600\Omega$ , $C_L = 100pF$		12		dB
$e_n$	Equivalent Input Noise Voltage - $f = 1kHz$		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion $V_{out} = 2V_{pk-pk}$ , $F = 1kHz$ , $A_v = 1$ , $R_L = 600\Omega$		0.005		%
$C_s$	Channel Separation		120		dB

Figure 3. Output short circuit current vs. output voltage

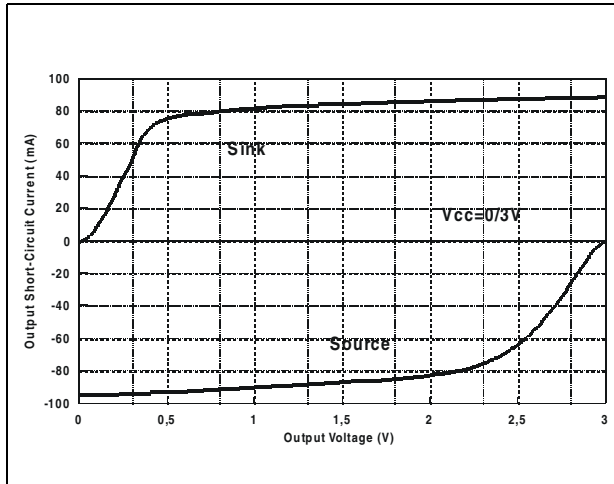


Figure 4. Total supply current vs. supply voltage

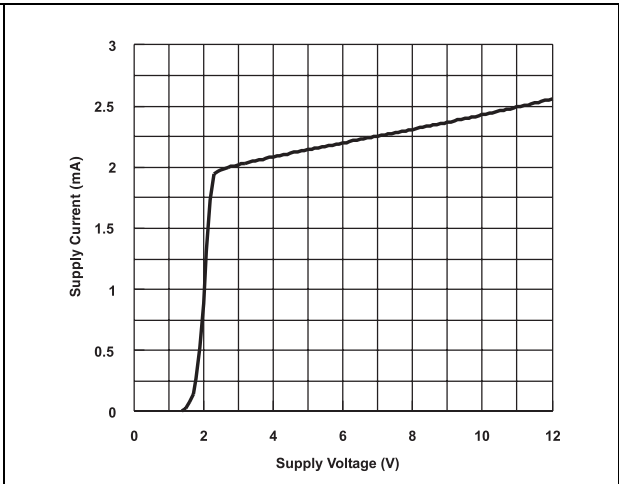


Figure 5. Voltage gain and phase vs. frequency

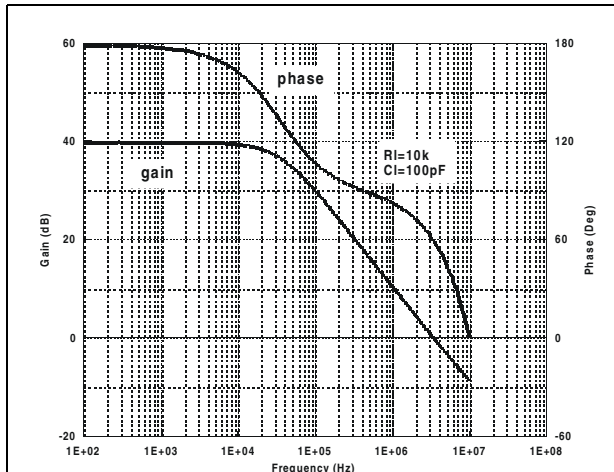


Figure 6. Equivalent input noise voltage vs. frequency

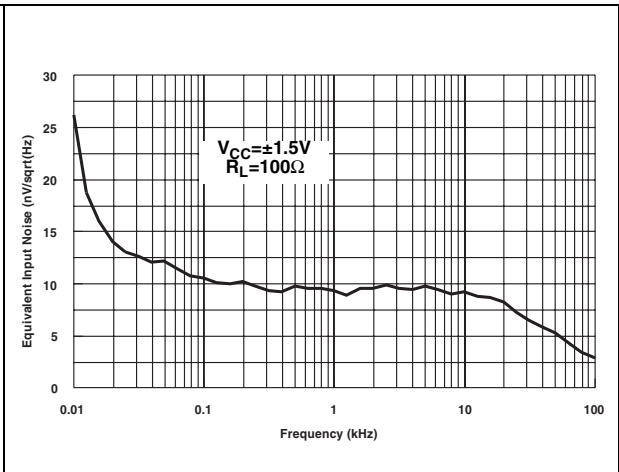


Figure 7. THD + noise vs. frequency

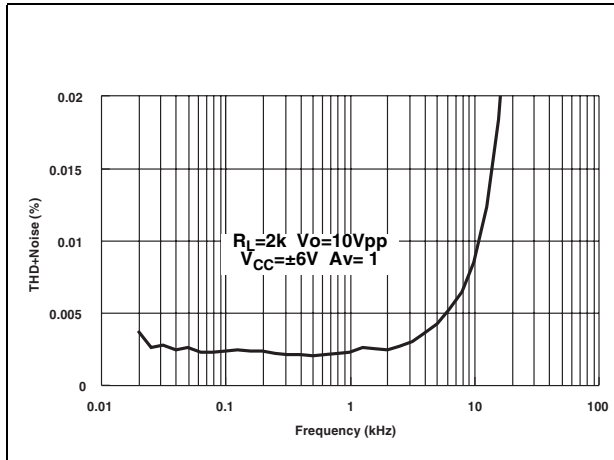


Figure 8. THD + noise vs. frequency

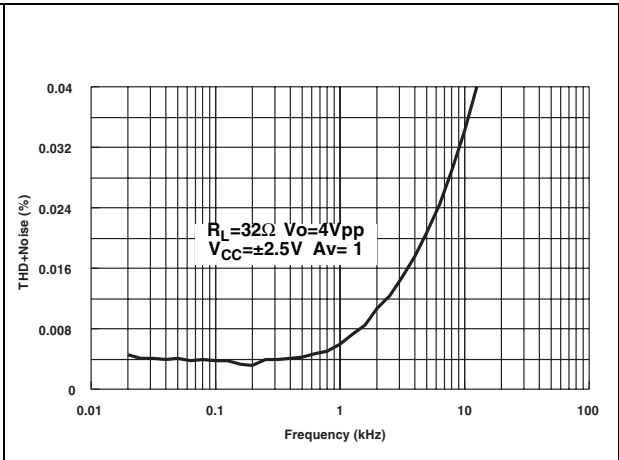




Figure 9. THD + noise vs. frequency

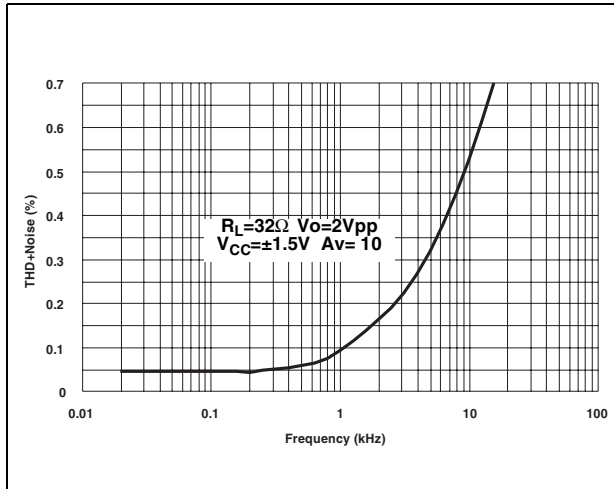


Figure 10. THD + noise vs. output voltage

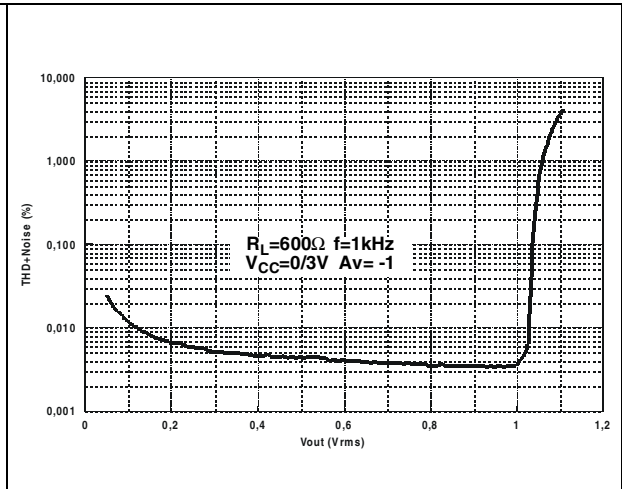


Figure 11. THD + noise vs. output voltage

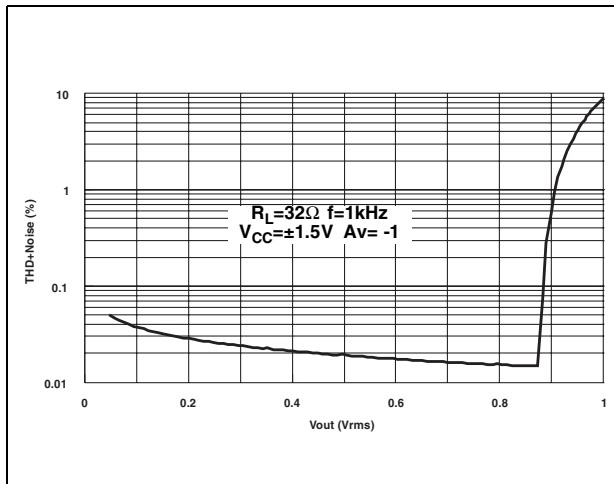


Figure 12. THD + noise vs. output voltage

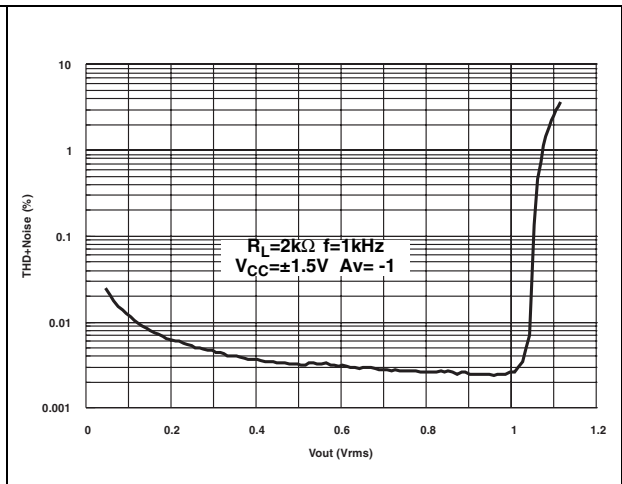
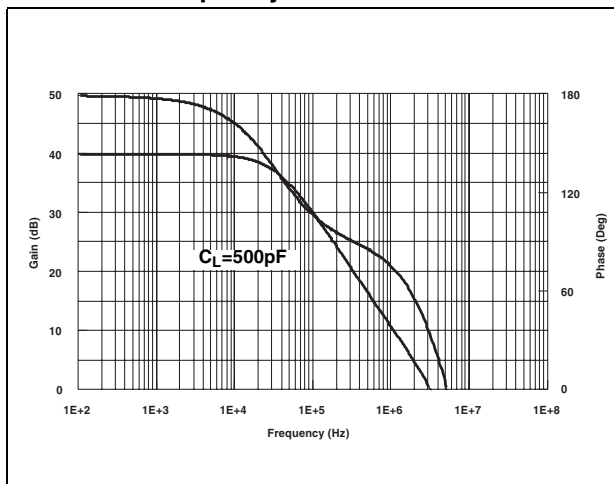


Figure 13. Open loop gain and phase vs. frequency



## 5 Macromodel

### 5.1 Important note concerning this macromodel

Please consider following remarks before using this macromodel.

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.

Data issued from macromodels used outside of its specified conditions ( $V_{CC}$ , Temperature, etc.) or even worse: outside of the device operating conditions ( $V_{CC}$ ,  $V_{icm}$ , etc.) are not reliable in any way.

In [Section 5.2](#), the electrical characteristics resulting from the use of these macromodels are presented.

### 5.2 Electrical characteristics from macromodelization

**Table 5. Electrical characteristics resulting from macromodel simulation at  $V_{CC} = 3V$ ,  $V_{DD} = 0V$ ,  $R_L$ ,  $C_L$  connected to  $V_{CC}/2$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)**

Symbol	Conditions	Value	Unit
$V_{io}$		0	mV
$A_{vd}$	$R_L = 10k\Omega$	200	V/mV
$I_{CC}$	No load, per operator	1.2	mA
$V_{icm}$		-0.2 to 3.2	V
$V_{OH}$	$R_L = 10k\Omega$	2.95	V
$V_{OL}$	$R_L = 10k\Omega$	25	mV
$I_{sink}$	$V_O = 3V$	80	mA
$I_{source}$	$V_O = 0V$	80	mA
GBP	$R_L = 600k\Omega$	4	MHz
SR	$R_L = 10k\Omega$ , $C_L = 100pF$	1.3	V/ $\mu s$
$\phi_m$	$R_L = 600k\Omega$	68	Degrees

### 5.3 Macromodel code

```

** Standard Linear Ics Macromodels, 1996.
** CONNECTIONS:
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
*
.SUBCKT TS92X 1 2 3 4 5
*
.MODEL MDTH D IS=1E-8 KF=2.664234E-16 CJO=10F
*
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 8.125000E+00
RIN 15 16 8.125000E+00
RIS 11 15 2.238465E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 153.5u
VOFN 13 14 DC 0
IPOL 13 5 3.200000E-05
CPS 11 15 1e-9
DINN 17 13 MDTH 400E-12
VIN 17 5 -0.100000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.400000E+00
FCP 4 5 VOFP 1.865000E+02
FCN 5 4 VOFN 1.865000E+02
FIBP 2 5 VOFP 6.250000E-03
FIBN 5 1 VOFN 6.250000E-03
* GM1 STAGE *****
FGM1P 119 5 VOFP 1.1
FGM1N 119 5 VOFN 1.1
RAP 119 4 2.6E+06
RAN 119 5 2.6E+06
* GM2 STAGE *****
G2P 19 5 119 5 1.92E-02
G2N 19 5 119 4 1.92E-02
R2P 19 4 1E+07
R2N 19 5 1E+07
*****
VINT1 500 0 5
GCONVP 500 501 119 4 19.38
VP 501 0 0
GCONVN 500 502 119 5 19.38
VN 502 0 0

```

```
***** orientation isink isource *****
VINT2 503 0 5
FCOPY 503 504 VOUT 1
DCOPYP 504 505 MDTH 400E-9
VCOPYP 505 0 0
DCOPYN 506 504 MDTH 400E-9
VCOPYN 0 506 0
*****
F2PP 19 5 poly(2) VCOPYP VP 0 0 0 0 0.5
F2PN 19 5 poly(2) VCOPYP VN 0 0 0 0 0.5
F2NP 19 5 poly(2) VCOPYN VP 0 0 0 0 1.75
F2NN 19 5 poly(2) VCOPYN VN 0 0 0 0 1.75
* COMPENSATION *****
CC 19 119 25p
* OUTPUT *****
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 6.250000E+02
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 6.250000E+02
VINM 5 27 5.000000E+01
VOUT 3 23 0
ROUT 23 19 6
COUT 3 5 1.300000E-10
DOP 19 25 MDTH 400E-12
VOP 4 25 1.052
DON 24 19 MDTH 400E-12
VON 24 5 1.052
.ENDS;TS92X
```

## 6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

### 6.1 Flip-chip package (8 bumps)

Figure 14. Top view and dimensions of 8-bump flip-chip

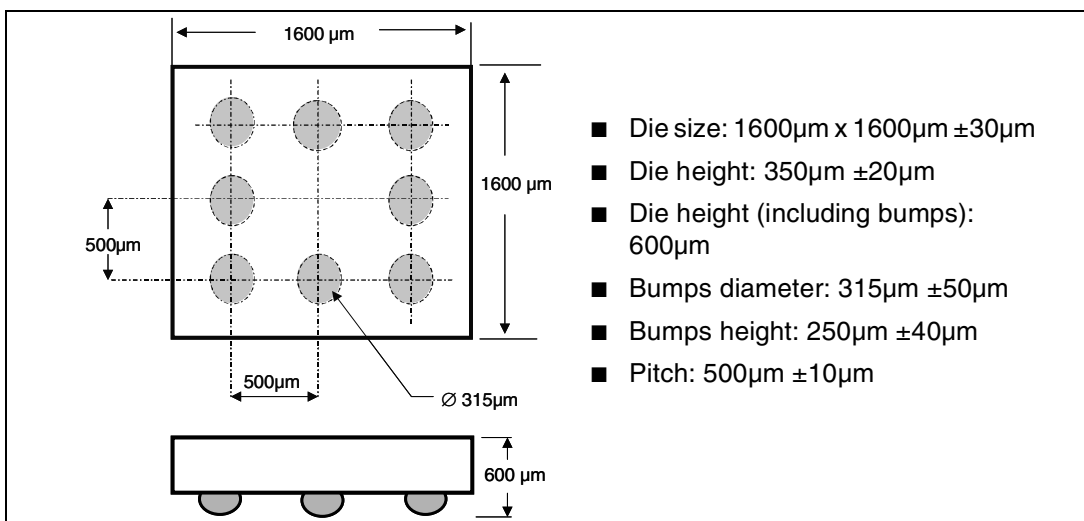


Figure 15. Flip-chip footprint recommendation

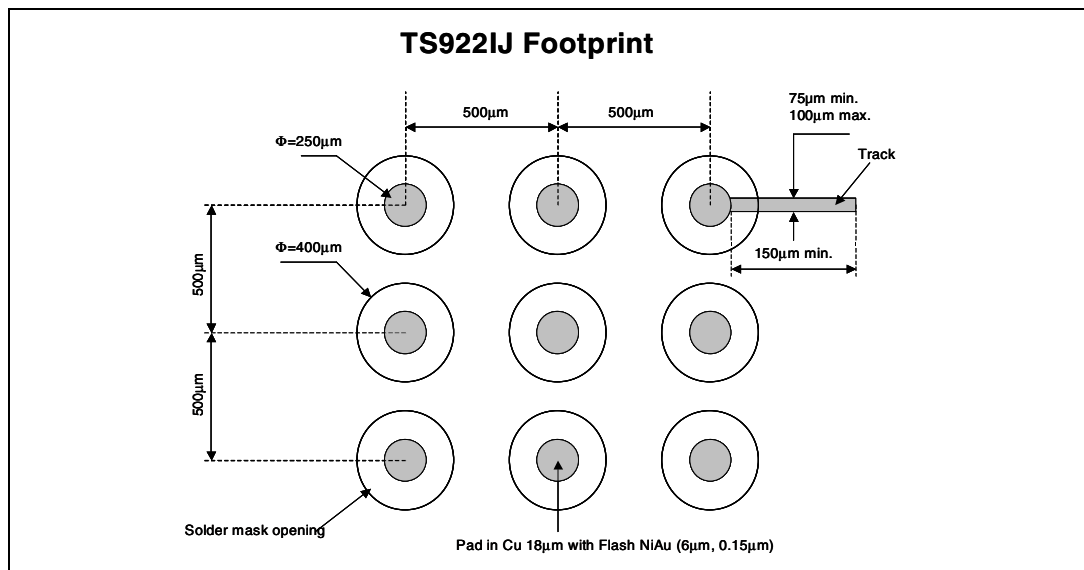
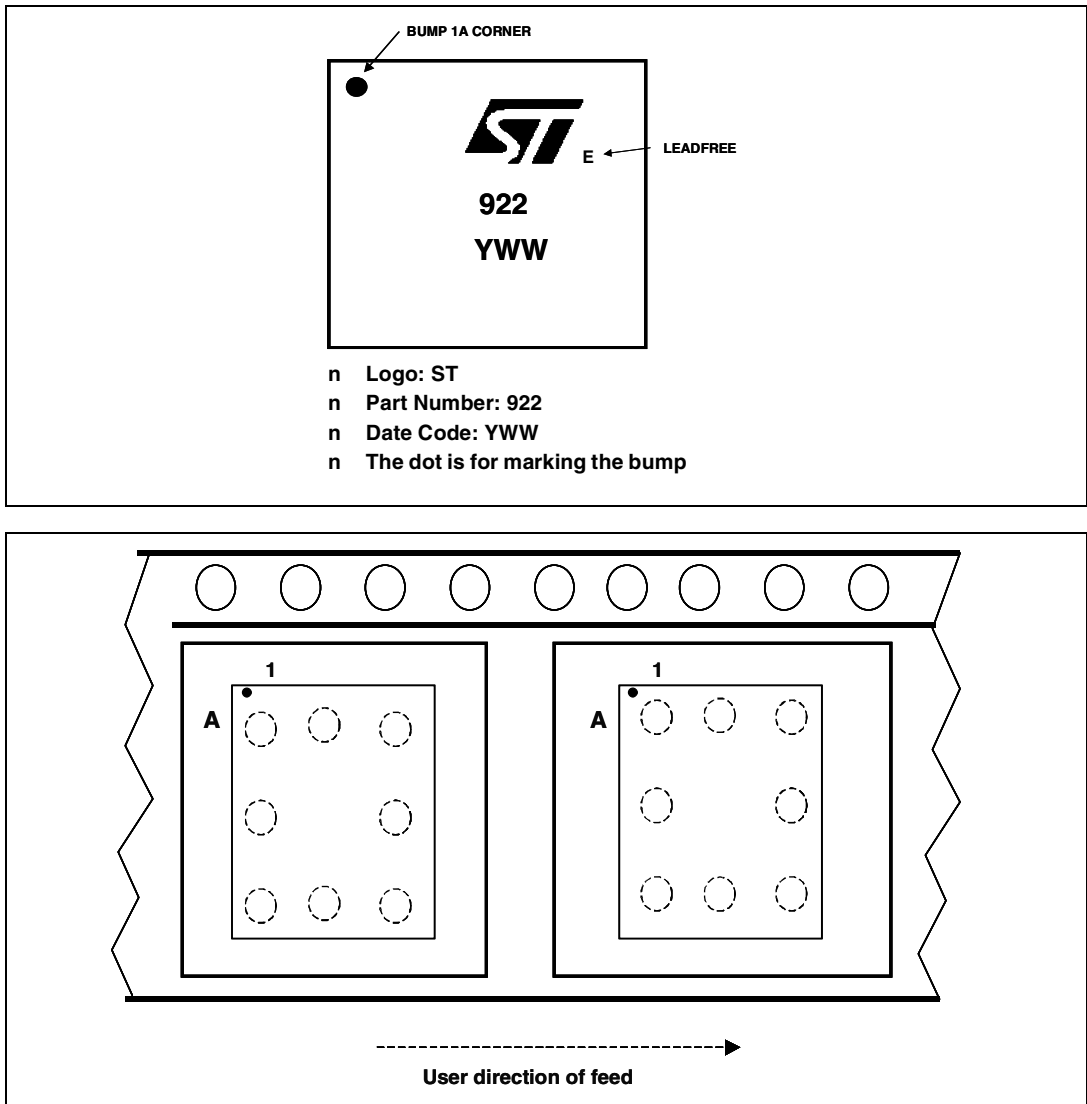


Figure 16. Flip-chip marking (top view)

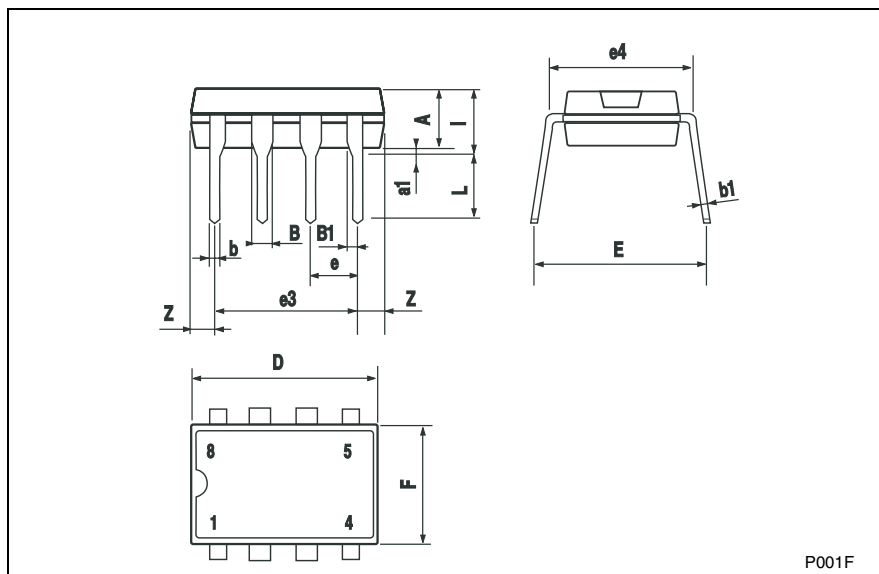


Note: **Device Orientation:** the devices are oriented in the carrier pocket with bump number A1 adjacent to the sprocket holes.

## 6.2 DIP8 package

**Plastic DIP-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
l			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

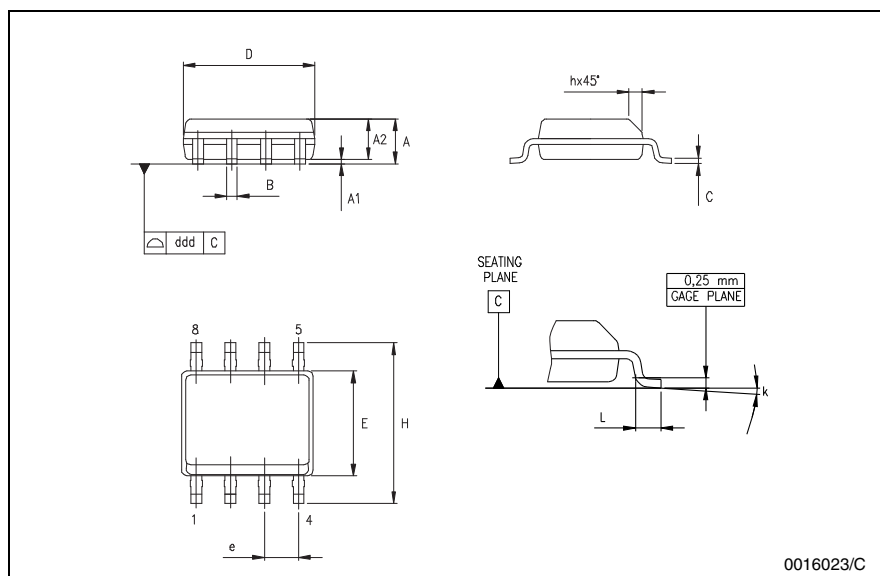


P001F

### 6.3 SO-8 package

**SO-8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



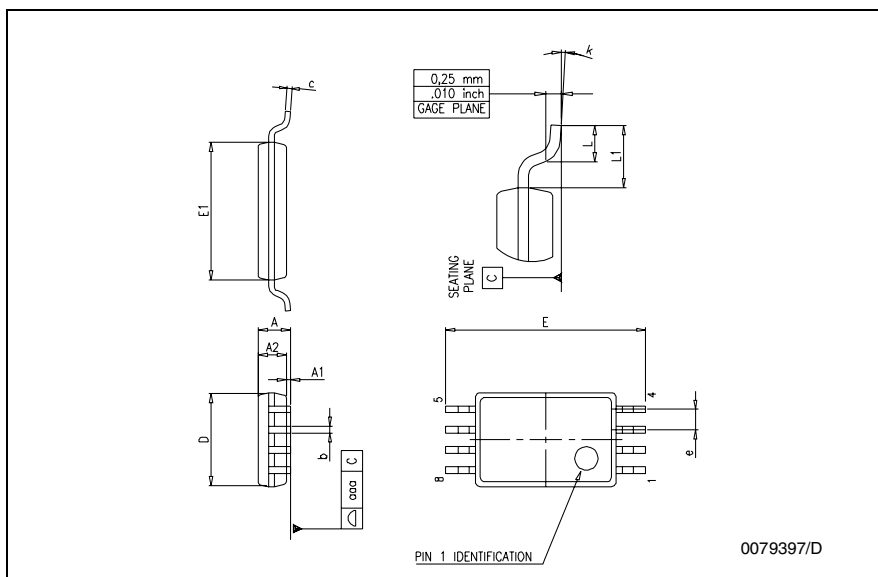
0016023/C



### 6.4 TSSOP8 package

**TSSOP8 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	



## 7 Revision history

**Table 6. Document revision history**

Date	Revision	Changes
Feb.2001	1	First Release.
July 2004	2	Flip-Chip package inserted in the document.
May 2005	3	Modifications on AMR <a href="#">Table 3 on page 4</a> (explanation of Vid and Vi limits, ESD MM and CDM values added, Rthja added).
Aug. 2005	4	PPAP references inserted in the datasheet see <a href="#">Table 1 on page 2</a> .
March 2006	5	TS922EIJT part number inserted in the datasheet see <a href="#">Table 1 on page 2</a> .

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