

LOW-NOISE FAST-TRANSIENT-RESPONSE 1.5-A LDO VOLTAGE REGULATORS

Check for Samples: [TPS7A45xx](#)

FEATURES

- Optimized for Fast Transient Response
- Output Current: 1.5 A
- High Output Voltage Accuracy : 1% at 25°C
- Dropout Voltage: 300 mV
- Low Noise: 35 μV_{RMS} (10 Hz to 100 kHz)
- High Ripple Rejection: 68 dB
- 1-mA Quiescent Current
- No Protection Diodes Needed
- Controlled Quiescent Current in Dropout
- Fixed Output Voltages: 1.5 V, 1.8 V, 2.5 V, 3.3 V
- Adjustable Output from 1.21 V to 20 V
- Less Than 1- μA Quiescent Current in Shutdown
- Stable with 10- μF Output Capacitor
- Stable with Ceramic Capacitors
- Reverse-Battery Protection
- No Reverse Current
- Thermal Limiting

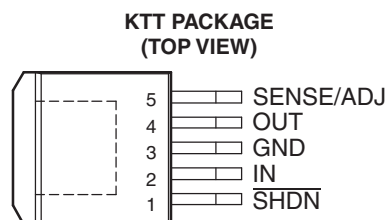
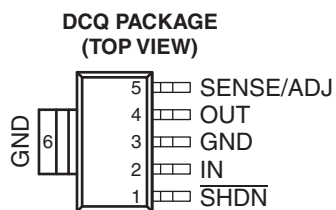
APPLICATIONS

- 3.3-V to 2.5-V Logic Power Supplies
- Post Regulator for Switching Supplies
- Wireless Infrastructure
- Radio-Frequency Systems

DESCRIPTION

The TPS7A45xx devices are low-dropout (LDO) regulators optimized for fast transient response. The device can supply 1.5 A of output current with a dropout voltage of 300 mV. Operating quiescent current is 1 mA, dropping to less than 1 μA in shutdown. Quiescent current is well controlled; it does not rise in dropout, as with many other regulators. In addition to fast transient response, the TPS7A45xx regulators have very low output noise, which makes them ideal for sensitive RF supply applications.

Output voltage range is from 1.21 V to 20 V. The TPS7A45xx regulators are stable with output capacitors as low as 10 μF . Small ceramic capacitors can be used without the necessary addition of ESR, as is common with other regulators. Internal protection circuitry includes reverse-battery protection, current limiting, thermal limiting, and reverse-current protection. The devices are available in fixed output voltages of 1.5 V, 1.8 V, 2.5 V, 3.3 V, and as an adjustable device with a 1.21-V reference voltage. The TPS7A45xx regulators are available in the 5-pin TO-263 (KTT) and 6-pin TO-223 (DCQ) packages.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION^{(1) (2)}

PRODUCT	V _{OUT}
TPS7A45xxyyyz	<p>xx is nominal output voltage 15 = 1.5 V, 18 = 1.8 V, 25 = 2.5 V, 33 = 3.3 V, 01 = adjustable yyy is package designator (DCQ or KTT) z is package quantity (R = 2500 for DCQ, 500 for KTT)</p>

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating virtual-junction temperature range (unless otherwise noted)

Input voltage range, V _{IN}	IN	-20 V to 20 V
	OUT	-20 V to 20 V
	Input-to-output differential ⁽²⁾	-20 V to 20 V
	SENSE	-20 V to 20 V
	ADJ	-7 V to 7 V
	$\overline{\text{SHDN}}$	-20 V to 20 V
Output short-circuit duration, t _{short}	Indefinite	
Maximum lead temperature (10-s soldering time), T _{lead}	300°C	
Operating virtual junction temperature range, T _J	-40°C to 125°C	
Storage temperature range, T _{stg}	-65°C to 150°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum input-to-output differential voltage cannot be achieved with all combinations of rated IN pin and OUT pin voltages. With the IN pin at 20 V, the OUT pin may not be pulled below 0 V. The total measured voltage from IN to OUT can not exceed ±20 V.

PACKAGE THERMAL DATA⁽¹⁾

PACKAGE	BOARD	θ _{JA}	θ _{JC}	θ _{JP} ⁽²⁾
TO-223 (DCQ)	Low K, JESD 51-5	53°C/W	15°C/W	N/A
TO-263 (KTT)	High K, JESD 51-5	26.5°C/W	24.1°C/W	0.38°C/W

- (1) Maximum power dissipation is a function of T_{J(max)}, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} – T_A)/θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (2) For packages with exposed thermal pads, such as QFN, PowerPAD™, and PowerFLEX™, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

ELECTRICAL CHARACTERISTICS⁽¹⁾

 Over operating temperature range $T_J = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_J	MIN	TYP ⁽²⁾	MAX	UNIT						
V_{IN}	Minimum input voltage ⁽³⁾ (4)	$I_{LOAD} = 0.5\text{ A}$		25°C		1.9		V						
		$I_{LOAD} = 1.5\text{ A}$		Full range		2.1	2.5							
V_{OUT}	Regulated output voltage ⁽⁵⁾	TPS7A4515	$V_{IN} = 2.21\text{ V}, I_{LOAD} = 1\text{ mA}$	25°C	1.485	1.5	1.515	V						
			$V_{IN} = 2.5\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	Full range	1.447	1.5	1.545							
		TPS7A4518	$V_{IN} = 2.3\text{ V}, I_{LOAD} = 1\text{ mA}$	25°C	1.782	1.8	1.818		V					
			$V_{IN} = 2.8\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	Full range	1.737	1.8	1.854							
		TPS7A4525	$V_{IN} = 3\text{ V}, I_{LOAD} = 1\text{ mA}$	25°C	2.475	2.5	2.525			V				
			$V_{IN} = 3.5\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	Full range	2.412	2.5	2.575							
		TPS7A4533	$V_{IN} = 3.8\text{ V}, I_{LOAD} = 1\text{ mA}$	25°C	3.266	3.3	3.333				V			
			$V_{IN} = 4.3\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	Full range	3.2	3.3	3.4							
		V_{ADJ}	ADJ pin voltage ⁽³⁾ (5)	TPS7A4501	$V_{IN} = 2.21\text{ V}, I_{LOAD} = 1\text{ mA}$	25°C	1.197					1.21	1.222	V
					$V_{IN} = 2.5\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	Full range	1.174					1.21	1.246	
Line regulation		TPS7A4515	$\Delta V_{IN} = 2.21\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA}$	Full range		2	6	mV						
		TPS7A4518	$\Delta V_{IN} = 2.3\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA}$	Full range		2.5	7							
		TPS7A4525	$\Delta V_{IN} = 3\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA}$	Full range		3	10							
		TPS7A4533	$\Delta V_{IN} = 3.8\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA}$	Full range		3.5	10							
		TPS7A4501 ⁽³⁾	$\Delta V_{IN} = 2.21\text{ V to }20\text{ V}, I_{LOAD} = 1\text{ mA}$	Full range		1.5	3							
Load regulation		TPS7A4515	$V_{IN} = 2.5\text{ V}, \Delta I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	25°C		2	9	mV						
			Full range				18							
		TPS7A4518	$V_{IN} = 2.8\text{ V}, \Delta I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	25°C		2	10		mV					
			Full range				20							
		TPS7A4525	$V_{IN} = 3.5\text{ V}, \Delta I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	25°C		2.5	15			mV				
			Full range				30							
		TPS7A4533	$V_{IN} = 4.3\text{ V}, \Delta I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	25°C		3	20				mV			
				-40°C to +85°C								30		
				Full range								70		
		TPS7A4501 ⁽³⁾	$V_{IN} = 2.5\text{ V}, \Delta I_{LOAD} = 1\text{ mA to }1.5\text{ A}$	25°C		2	8				mV			
-40°C to +85°C						8								
Full range						18								

- (1) The TPS7A45xx regulators are tested and specified under pulse load conditions such that $T_J = T_A$. They are fully tested at $T_A = 25^{\circ}\text{C}$. Performance at -40°C and 125°C is specified by design, characterization, and correlation with statistical process controls.
- (2) Typical values represent the likely parametric nominal values determined at the time of characterization. Typical values depend on the application and configuration and may vary over time. Typical values are not ensured on production material.
- (3) The TPS7A4501 is tested and specified for these conditions with the ADJ pin connected to the OUT pin.
- (4) For the TPS7A4501, TPS7A4515 and TPS7A4518, dropout voltages are limited by the minimum input voltage specification under some output voltage/load conditions.
- (5) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

ELECTRICAL CHARACTERISTICS ⁽¹⁾ (continued)

Over operating temperature range $T_J = -40^{\circ}\text{C}$ to 125°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_J	MIN	TYP ⁽²⁾	MAX	UNIT	
V_{DO}	Dropout voltage ⁽⁴⁾ ⁽⁶⁾ ⁽⁷⁾ $V_{IN} = V_{OUT(NOMINAL)}$	$I_{LOAD} = 1\text{ mA}$	25°C	0.02	0.05	V	
			Full range		0.06		
		$I_{LOAD} = 100\text{ mA}$	25°C	0.085	0.10		
			Full range		0.13		
		$I_{LOAD} = 500\text{ mA}$	25°C	0.17	0.180		
			Full range		0.250		
$I_{LOAD} = 1.5\text{ A}$	25°C	0.300	0.350				
	Full range		0.450				
I_{GND}	GND pin current ⁽⁷⁾ ⁽⁸⁾ $V_{IN} = V_{OUT(NOMINAL)} + 1$	$I_{LOAD} = 0\text{ mA}$	Full range	1	1.5	mA	
		$I_{LOAD} = 1\text{ mA}$	Full range	1.1	1.6		
		$I_{LOAD} = 100\text{ mA}$	Full range	3.3	3.5		
		$I_{LOAD} = 500\text{ mA}$	Full range	15	17		
		$I_{LOAD} = 1.5\text{ A}$	Full range	80	90		
e_N	Output voltage noise	$C_{OUT} = 10\text{ }\mu\text{F}$, $I_{LOAD} = 1.5\text{ A}$, $B_W = 10\text{ Hz to }100\text{ kHz}$	25°C	35		μV_{RMS}	
I_{ADJ}	ADJ pin bias current ⁽³⁾ ⁽⁹⁾		25°C	3	7	μA	
	Shutdown threshold	$V_{OUT} = \text{OFF to ON}$	Full range	0.9	2	V	
		$V_{OUT} = \text{ON to OFF}$	Full range	0.25	0.75		
$I_{\overline{SHDN}}$	\overline{SHDN} pin current	$V_{\overline{SHDN}} = 0\text{ V}$	25°C	0.01	1	μA	
		$V_{\overline{SHDN}} = 20\text{ V}$	25°C	3	20		
	Quiescent current in shutdown	$V_{IN} = 6\text{ V}$, $V_{\overline{SHDN}} = 0\text{ V}$	25°C	0.01	1	μA	
	Ripple rejection	$V_{IN} - V_{OUT} = 1.5\text{ V (avg)}$, $V_{RIPPLE} = 0.5\text{ V}_{P-P}$, $f_{RIPPLE} = 120\text{ Hz}$, $I_{LOAD} = 0.75\text{ A}$	25°C	68		dB	
I_{LIMIT}	Current limit	$V_{IN} = 7\text{ V}$, $V_{OUT} = 0\text{ V}$	25°C	2		A	
		$V_{IN} = V_{OUT(NOMINAL)} + 1$	Full range	1.6			
I_{IL}	Input reverse leakage current	$V_{IN} = -20\text{ V}$, $V_{OUT} = 0\text{ V}$	Full range		300	μA	
I_{RO}	Reverse output current ⁽¹⁰⁾	TPS7A4515	$V_{OUT} = 1.5\text{ V}$, $V_{IN} < 1.5\text{ V}$	25°C	600	1000	μA
		TPS7A4518	$V_{OUT} = 1.8\text{ V}$, $V_{IN} < 1.8\text{ V}$	25°C	600	1000	
		TPS7A4525	$V_{OUT} = 2.5\text{ V}$, $V_{IN} < 2.5\text{ V}$	25°C	600	1000	
		TPS7A4533	$V_{OUT} = 3.3\text{ V}$, $V_{IN} < 3.3\text{ V}$	25°C	600	1000	
		TPS7A4501	$V_{OUT} = 1.21\text{ V}$, $V_{IN} < 1.21\text{ V}$	25°C	300	500	

- (6) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is equal to: $V_{IN} - V_{DROPOUT}$.
- (7) To satisfy requirements for minimum input voltage, the TPS7A4501 is tested and specified for these conditions with an external resistor divider (two 4.12-k Ω resistors) for an output voltage of 2.4 V. The external resistor divider adds a 300-mA DC load on the output.
- (8) GND pin current is tested with $V_{IN} = (V_{OUT(NOMINAL)} + 1\text{ V})$ and a current source load. The GND pin current decreases at higher input voltages.
- (9) ADJ pin bias current flows into the ADJ pin.
- (10) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out the GND pin.

DEVICE INFORMATION

TERMINAL FUNCTIONS

PIN		DESCRIPTION
NO.	NAME	
1	$\overline{\text{SHDN}}$	Shutdown. $\overline{\text{SHDN}}$ is used to put the TPS7A45xx regulators into a low-power shutdown state. The output is off when $\overline{\text{SHDN}}$ is pulled low. $\overline{\text{SHDN}}$ can be driven either by 5-V logic or open-collector logic with a pullup resistor. The pullup resistor is required to supply the pullup current of the open-collector gate, normally several microamperes, and $\overline{\text{SHDN}}$ current, typically 3 μA . If unused, $\overline{\text{SHDN}}$ must be connected to V_{IN} . The device is in the low-power shutdown state if $\overline{\text{SHDN}}$ is not connected.
2	IN	Input. Power is supplied to the device through IN. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general, the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. A bypass capacitor (ceramic) in the range of 1 μF to 10 μF is sufficient. The TPS7A45xx regulators are designed to withstand reverse voltages on IN with respect to ground and on OUT. In the case of a reverse input, which can happen if a battery is plugged in backwards, the device acts as if there is a diode in series with its input. There is no reverse current flow into the regulator, and no reverse voltage appears at the load. The device protects both itself and the load.
3	GND	Ground. For the KTT package, the exposed thermal pad is connected to GND and must be soldered to the PCB for rated thermal performance.
4	OUT	Output. The output supplies power to the load. A minimum output capacitor (ceramic) of 10 μF is required to prevent oscillations. Larger output capacitors are required for applications with large transient loads to limit peak voltage transients.
5	ADJ	Adjust. For the adjustable version only (TPS7A4501), this is the input to the error amplifier. ADJ is internally clamped to $\pm 7\text{ V}$. It has a bias current of 3 μA that flows into the pin. ADJ voltage is 1.21 V referenced to ground, and the output voltage range is 1.21 V to 20 V.
5	SENSE	Sense. For fixed-voltage versions (TPS7A4515, TPS7A4518, TPS7A4525, and TPS7A4533), SENSE is the input to the error amplifier. Optimum regulation is obtained at the point where SENSE is connected to the OUT pin of the regulator. In critical applications, small voltage drops are caused by the resistance (R_p) of PC traces between the regulator and the load. These may be eliminated by connecting SENSE to the output at the load as shown in Figure 32 . Note that the voltage drop across the external PC traces adds to the dropout voltage of the regulator. SENSE bias current is 600 μA at the rated output voltage. SENSE can be pulled below ground (as in a dual supply system in which the regulator load is returned to a negative supply) and still allow the device to start and operate.
6	GND	Ground. DCQ package only.

TYPICAL CHARACTERISTICS

DROPOUT VOLTAGE
vs
OUTPUT CURRENT

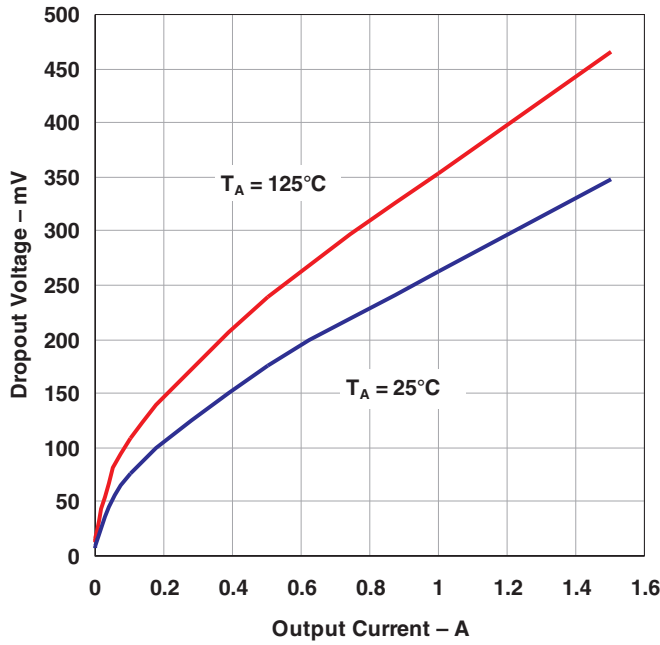


Figure 1.

DROPOUT VOLTAGE
vs
TEMPERATURE

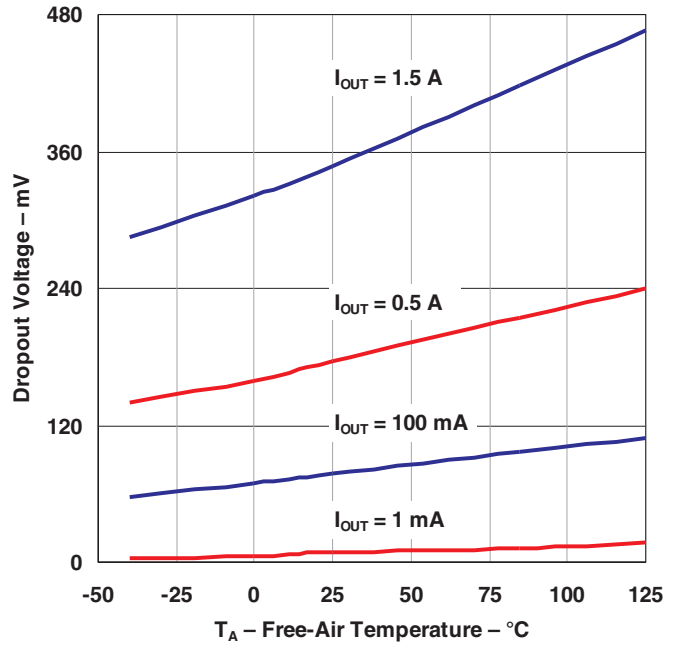


Figure 2.

QUIESCENT CURRENT
vs
TEMPERATURE

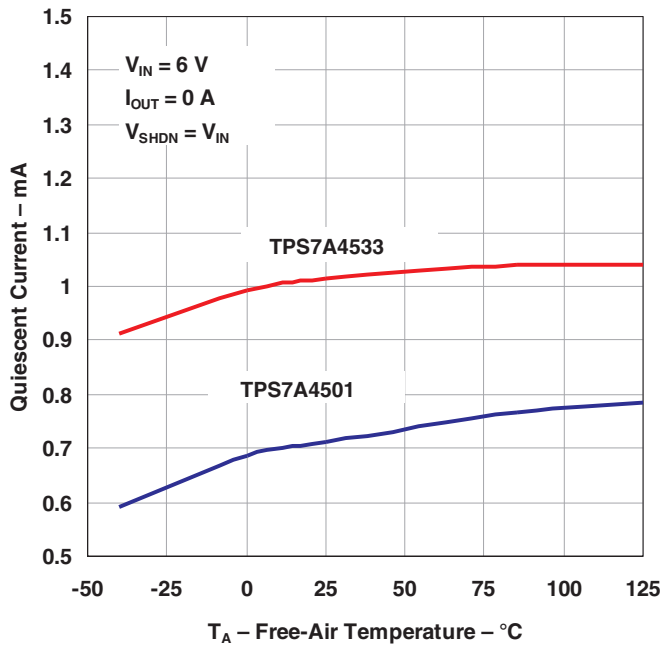


Figure 3.

OUTPUT VOLTAGE
vs
TEMPERATURE

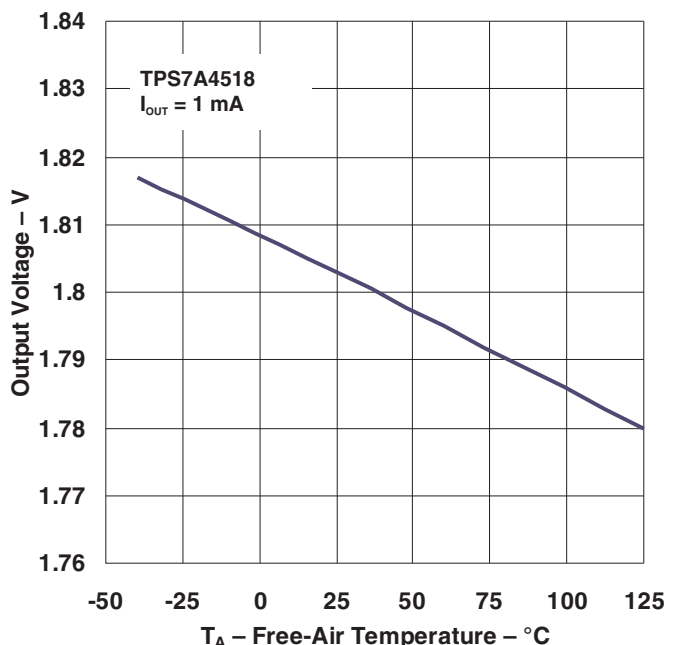


Figure 4.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE
VS
TEMPERATURE

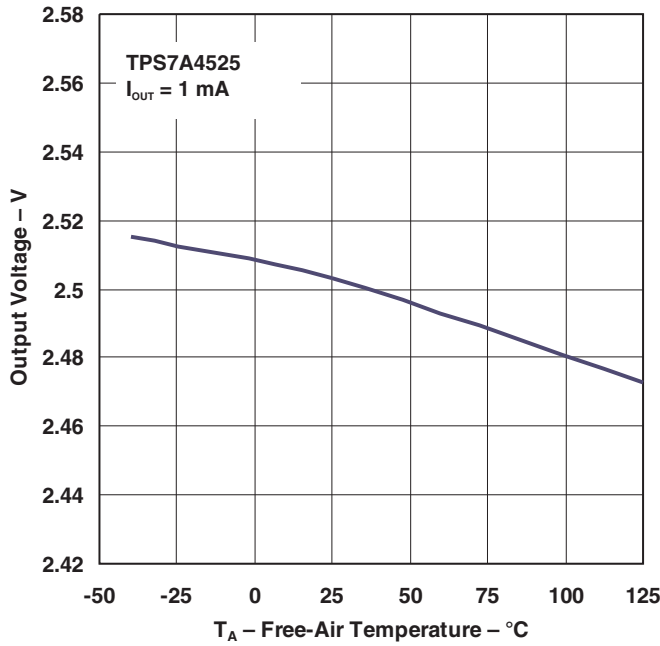


Figure 5.

OUTPUT VOLTAGE
VS
TEMPERATURE

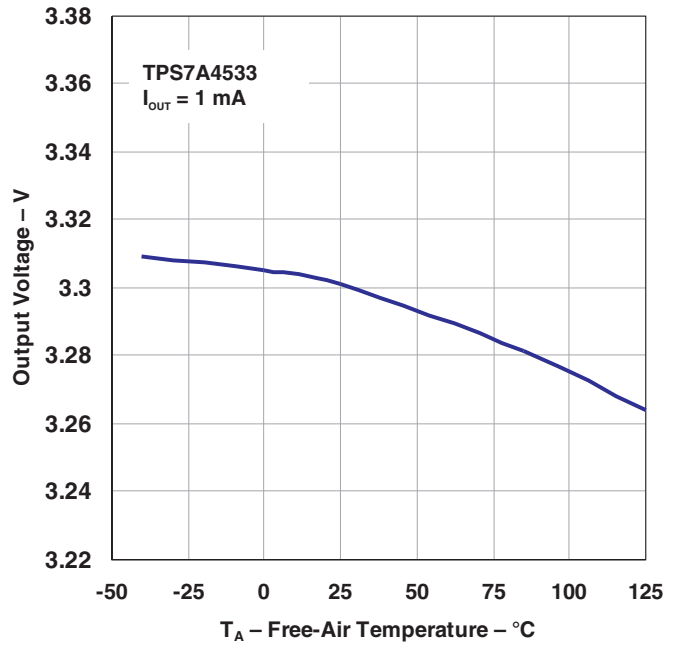


Figure 6.

OUTPUT VOLTAGE
VS
TEMPERATURE

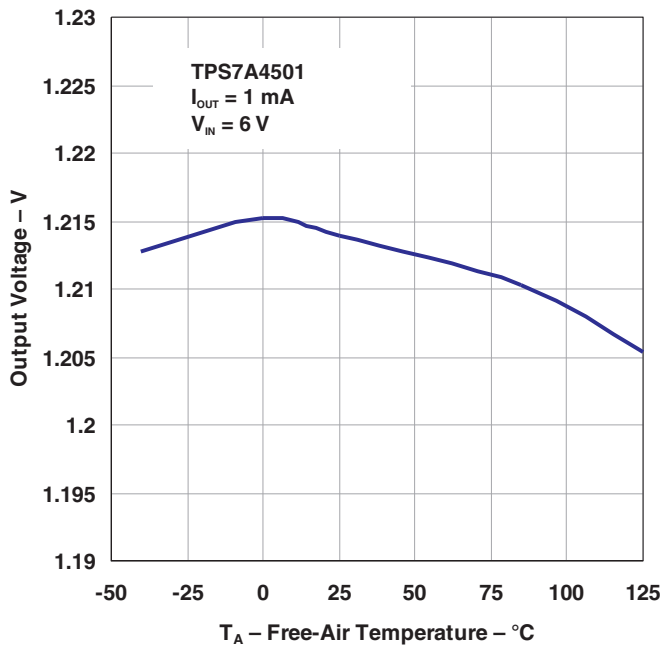


Figure 7.

QUIESCENT CURRENT
VS
INPUT VOLTAGE

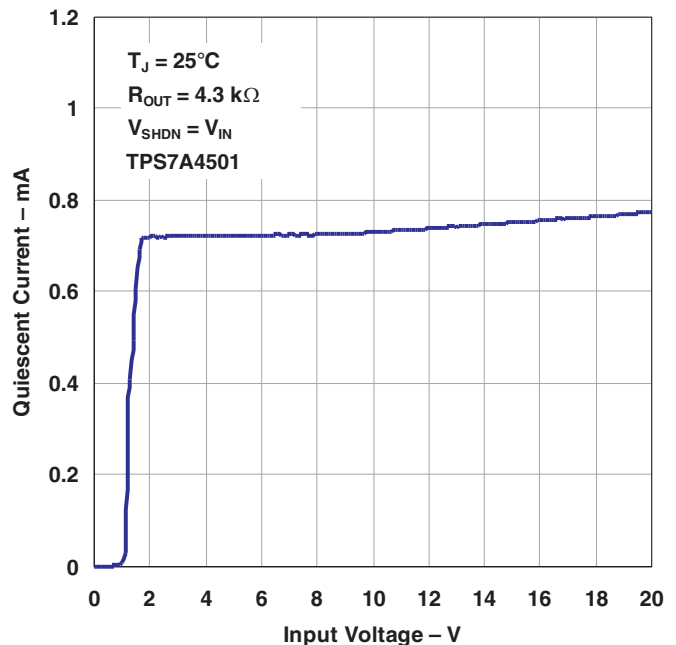


Figure 8.

TYPICAL CHARACTERISTICS (continued)

GROUND CURRENT
VS
INPUT VOLTAGE

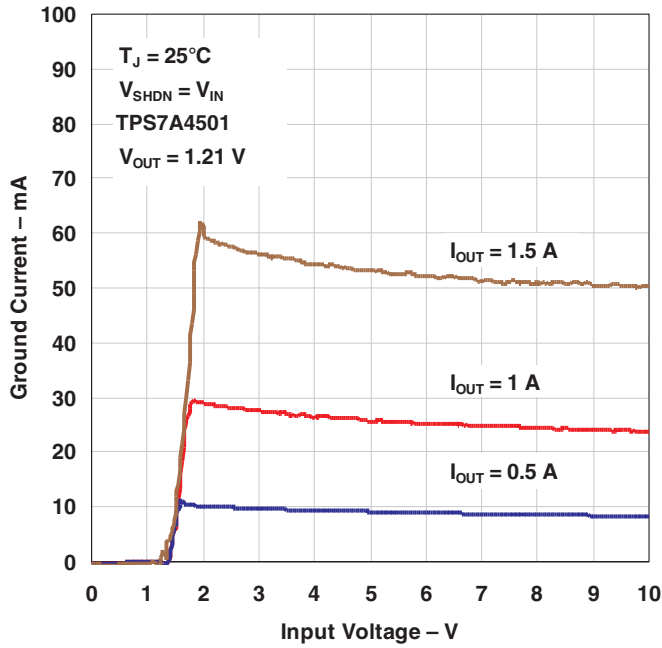


Figure 9.

GROUND CURRENT
VS
INPUT VOLTAGE

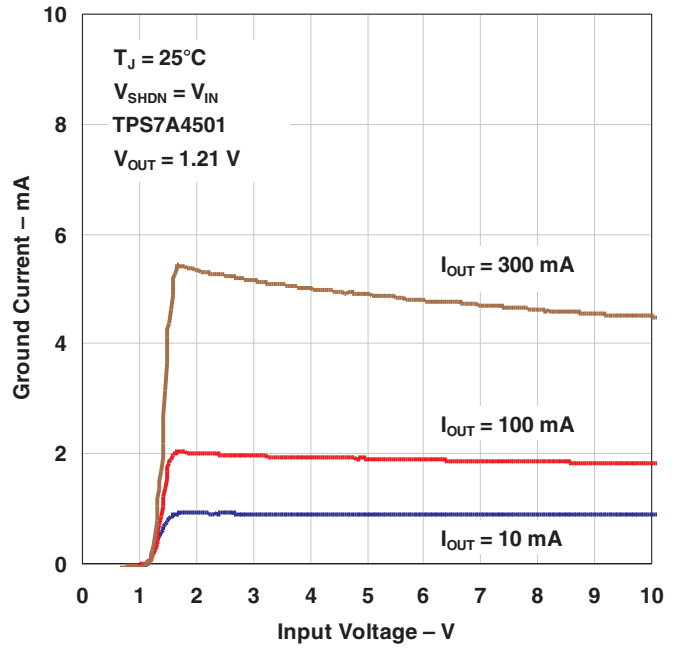


Figure 10.

GROUND CURRENT
VS
INPUT VOLTAGE

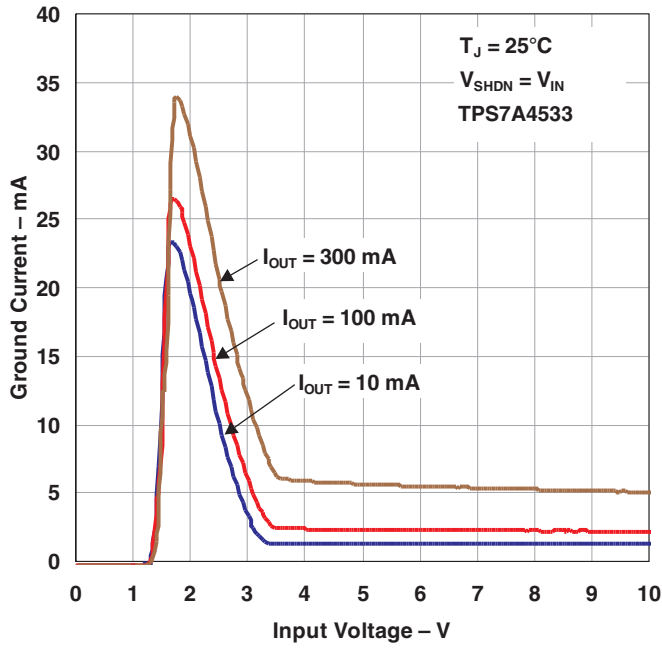


Figure 11.

GROUND CURRENT
VS
INPUT VOLTAGE

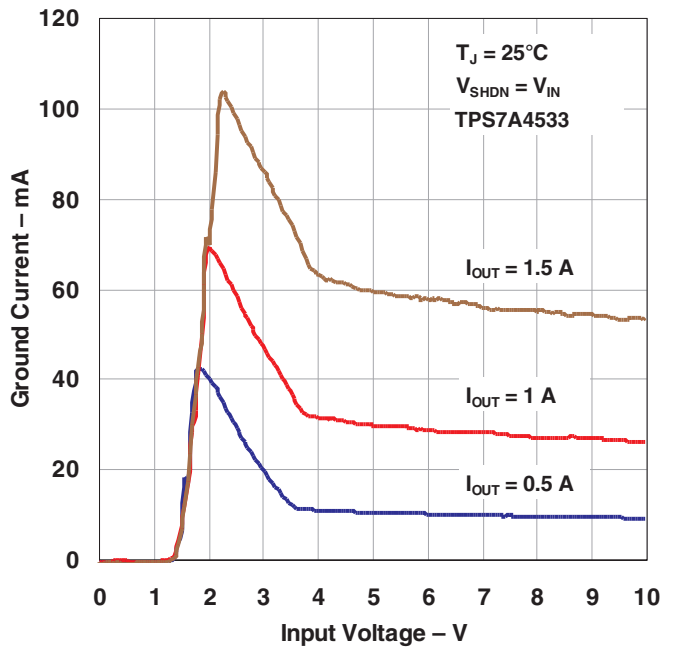


Figure 12.

TYPICAL CHARACTERISTICS (continued)

GROUND CURRENT
VS
OUTPUT CURRENT

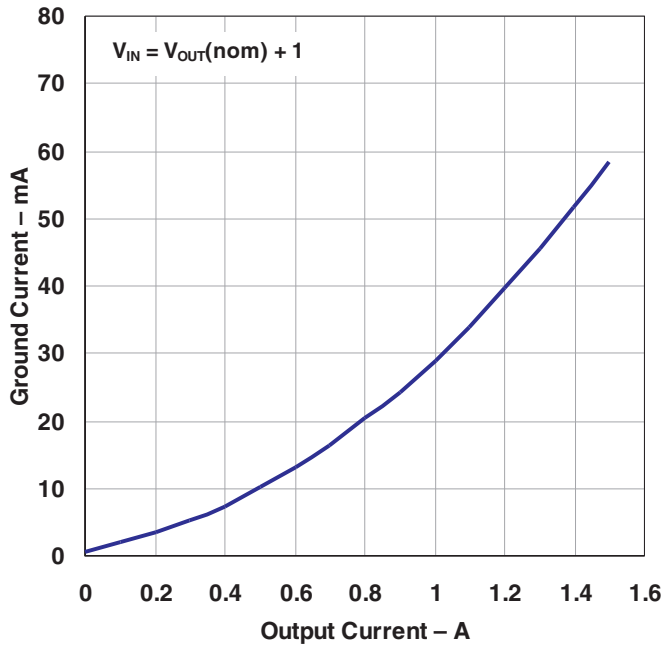


Figure 13.

SHDN INPUT CURRENT
VS
TEMPERATURE

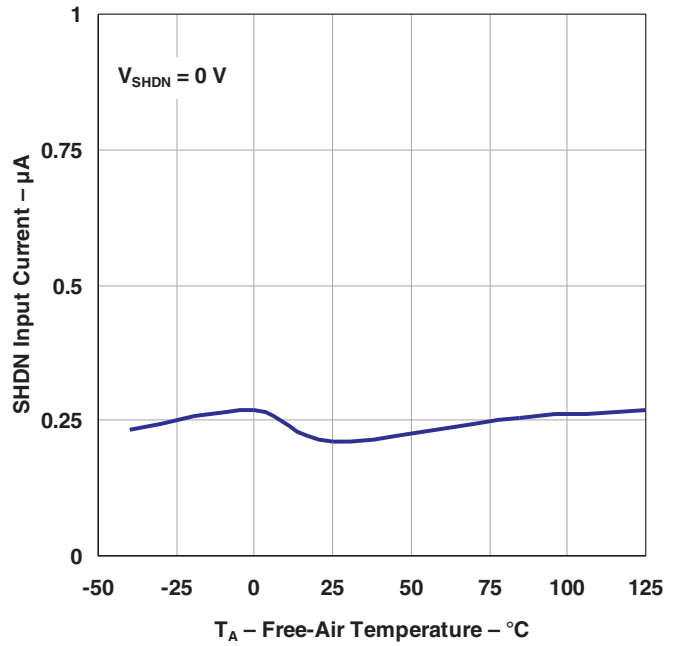


Figure 14.

SHDN INPUT CURRENT
VS
SHDN INPUT VOLTAGE

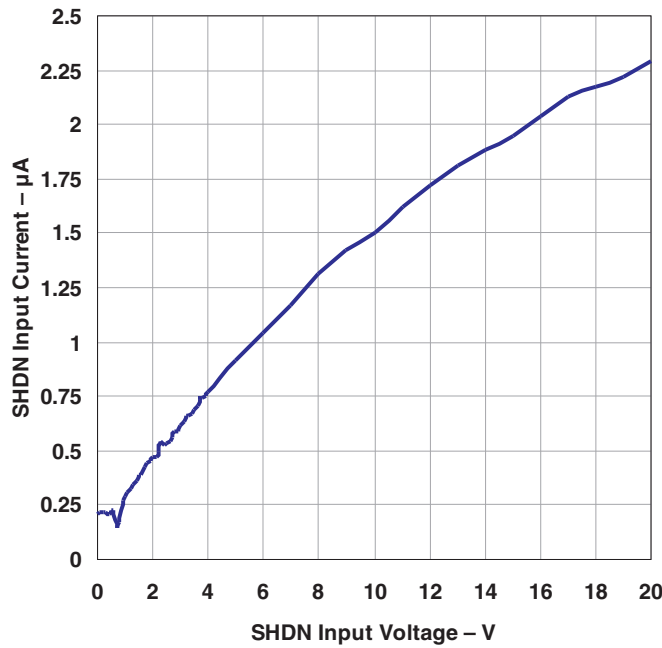


Figure 15.

SHDN THRESHOLD (OFF TO ON)
VS
TEMPERATURE

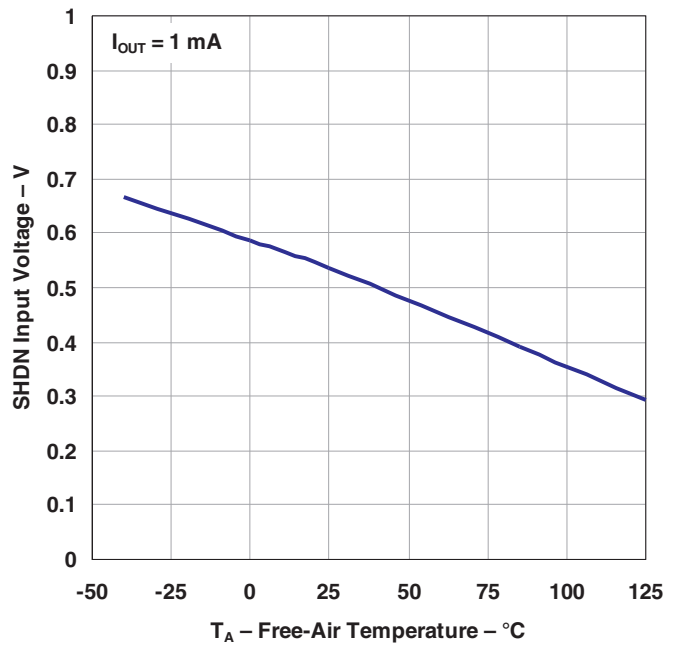


Figure 16.

TYPICAL CHARACTERISTICS (continued)

SHDN THRESHOLD (ON TO OFF)
VS
TEMPERATURE

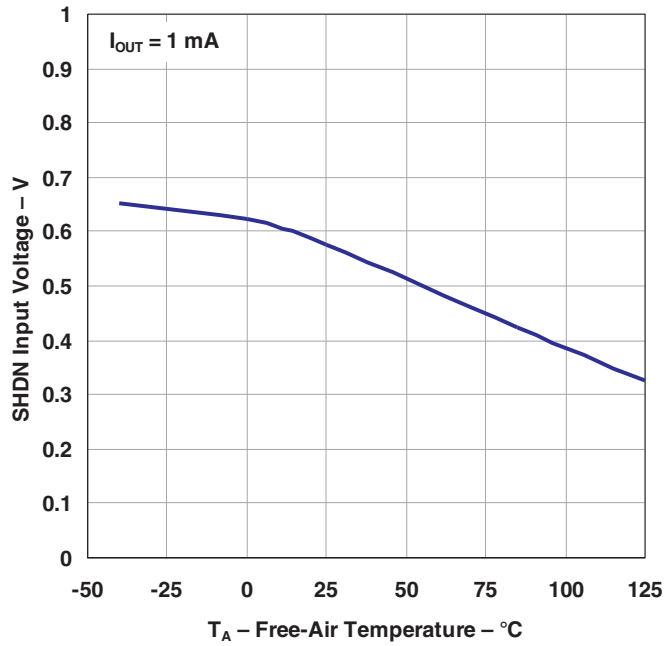


Figure 17.

ADJ BIAS CURRENT
VS
TEMPERATURE

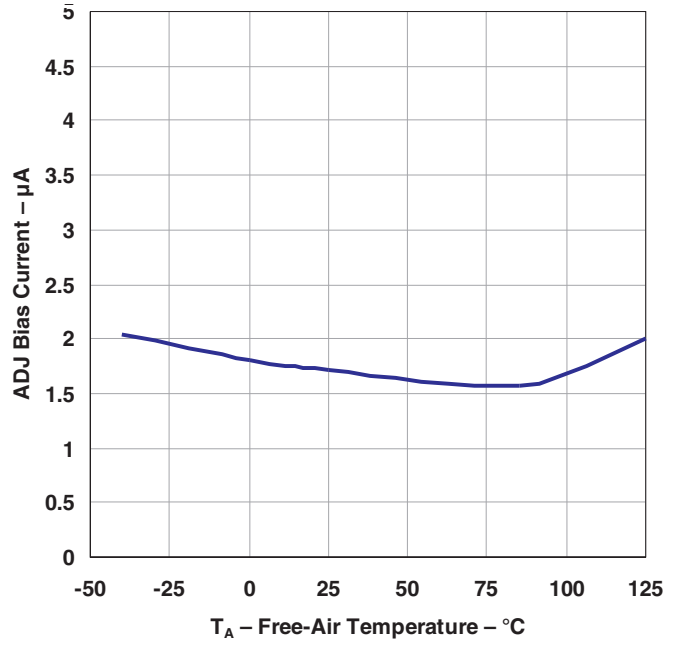


Figure 18.

CURRENT LIMIT
VS
INPUT/OUTPUT DIFFERENTIAL VOLTAGE

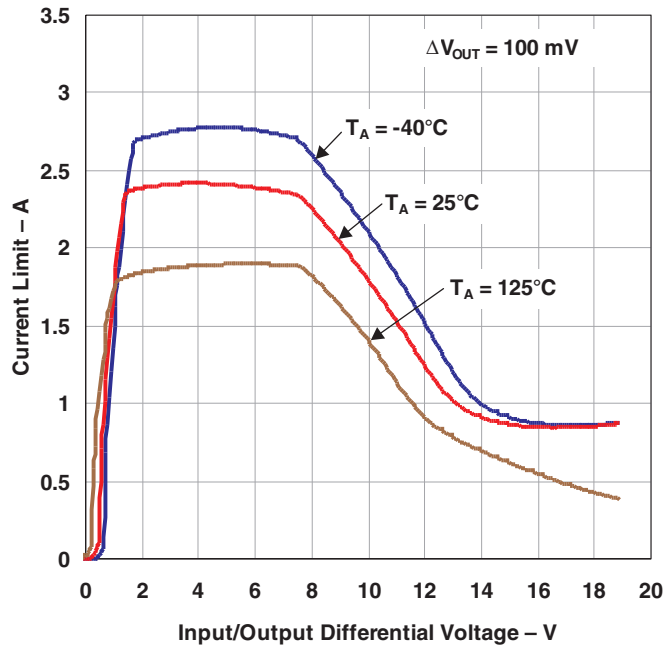


Figure 19.

CURRENT LIMIT
VS
TEMPERATURE

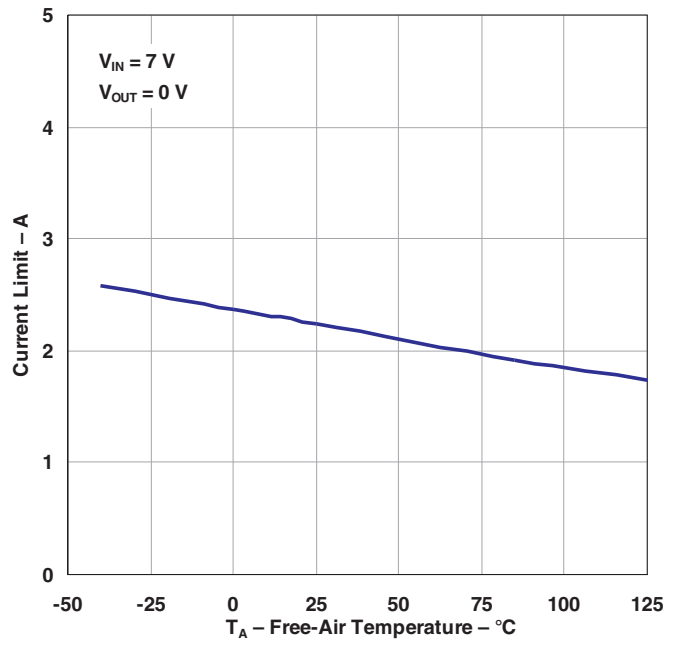


Figure 20.

TYPICAL CHARACTERISTICS (continued)

REVERSE OUTPUT CURRENT
VS
OUTPUT VOLTAGE

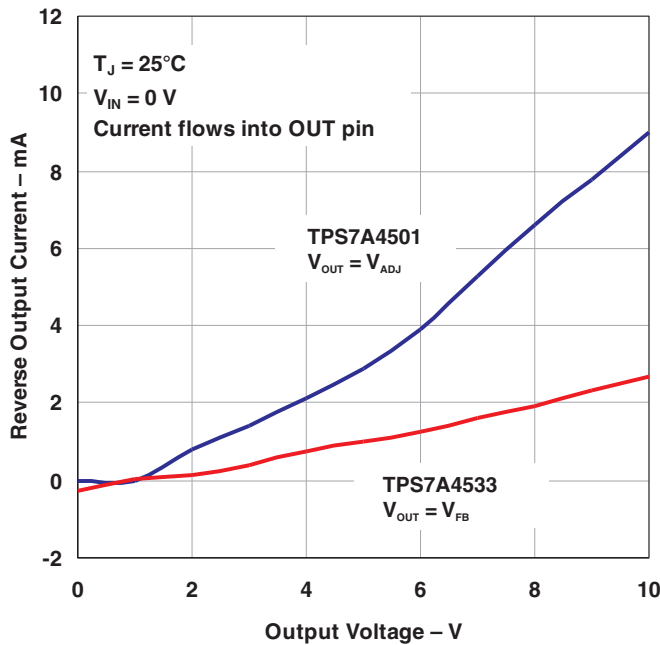


Figure 21.

REVERSE OUTPUT CURRENT
VS
TEMPERATURE

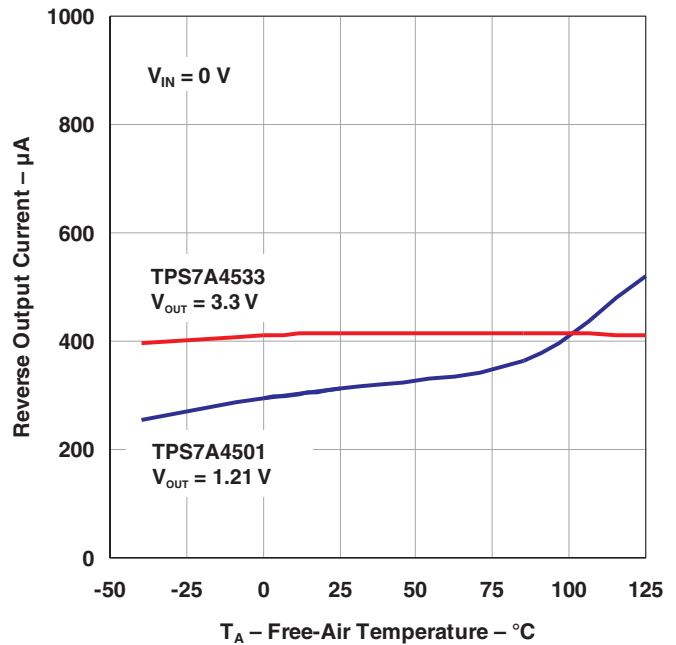


Figure 22.

RIPPLE REJECTION
VS
FREQUENCY

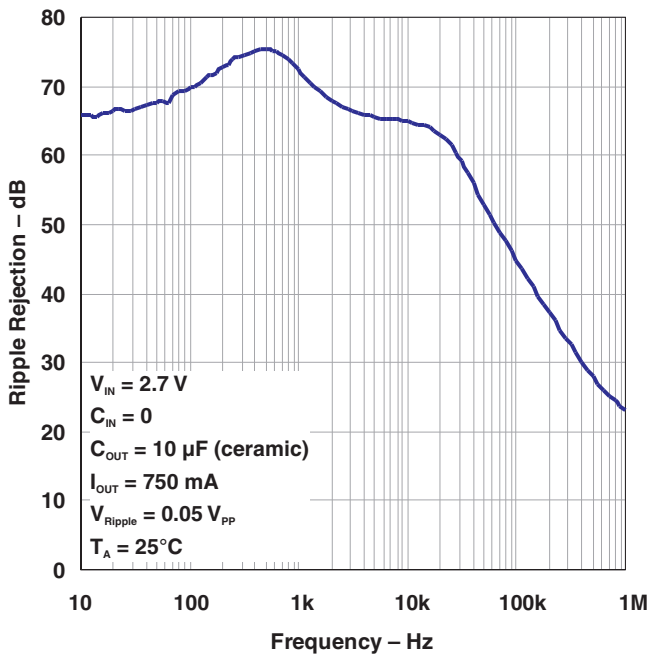


Figure 23.

LOAD REGULATION
VS
TEMPERATURE

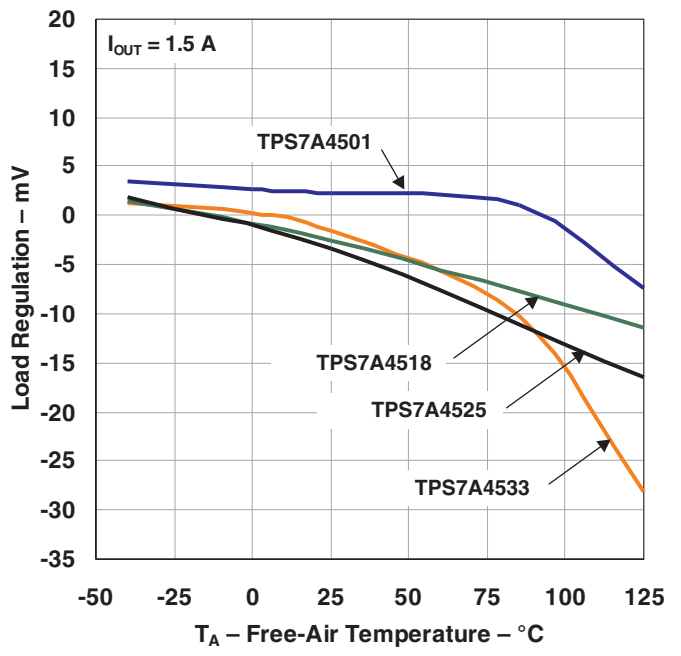


Figure 24.

TYPICAL CHARACTERISTICS (continued)

OUTPUT NOISE VOLTAGE
VS
FREQUENCY

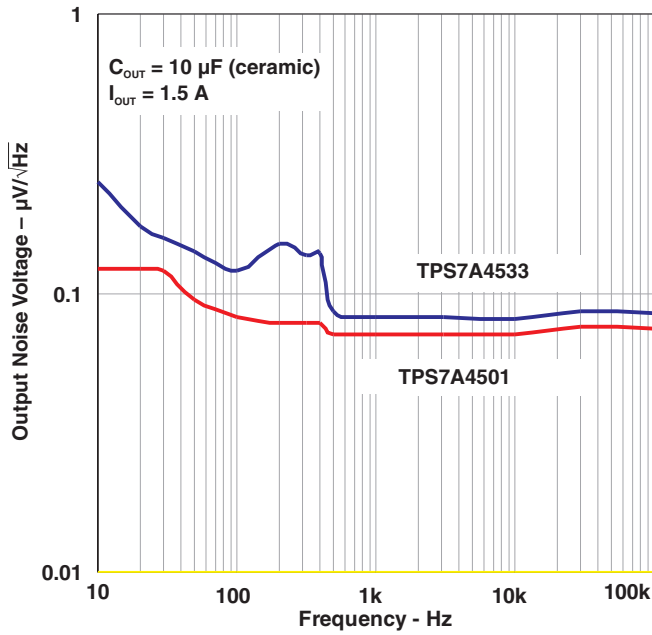


Figure 25.

LOAD TRANSIENT RESPONSE

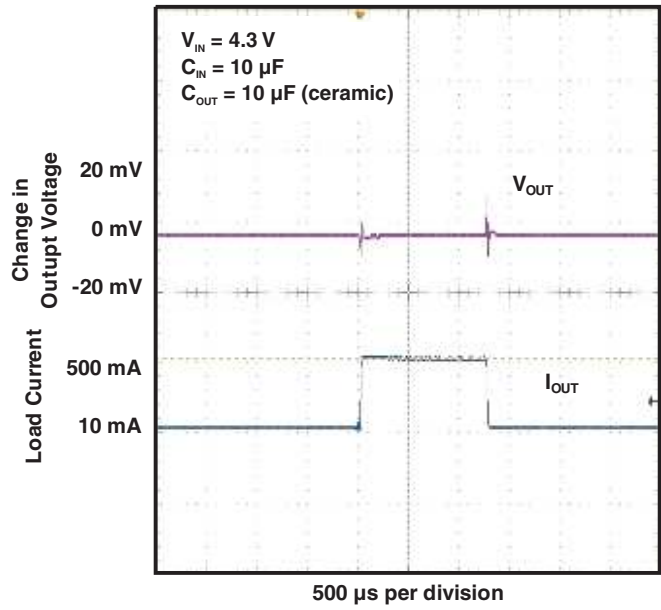
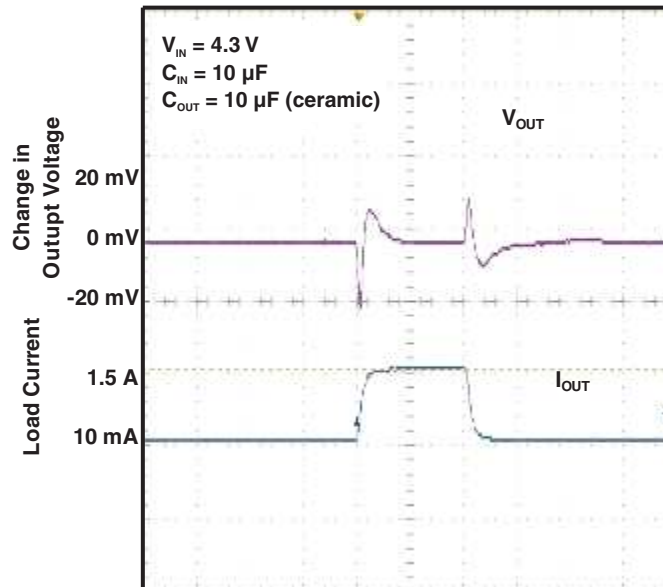


Figure 26.

LOAD TRANSIENT RESPONSE



500 μs per division
Figure 27.

APPLICATION INFORMATION

The TPS7A45xx series are 1.5-A low-dropout regulators optimized for fast transient response. The devices are capable of supplying 1.5 A at a dropout voltage of 300 mV. The low operating quiescent current (1 mA) drops to less than 1 μ A in shutdown. In addition to the low quiescent current, the TPS7A45xx regulators incorporate several protection features that make them ideal for use in battery-powered systems. The devices are protected against both reverse input and reverse output voltages. In battery-backup applications where the output can be held up by a backup battery when the

input is pulled to ground, the TPS7A45xx acts as if it has a diode in series with its output and prevents reverse current flow. Additionally, in dual-supply applications where the regulator load is returned to a negative supply, the output can be pulled below ground by as much as 20 V and still allow the device to start and operate.

Typical Applications

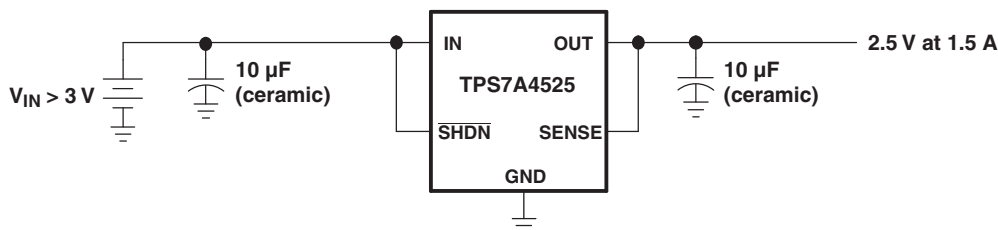
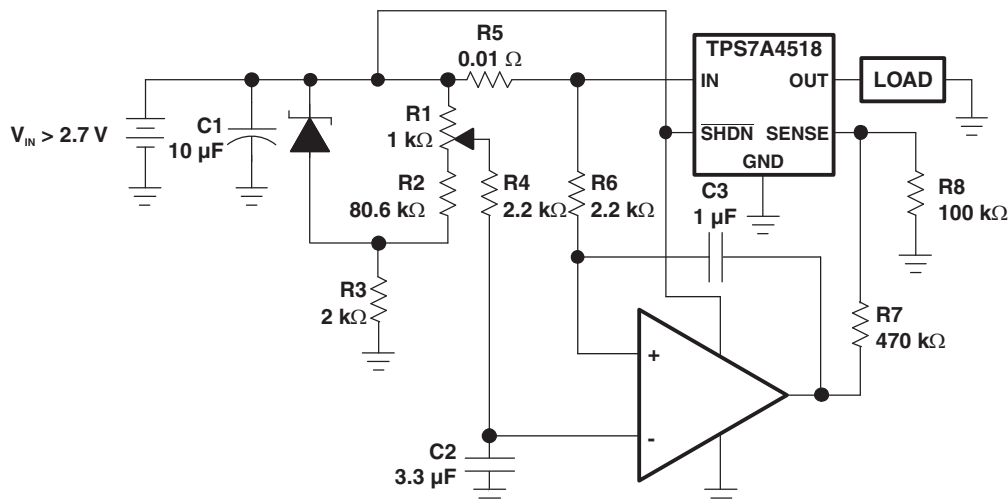
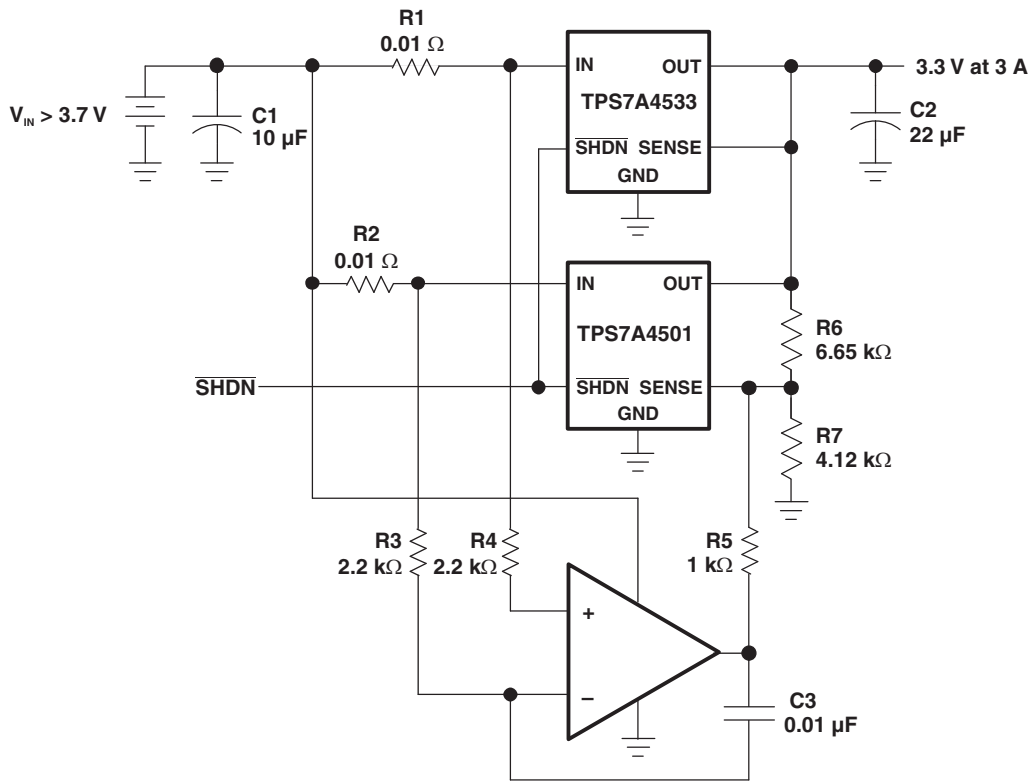


Figure 29. 3.3 V to 2.5 V Regulator



NOTE: All capacitors are ceramic.

Figure 30. Adjustable Current Source



NOTE: All capacitors are ceramic.

Figure 31. Paralleling Regulators for Higher Output Current

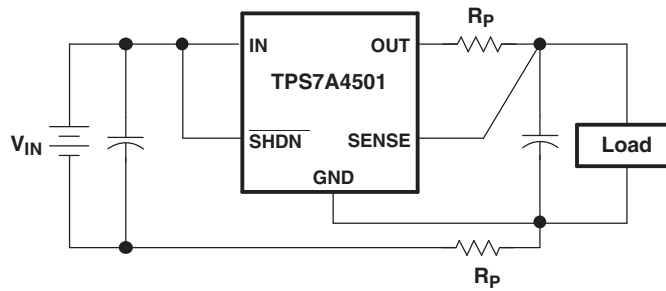
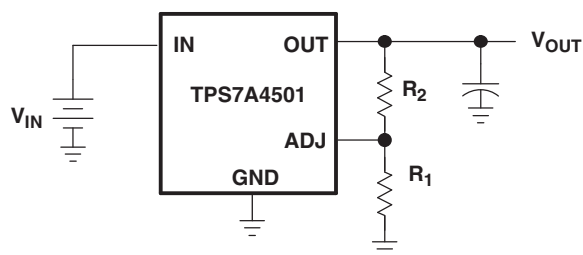


Figure 32. Kelvin Sense Connection

Adjustable Operation

The adjustable version of the TPS7A45xx has an output voltage range of 1.21 V to 20 V. The output voltage is set by the ratio of two external resistors as shown in Figure 33. The device maintains the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to $(1.21 \text{ V}/R1)$, and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 3 μA at 25°C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula shown in Figure 33. The value of R1 should be less than 4.17 k Ω to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off, and the divider current is zero.



$$V_{\text{OUT}} = 1.21 \text{ V} \left(1 + \frac{R_2}{R_1} \right) + (I_{\text{ADJ}})(R_2)$$

$$V_{\text{ADJ}} = 1.21 \text{ V}$$

$$I_{\text{ADJ}} = 3 \mu\text{A at } 25^\circ\text{C}$$

$$\text{Output range} = 1.21 \text{ V to } 20 \text{ V}$$

Figure 33. Adjustable Operation

The adjustable device is tested and specified with the ADJ pin tied to the OUT pin for an output voltage of 1.21 V. Specifications for output voltages greater than 1.21 V are proportional to the ratio of the desired output voltage to 1.21 V: $V_{\text{OUT}}/1.21 \text{ V}$. For example, load regulation for an output current change of 1 mA to 1.5 A is –3 mV (typ) at $V_{\text{OUT}} = 1.21 \text{ V}$. At $V_{\text{OUT}} = 5 \text{ V}$, load regulation is:

$$(5 \text{ V}/1.21 \text{ V})(-3 \text{ mV}) = -12.4 \text{ mV}$$

Output Capacitance and Transient Response

The TPS7A45xx regulators are designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10 μF with an ESR of 3 Ω or less is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes. Bypass capacitors, used to decouple individual components powered by the TPS7A45xx, increase the effective output capacitor value.

Extra consideration must be given to the use of

ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10- μF Y5V capacitor can exhibit an effective value as low as 1 μF to 2 μF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to the way a piezoelectric accelerometer or microphone works. For a ceramic capacitor the stress can be induced by vibrations in the system or thermal transients.

Overload Recovery

Like many IC power regulators, the TPS7A45xx has safe operating area protection. The safe area protection decreases the current limit as input-to-output voltage increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltage. The protection is designed to provide some output current at all values of input-to-output voltage up to the device breakdown.

When power is first turned on, as the input voltage rises, the output follows the input, allowing the regulator to start up into very heavy loads. During start up, as the input voltage is rising, the input-to-output voltage differential is small, allowing the regulator to supply large output currents. With a high input voltage, a problem can occur wherein removal of an output short does not allow the output voltage to recover. Other regulators also exhibit this phenomenon, so it is not unique to the TPS7A45xx.

The problem occurs with a heavy output load when the input voltage is high and the output voltage is low. Common situations occur immediately after the removal of a short circuit or when the shutdown pin is pulled high after the input voltage has already been turned on. The load line for such a load may intersect the output current curve at two points. If this happens, there are two stable output operating points for the regulator. With this double intersection, the input power supply may need to be cycled down to zero and brought up again to make the output recover.

Output Voltage Noise

The TPS7A45xx regulators have been designed to provide low output voltage noise over the 10-Hz to 100-kHz bandwidth while operating at full load. Output voltage noise is typically 35 nV/√Hz over this frequency bandwidth for the TPS7A4501 (adjustable version). For higher output voltages (generated by using a resistor divider), the output voltage noise is gained up accordingly. This results in RMS noise over the 10-Hz to 100-kHz bandwidth of 14 μV_{RMS} for the TPS7A4501, increasing to 38 μV_{RMS} for the TPS7A4533.

Higher values of output voltage noise may be measured when care is not exercised with regard to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TPS7A45xx. Power-supply ripple rejection must also be considered; the TPS7A45xx regulators do not have unlimited power-supply rejection and pass a small portion of the input noise through to the output.

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the input/output voltage differential: $I_{OUT}(V_{IN} - V_{OUT})$
2. GND pin current multiplied by the input voltage: $I_{GND}V_{IN}$.

The GND pin current can be found using the GND Pin Current graphs in *Typical Characteristics*. Power dissipation is equal to the sum of the two components listed above.

The TPS7A45xx series regulators have internal thermal limiting designed to protect the device during overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface-mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

Table 1 lists thermal resistance for several different board sizes and copper areas. All measurements were taken in still air on 1/16" FR-4 board with 1-oz copper.

Table 1. Thermal Data

COPPER AREA		BOARD AREA	THERMAL RESISTANCE (JUNCTION TO AMBIENT)
TOPSIDE ⁽¹⁾	BACKSIDE		
KTT Package (5-Pin TO-263)			
2500 mm ²	2500 mm ²	2500 mm ²	23°C/W
1000 mm ²	2500 mm ²	2500 mm ²	25°C/W
125 mm ²	2500 mm ²	2500 mm ²	33°C/W

(1) Device is mounted on topside.

Calculating Junction Temperature

Example: Given an output voltage of 3.3 V, an input voltage range of 4 V to 6 V, an output current range of 0 mA to 500 mA, and a maximum ambient temperature of 50°C, what is the maximum junction temperature?

The power dissipated by the device is equal to:

$$I_{OUT(MAX)}(V_{IN(MAX)} - V_{OUT}) + I_{GND}(V_{IN(MAX)})$$

where,

$$I_{OUT(MAX)} = 500 \text{ mA}$$

$$V_{IN(MAX)} = 6 \text{ V}$$

$$I_{GND} \text{ at } (I_{OUT} = 500 \text{ mA}, V_{IN} = 6 \text{ V}) = 10 \text{ mA}$$

So,

$$P = 500 \text{ mA} \times (6 \text{ V} - 3.3 \text{ V}) + 10 \text{ mA} \times 6 \text{ V} = 1.41 \text{ W}$$

Using a KTT package, the thermal resistance is in the range of 23°C/W to 33°C/W, depending on the copper area. So the junction temperature rise above ambient is approximately equal to:

$$1.41 \text{ W} \times 28^\circ\text{C/W} = 39.5^\circ\text{C}$$

The maximum junction temperature is then be equal to the maximum junction-temperature rise above ambient plus the maximum ambient temperature or:

$$T_{JMAX} = 50^\circ\text{C} + 39.5^\circ\text{C} = 89.5^\circ\text{C}$$

Protection Features

The TPS7A45xx regulators incorporate several protection features which make them ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the devices are protected against reverse input voltages, reverse output voltages and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 125°C.

The input of the device withstands reverse voltages of 20 V. Current flow into the device is limited to less than 1 mA (typically less than 100 µA), and no negative voltage appears at the output. The device protects both itself and the load. This provides protection against batteries that can be plugged in backward.

The output of the TPS7A45xx can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. For fixed voltage versions, the output acts like a large resistor, typically 5 kΩ or higher, limiting current flow to typically less than 600 µA. For adjustable versions, the output acts like an open circuit; no current flows out of the pin. If the input is powered by a voltage source, the output sources the short-circuit current of the device and protects itself by thermal limiting. In this case, grounding the SHDN pin turns off the device and stops the output from sourcing the short-circuit current.

The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin acts like an open circuit when pulled below ground and like a large resistor (typically 5 kΩ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7-V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5-V output from the 1.21-V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5 mA when the ADJ pin is at 7 V. The 13-V difference between OUT and ADJ divided by the 5-mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6 kΩ.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage, or is left open circuit.

When the IN pin of the TPS7A45xx is forced below the OUT pin or the OUT pin is pulled above the IN pin, input current typically drops to less than 2 µA. This can happen if the input of the device is connected to a discharged (low voltage) battery and the output is held up by either a backup battery or a second regulator circuit. The state of the SHDN pin has no effect on the reverse output current when the output is pulled above the input.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
TPS7A4501DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS7A4501DCQT	ACTIVE	SOT-223	DCQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS7A4501KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS7A4515DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS7A4515KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS7A4515KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS7A4515KTTT	PREVIEW	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS7A4518DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS7A4518KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS7A4518KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS7A4518KTTT	PREVIEW	DDPAK/ TO-263	KTT	5		TBD	Call TI	Call TI
TPS7A4525DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS7A4525KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS7A4525KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
TPS7A4533DCQR	ACTIVE	SOT-223	DCQ	6	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS7A4533DCQT	ACTIVE	SOT-223	DCQ	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS7A4533KTTR	ACTIVE	DDPAK/ TO-263	KTT	5	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4501DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.8	7.3	1.88	8.0	12.0	Q3
TPS7A4501DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TPS7A4501KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS7A4515DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TPS7A4515KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS7A4518DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TPS7A4518KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS7A4525DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TPS7A4525KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2
TPS7A4533DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TPS7A4533DCQT	SOT-223	DCQ	6	250	177.8	12.4	7.05	7.45	1.88	8.0	12.0	Q3
TPS7A4533KTTR	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.6	15.8	4.9	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4501DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS7A4501DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TPS7A4501KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4515DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS7A4515KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4518DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS7A4518KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4525DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS7A4525KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0
TPS7A4533DCQR	SOT-223	DCQ	6	2500	358.0	335.0	35.0
TPS7A4533DCQT	SOT-223	DCQ	6	250	180.0	180.0	85.0
TPS7A4533KTTR	DDPAK/TO-263	KTT	5	500	340.0	340.0	38.0

DCQ (R-PDSO-G6)

PLASTIC SMALL-OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Controlling dimension in inches.
 - $\triangle D$ Body length and width dimensions are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
 - $\triangle E$ Lead width dimension does not include dambar protrusion.
 - $\triangle F$ Lead width and thickness dimensions apply to solder plated leads.
 - G. Interlead flash allow 0.008 inch max.
 - H. Gate burr/protrusion max. 0.006 inch.
 - I. Datums A and B are to be determined at Datum H.

DCQ (R-PDSO-G6)

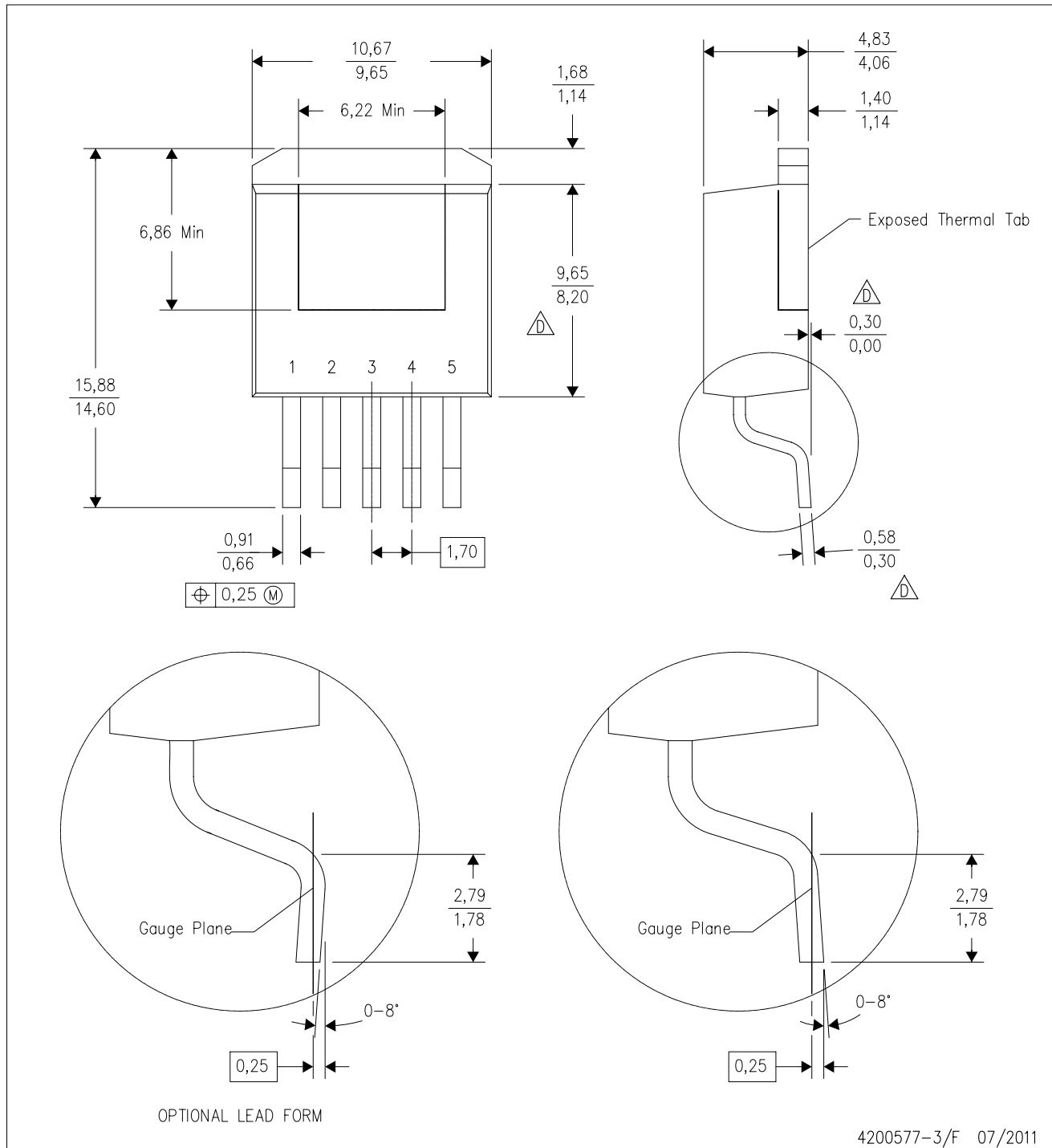
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-SM-782 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - Please refer to the product data sheet for specific via and thermal dissipation requirements.

KTT (R-PSFM-G5)

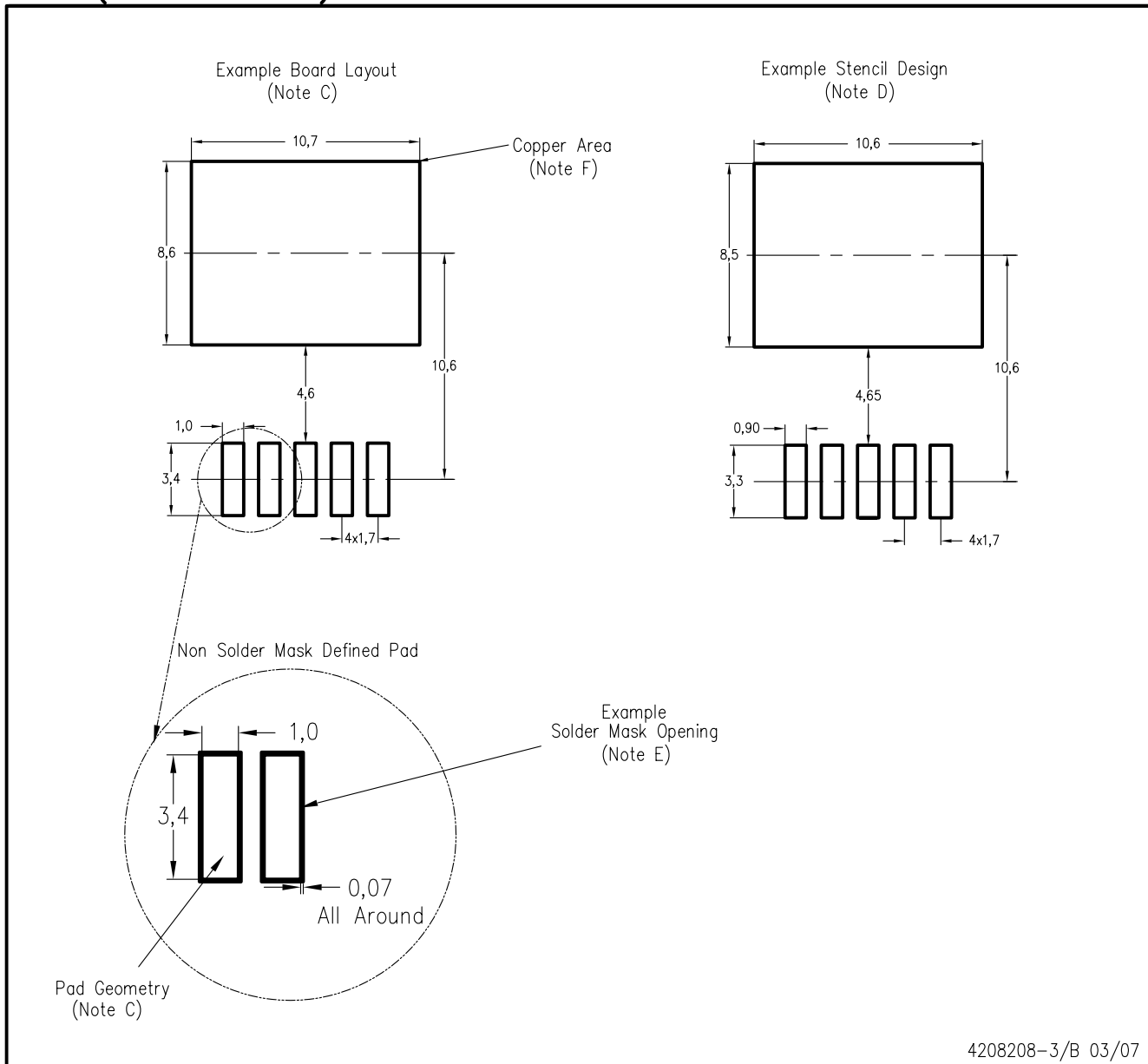
PLASTIC FLANGE-MOUNT PACKAGE



4200577-3/F 07/2011

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- $\triangle D$ Falls within JEDEC TO-263 variation BA, except minimum lead thickness, maximum seating height, and minimum body length.

KTT (R-PSFM-G5)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-SM-782 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
 - F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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