Window Comparator for Over- and Undervoltage Detection

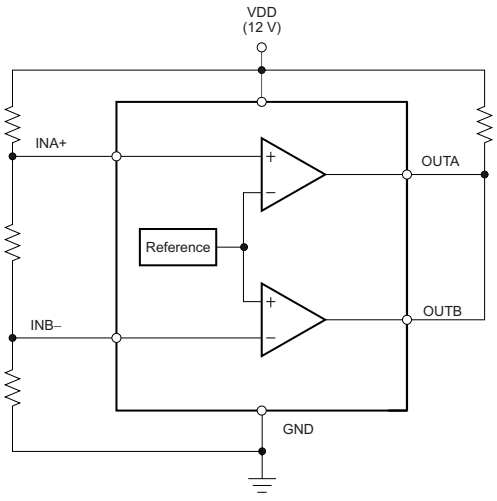
Check for Samples: TPS3700

FEATURES

- **Wide Supply Voltage Range: 1.8 V to 18 V**
- **Adjustable Threshold: Down to 400 mV**
- **Open-Drain Outputs for Over- and Undervoltage Detection**
- **Low Quiescent Current: 6 µA (typ)**
- **High Threshold Accuracy: 1.0% Over Temperature**
- **Internal Hysteresis: 6.5 mV (typ)**
- **Temperature Range: –40°C to +125°C**
- **Available in a TSOT23-6 Package**

APPLICATIONS

- **Industrial Control Systems**
- **Automotive Systems**
- **DSP, Microcontroller, or Microprocessor Applications**
- **Notebook and Desktop Computers**
- **Portable- and Battery-Powered Products**
- **FPGA and ASIC Applications**

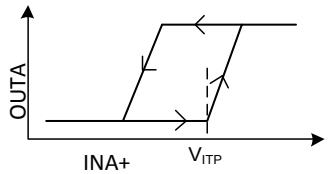


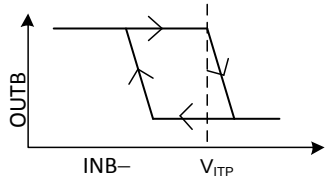
DESCRIPTION

The TPS3700 wide-supply voltage window comparator operates over a 1.8-V to 18-V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for over- and undervoltage detection. The TPS3700 can be used as a window comparator or as two independent voltage monitors; the monitored voltage can be set with the use of external resistors.

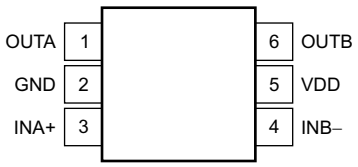
OUTA is driven low when the voltage at INA+ drops below $V_{ITP} – V_{HYS}$, and goes high when the voltage returns above the respective threshold (V_{ITP}). OUTB is driven low when the voltage at INB– rises above V_{ITP}, and goes high when the voltage drops below the respective threshold ($V_{ITP} – V_{HYS}$). Both comparators in the TPS3700 include built-in hysteresis for filtering to reject brief glitches, thereby ensuring stable output operation without false triggering.

The TPS3700 is available in a ThinSOT23-6 package and is specified over a temperature range of T_J = –40°C to +125°C.





DDC PACKAGE
SOT23-6
(TOP VIEW)



PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	DESCRIPTION
TPS3700**yyyz**	**yyy** is package designator **z** is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	VCC	–0.3	+20	V
	V_{OUTA}, V_{OUTB}	–0.3	+20	V
	V_{INA+}, $V_{INB–}$	–0.3	+7	V
Current	I_{OL}		40	mA
Temperature	Operating junction, T_J	–40	+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge rating (ESD)(3)	Human body model (HBM)		2	kV
	Charge device model (CDM)		500	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS3700 DDC (SOT23) 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	TBD	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	TBD	
θ_{JB}	Junction-to-board thermal resistance	TBD	
ψ_{JT}	Junction-to-top characterization parameter	TBD	
ψ_{JB}	Junction-to-board characterization parameter	TBD	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	TBD	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

Over the operating temperature range of T_J = –40°C to +125°C, and 1.8 V < V_{CC}< 18 V, unless otherwise noted.
Typical values are at T_J = +25°C and V_{CC} = 5 V.

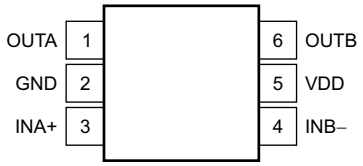
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage range		1.8		18	V
$V_{(POR)}$	Power-on reset voltage(1)	V_{OL} (max) = 0.2 V, $I_{(OUT)}$ = 15 µA			0.8	V
V_{ITP}	Positive-going input threshold voltage	V_{CC} = 1.8 V	396	400	404	mV
		V_{CC} = 18 V	396	400	404	mV
V_{ITN}	Negative-going input threshold voltage	V_{CC} = 1.8 V	387	393.5	400	mV
		V_{CC} = 18 V	387	393.5	400	mV
V_{HYS}	Hysteresis voltage (HYS = V_{ITP} – V_{ITN})			6.5	13	mV
I_{IN}	Input current (at IN pin)	V_{CC} = 1.8 V, V_{IN} = 6.5 V	–25	10	25	nA
		V_{CC} = 18 V, V_{IN} = 6.5 V	–25	10	25	nA
		V_{CC} = 1.8 V and 18 V, V_{IN} = 0.1 V		10	15	nA
V_{OL}	Low-level output voltage	10-mV input overdrive, V_{CC} = 1.3 V, I_{OUT} = 0.4 mA			250	mV
		10-mV input overdrive, V_{CC} = 1.8 V, I_{OUT} = 3 mA			250	mV
		10-mV input overdrive, V_{CC} = 5 V, I_{OUT} = 5 mA			250	mV
$I_{lkg(OD)}$	Open-drain output leakage current	V_{IN} = 40-mV overdrive, V_{CC} = 1.8 V and 18 V, V_{OUT} = V_{CC}			1	µA
		V_{IN} = 40-mV overdrive, V_{CC} = 1.8 V, V_{OUT} = 18 V			1	µA
$t_{PD(HL)}$	High-to-low propagation delay	V_{CC} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_{OL} = 400 mV		18		µs
$t_{PD(LH)}$	Low-to-high propagation delay	V_{CC} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_{OH} = 0.9 × V_{CC}		29		µs
t_R	Output rise time	V_{CC} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_O = (0.1 to 0.9) × V_{CC}		2.2		µs
t_F	Output fall time	V_{CC} = 5 V, 10-mV input overdrive, R_L = 10 kΩ, V_O = (0.1 to 0.9) × V_{CC}		0.22		µs
I_{CC}	Supply current	V_{CC} = 1.8 V, no load		5	13	µA
		V_{CC} = 5 V		6	14	µA
		V_{CC} = 12 V		6	14	µA
		V_{CC} = 18 V		7	15	µA
	Startup delay(2)			150		µs

(1) The lowest supply voltage (V_{CC}) at which output is active; $t_r(V_{CC})$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) During power on, V_{CC} must exceed 1.8 V for at least 150 µs before the output is in a correct state.

PRODUCT PREVIEW

PIN CONFIGURATIONS

DDC PACKAGE
SOT23-6
(TOP VIEW)



PIN ASSIGNMENTS

PIN NAME	PIN NO.	DESCRIPTION
GND	2	Ground
OUTB	6	INB– comparator open-drain output. OUTB goes low when the voltage at this comparator exceeds V_{ITP}. The output goes high when the sense voltage returns below the respective threshold (V_{ITP} – V_{HYS}).
INB–	4	This pin is connected to the voltage to be monitored with the use of an external resistor. When the voltage at this terminal exceeds the threshold voltage (V_{ITP}), OUTB goes low.
OUTA	1	INA+ comparator open-drain output. OUTA goes low when the voltage at this comparator is below V_{ITP} – V_{HYS}. The output goes high when the sense voltage returns above the respective threshold (V_{ITP}).
INA+	3	This pin is connected to the voltage to be monitored with the use of an external resistor. When the voltage at this terminal drops below the threshold voltage (V_{ITP} – V_{HYS}), OUTA goes low.
VCC	5	Supply voltage input. Connect a 1.8-V to 18-V supply to VCC to power the device. It is good analog design practice to place a 0.1-µF ceramic capacitor close to this pin.

PRODUCT PREVIEW

PACKAGING INFORMATION

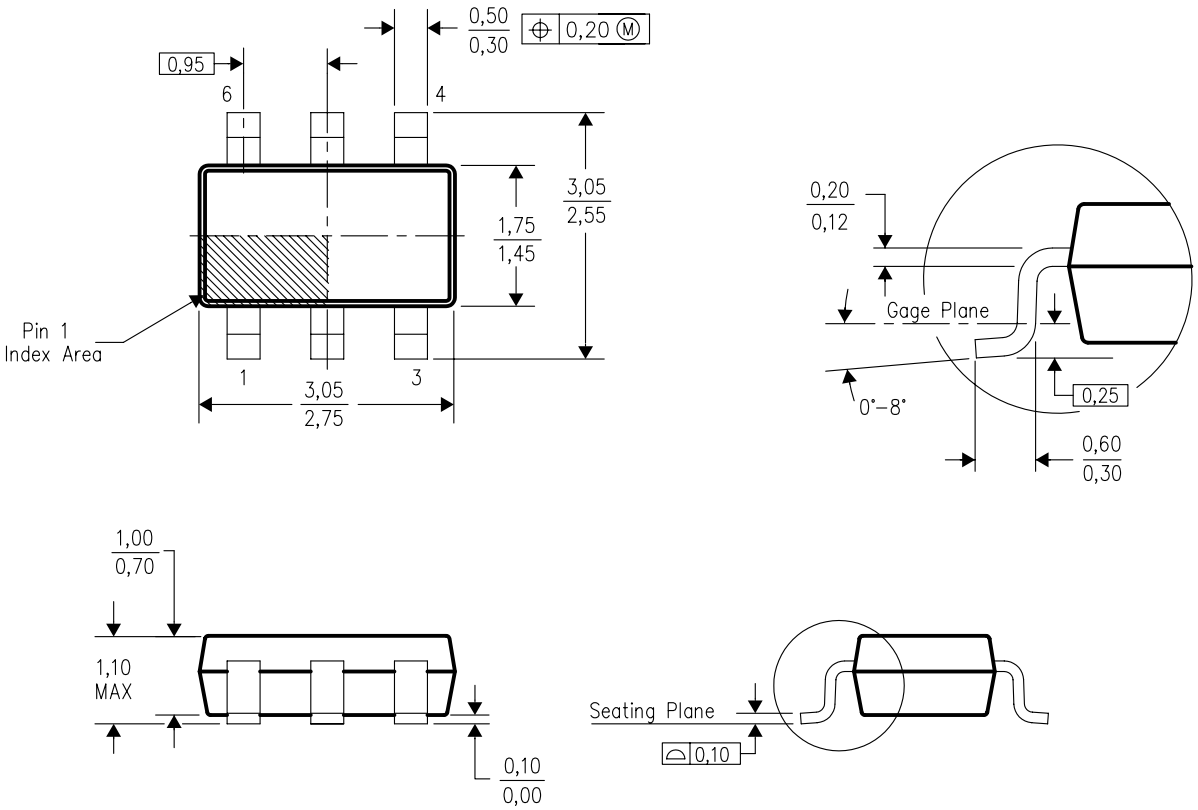
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS3700DDCR	PREVIEW	SOT	DDC	6	3000	TBD	Call TI	Call TI	
TPS3700DDCT	PREVIEW	SOT	DDC	6	250	TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DDC (R–PDSO–G6) PLASTIC SMALL–OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AA (6 pin).

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