

## AUTOSWITCHING POWER MUX

Check for Samples: [TPS2114A](#), [TPS2115A](#)

### FEATURES

- **Two-Input, One-Output Power Multiplexer with Low  $r_{DS(on)}$  Switches:**
  - 120 m $\Omega$  Typ (TPS2114A)
  - 84 m $\Omega$  Typ (TPS2115A)
- **Reverse and Cross-Conduction Blocking**
- **Wide Operating Voltage Range: 2.8 V to 5.5 V**
- **Low Standby Current: 0.5- $\mu$ A Typ**
- **Low Operating Current: 55- $\mu$ A Typ**
- **Adjustable Current Limit**
- **Controlled Output Voltage Transition Times Limit Inrush Current and Minimize Output Voltage Hold-Up Capacitance**
- **CMOS- and TTL-Compatible Control Inputs**
- **Manual and Auto-Switching Operating Modes**
- **Thermal Shutdown**
- **Available in TSSOP-8 and 3mm  $\times$  3mm SON-8 Packages**

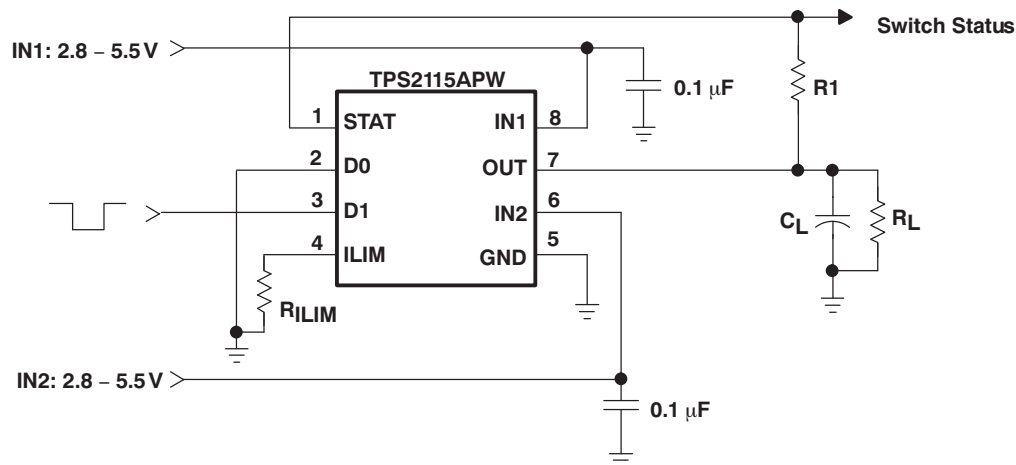
### APPLICATIONS

- PCs
- PDAs
- Digital Cameras
- Modems
- Cell Phones
- Digital Radios
- MP3 Players

### DESCRIPTION

The TPS211xA family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8–5.5 V and delivering up to 1 A. The TPS211xA family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

### TYPICAL APPLICATION



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### DEVICE INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE	ORDERING NUMBER	MARKING
–40°C to 85°C	TSSOP-8 (PW)	TPS2114APW	2114A
		TPS2115APW	2115A
	SON-8 (DRB)	TPS2115ADRB	CGF

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

		VALUE		UNIT
		MIN	MAX	
Voltage	IN1, IN2, D0, D1, ILIM <sup>(2)</sup>	–0.3	6	V
	V <sub>O(OUT)</sub> , V <sub>O(STAT)</sub> <sup>(2)</sup>	–0.3	6	V
Current	Output sink, I <sub>O(STAT)</sub>		5	mA
	Continuous output, I <sub>O</sub> (TPS2114A)		0.9	A
	Continuous output, I <sub>O</sub> (TPS2115A)		1.5	A
Power dissipation	Continuous total	See <a href="#">Power Dissipation Ratings</a> table		
Temperature	Operating virtual junction, T <sub>J</sub>	–40	125	°C
	Storage, T <sub>stg</sub>	–65	150	°C
ESD ratings	Human body model, HBM		2	kV
	Charge device model, CDM		500	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to GND.

### AVAILABLE OPTIONS

FEATURE	TPS2114A	TPS2115A
Current limit adjustment range	0.31 A to 0.75 A	0.63 A to 1.25 A
Switching modes	Manual	Yes
	Automatic	Yes
Switch status output	Yes	Yes
Package	TSSOP-8	TSSOP-8
		SON-8

**PACKAGE DISSIPATION RATINGS**

PACKAGE	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A \leq 25^\circ\text{C}$ POWER RATING	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
TSSOP-8 (PW)	3.9 mW/ $^\circ\text{C}$	387 mW	213 mW	155 mW
SON-8 (DRB)	25.0 mW/ $^\circ\text{C}$	2.50 W	1.38 W	1.0 W

**RECOMMENDED OPERATING CONDITIONS**

		MIN	NOM	MAX	UNIT
Input voltage at IN1, $V_{I(IN1)}$	$V_{I(IN2)} \geq 2.8\text{ V}$	1.5		5.5	V
	$V_{I(IN2)} < 2.8\text{ V}$	2.8		5.5	V
Input voltage at IN2, $V_{I(IN2)}$	$V_{I(IN1)} \geq 2.8\text{ V}$	1.5		5.5	V
	$V_{I(IN1)} < 2.8\text{ V}$	2.8		5.5	V
Input voltage, $V_{I(DO)}$ , $V_{I(D1)}$		0		5.5	V
Current limit adjustment range, $I_{O(OUT)}$	TPS2114A	0.31		0.75	A
	TPS2115A	0.63		1.25	A
Operating virtual junction temperature, $T_J$		-40		125	$^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS: POWER SWITCH**

Over recommended operating junction temperature range,  $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$ , and  $R_{ILIM} = 400\ \Omega$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TPS2114A			TPS2115A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$r_{DS(on)}^{(1)}$ Drain-source on-state resistance (INx-OUT)	$T_J = 25^\circ\text{C}$ , $I_L = 500\text{ mA}$ , $V_{I(IN1)} = V_{I(IN2)} = 5.0\text{ V}$		120	140		84	110	m $\Omega$
	$T_J = 25^\circ\text{C}$ , $I_L = 500\text{ mA}$ , $V_{I(IN1)} = V_{I(IN2)} = 3.3\text{ V}$		120	140		84	110	m $\Omega$
	$T_J = 25^\circ\text{C}$ , $I_L = 500\text{ mA}$ , $V_{I(IN1)} = V_{I(IN2)} = 2.8\text{ V}$		120	140		84	110	m $\Omega$
	$T_J = 125^\circ\text{C}$ , $I_L = 500\text{ mA}$ , $V_{I(IN1)} = V_{I(IN2)} = 5.0\text{ V}$			220			150	m $\Omega$
	$T_J = 125^\circ\text{C}$ , $I_L = 500\text{ mA}$ , $V_{I(IN1)} = V_{I(IN2)} = 3.3\text{ V}$			220			150	m $\Omega$
	$T_J = 125^\circ\text{C}$ , $I_L = 500\text{ mA}$ , $V_{I(IN1)} = V_{I(IN2)} = 2.8\text{ V}$			220			150	m $\Omega$

- (1) The TPS211xA can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

## ELECTRICAL CHARACTERISTICS: GENERAL

Over recommended operating junction temperature range,  $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$ , and  $R_{ILIM} = 400\ \Omega$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TPS2114A			UNIT
		MIN	TYP	MAX	
<b>LOGIC INPUTS (D0 AND D1)</b>					
$V_{IH}$	High-level input voltage	2			V
$V_{IL}$	Low-level input voltage				0.7
Input current at D0 or D1	D0 or D1 = high, sink current				1
	D0 or D1 = low, source current	0.5	1.4	5	$\mu\text{A}$
<b>SUPPLY AND LEAKAGE CURRENTS</b>					
Supply current from IN1 (operating)	D1 = high, D0 = low (IN1 active), $V_{I(IN1)} = 5.5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$	55			90
	D1 = high, D0 = low (IN1 active), $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5.5\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$	1			12
	D0 = D1 = low (IN2 active), $V_{I(IN1)} = 5.5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$				75
	D0 = D1 = low (IN2 active), $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5.5\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$				1
Supply current from IN2 (operating)	D1 = high, D0 = low (IN1 active), $V_{I(IN1)} = 5.5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$				1
	D1 = high, D0 = low (IN1 active), $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5.5\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$				75
	D0 = D1 = low (IN2 active), $V_{I(IN1)} = 5.5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$	1			12
	D0 = D1 = low (IN2 active), $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5.5\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$	55			90
Quiescent current from IN1 (STANDBY)	D0 = D1 = high (inactive), $V_{I(IN1)} = 5.5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$	0.5			2
	D0 = D1 = high (inactive), $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5.5\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$				1
Quiescent current from IN2 (STANDBY)	D0 = D1 = high (inactive), $V_{I(IN1)} = 5.5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$				1
	D0 = D1 = high (inactive), $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5.5\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$	0.5			2
Forward leakage current from IN1 (measured from OUT to GND)	D0 = D1 = high (inactive), $V_{I(IN1)} = 5.5\text{ V}$ , IN2 open, $V_{O(OUT)} = 0\text{ V}$ (shorted), $T_J = 25^\circ\text{C}$	0.1			5
Forward leakage current from IN2 (measured from OUT to GND)	D0 = D1 = high (inactive), $V_{I(IN2)} = 5.5\text{ V}$ , IN1 open, $V_{O(OUT)} = 0\text{ V}$ (shorted), $T_J = 25^\circ\text{C}$	0.1			5
Reverse leakage current to INx (measured from INx to GND)	D0 = D1 = high (inactive), $V_{I(INx)} = 0\text{ V}$ , $V_{O(OUT)} = 5.5\text{ V}$ , $T_J = 25^\circ\text{C}$	0.3			5
<b>CURRENT LIMIT CIRCUIT</b>					
Current limit accuracy, TPS2114A	$R_{ILIM} = 400\ \Omega$	0.51	0.63	0.80	A
	$R_{ILIM} = 700\ \Omega$	0.30	0.36	0.50	A
Current limit accuracy, TPS2115A	$R_{ILIM} = 400\ \Omega$	0.95	1.25	1.56	A
	$R_{ILIM} = 700\ \Omega$	0.47	0.71	0.99	A
$t_d$	Current limit settling time	Time for short-circuit output current to settle within 10% of its steady state value.			1
	Input current at ILIM	$V_{I(ILIM)} = 0\text{ V}$ , $I_{O(OUT)} = 0\text{ A}$			-15
<b>UVLO</b>					
IN1 and IN2 UVLO	Falling edge	1.15	1.25		V
	Rising edge	1.30		1.35	V
IN1 and IN2 UVLO hysteresis		30	57	65	mV
Internal $V_{DD}$ UVLO (the higher of IN1 and IN2)	Falling edge	2.4	2.53		V
	Rising edge	2.58		2.8	V
Internal $V_{DD}$ UVLO hysteresis		30	50	75	mV
UVLO deglitch for IN1, IN2	Falling edge	110			$\mu\text{s}$

**ELECTRICAL CHARACTERISTICS: GENERAL (continued)**

Over recommended operating junction temperature range,  $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$ , and  $R_{ILIM} = 400\ \Omega$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	TPS2114A			UNIT	
		MIN	TYP	MAX		
<b>REVERSE CONDUCTION BLOCKING</b>						
$\Delta V_{O(I\_block)}$	Minimum input-to-output voltage difference to block switching D0 = D1 = high, $V_{I(INx)} = 3.3\text{ V}$ Connect OUT to a 5-V supply through a series 1-k $\Omega$ resistor. Let D0 = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV	
<b>THERMAL SHUTDOWN</b>						
Thermal shutdown threshold	TPS211xA is in current limit	135			$^{\circ}\text{C}$	
Recovery from thermal shutdown	TPS211xA is in current limit	125			$^{\circ}\text{C}$	
Hysteresis		10			$^{\circ}\text{C}$	
<b>IN2-IN1 COMPARATORS</b>						
Hysteresis of IN2-IN1 comparator		0.1			0.2	V
Deglitch of IN2-IN1 comparator (both $\uparrow\downarrow$ )		10	20	50	$\mu\text{s}$	
<b>STAT OUTPUT</b>						
Leakage current	$V_{O(STAT)} = 5.5\text{ V}$	0.01			1	$\mu\text{A}$
Saturation voltage	$I_{I(STAT)} = 2\text{ mA}$ , IN1 switch is on	0.13			0.4	V
Deglitch time (falling edge only)		150			$\mu\text{s}$	

**SWITCHING CHARACTERISTICS**

Over recommended operating junction temperature range,  $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$ , and  $R_{ILIM} = 400\ \Omega$ , unless otherwise noted.

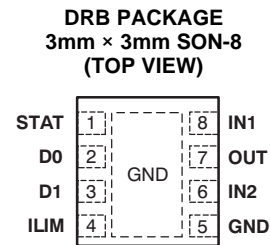
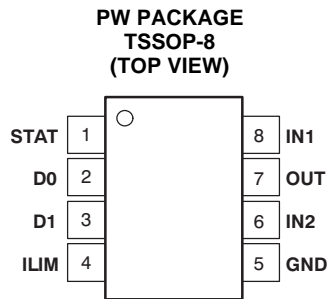
PARAMETER	TEST CONDITIONS	TPS2114A			TPS2115A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>POWER SWITCH</b>								
$t_r$	Output rise time from an enable $V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$ , $T_J = 25^{\circ}\text{C}$ , $C_L = 1\ \mu\text{F}$ , $I_L = 500\text{ mA}$ (see Figure 1a)	0.5	1.0	1.5	1	1.8	3	ms
$t_f$	Output fall time from a disable $V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$ , $T_J = 25^{\circ}\text{C}$ , $C_L = 1\ \mu\text{F}$ , $I_L = 500\text{ mA}$ (see Figure 1a)	0.35	0.5	0.7	0.5	1	2	ms
$t_t$	Transition time IN1 to IN2 transition, $V_{I(IN1)} = 3.3\text{ V}$ , $V_{I(IN2)} = 5\text{ V}$ , $T_J = 125^{\circ}\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ Measure transition time as 10–90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$ (see Figure 1b).	40			60	40	60	$\mu\text{s}$
	IN2 to IN1 transition, $V_{I(IN1)} = 5\text{ V}$ , $V_{I(IN2)} = 3.3\text{ V}$ , $T_J = 125^{\circ}\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ Measure transition time as 10–90% rise time or from 3.4 V to 4.8 V on $V_{O(OUT)}$ (see Figure 1b).	40			60	40	60	$\mu\text{s}$
$t_{PLH1}$	Turn-on propagation delay from enable $V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$ , measured from enable to 10% of $V_{O(OUT)}$ , $T_J = 25^{\circ}\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ (see Figure 1a)	0.5			1			ms
$t_{PHL1}$	Turn-off propagation delay from a disable $V_{I(IN1)} = V_{I(IN2)} = 5\text{ V}$ , measured from disable to 90% of $V_{O(OUT)}$ , $T_J = 25^{\circ}\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ (see Figure 1a)	3			5			ms
$t_{PLH2}$	Switch-over rising propagation delay Logic 1 to Logic 0 transition on D1, $V_{I(IN1)} = 1.5\text{ V}$ , $V_{I(IN2)} = 5\text{ V}$ , $V_{I(D0)} = 0\text{ V}$ , measured from D1 to 10% of $V_{O(OUT)}$ , $T_J = 25^{\circ}\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ (see Figure 1c)	40			100			$\mu\text{s}$
$t_{PHL2}$	Switch-over falling propagation delay Logic 0 to Logic 1 transition on D1, $V_{I(IN1)} = 1.5\text{ V}$ , $V_{I(IN2)} = 5\text{ V}$ , $V_{I(D0)} = 0\text{ V}$ , measured from D1 to 90% of $V_{O(OUT)}$ , $T_J = 25^{\circ}\text{C}$ , $C_L = 10\ \mu\text{F}$ , $I_L = 500\text{ mA}$ (see Figure 1c)	2	3	10	2	5	10	ms

**Table 1. Truth Table**

D1	D0	$V_{I(IN2)} > V_{I(IN1)}$	STAT	OUT <sup>(1)</sup>
0	0	X <sup>(2)</sup>	Hi-Z	IN2
0	1	No	0	IN1
0	1	Yes	Hi-Z	IN2
1	0	X	0	IN1
1	1	X	0	Hi-Z

- (1) The under-voltage lockout circuit causes the output OUT to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal  $V_{DD}$  UVLO.  
 (2) X = Don't care.

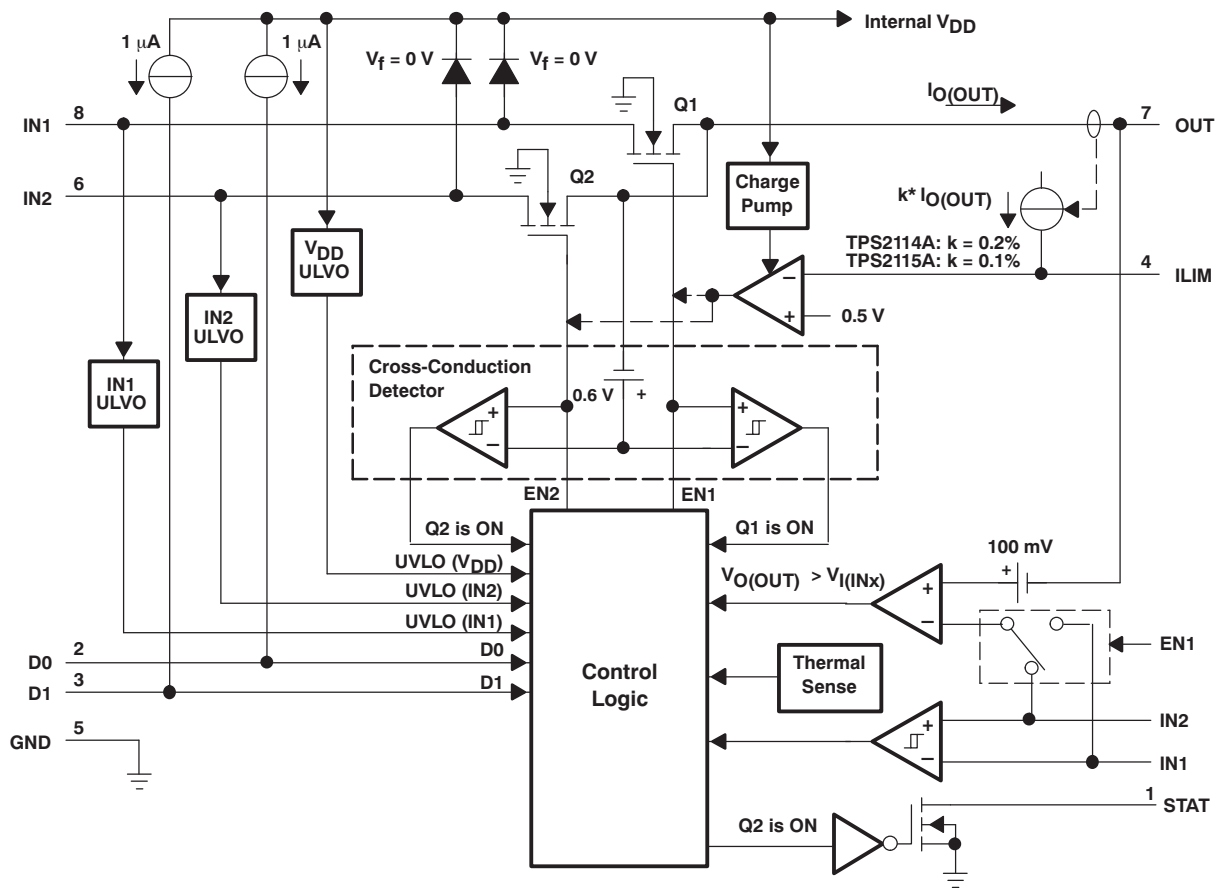
**PIN CONFIGURATIONS**



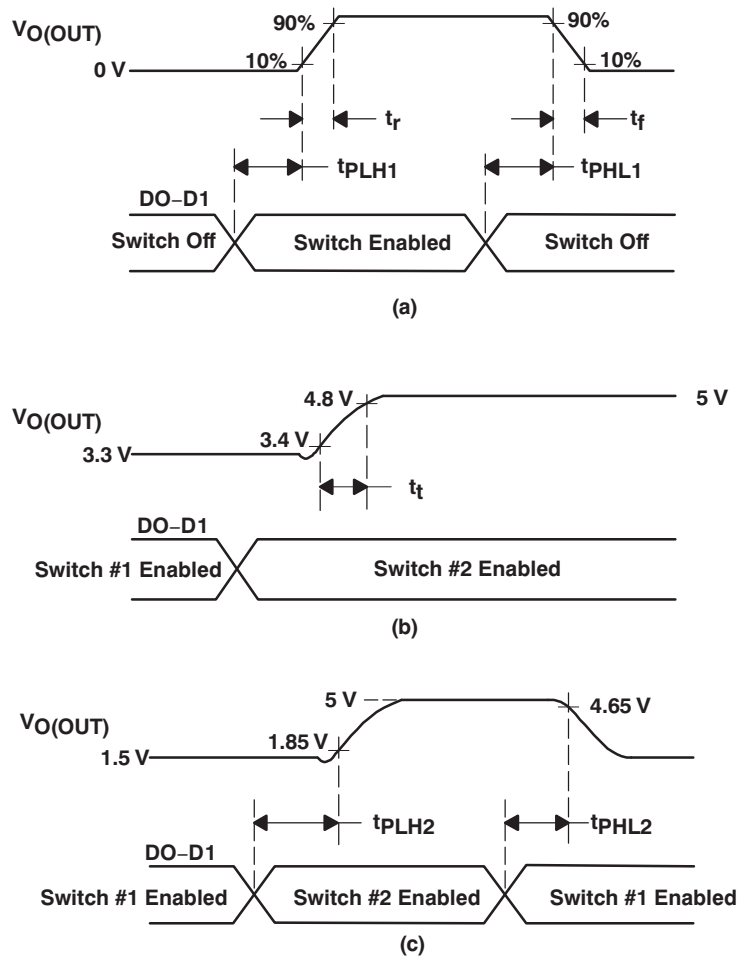
**TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
D0	2	I	TTL- and CMOS-compatible input pins. Each pin has a 1- $\mu$ A pull-up. <a href="#">Table 1</a> illustrates the functionality of D0 and D1.
D1	3	I	TTL- and CMOS-compatible input pins. Each pin has a 1- $\mu$ A pull-up. <a href="#">Table 1</a> illustrates the functionality of D0 and D1.
GND	5	I	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal $V_{DD}$ UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal $V_{DD}$ UVLO.
ILIM	4	I	A resistor $R_{ILIM}$ from ILIM to GND sets the current limit $I_L$ to $250/R_{ILIM}$ and $500/R_{ILIM}$ for the TPS2114A and TPS2115A, respectively.
OUT	7	O	Power switch output
STAT	1	O	STAT is an open-drain output that is Hi-Z if the IN2 switch is ON. STAT pulls low if the IN1 switch is ON or if OUT is Hi-Z (i.e., $\overline{EN}$ is equal to logic 0).
PAD	—	I	Tie to GND. Connect to internal planes for improved heatsinking with multiple vias.

FUNCTIONAL BLOCK DIAGRAM



**PARAMETER MEASUREMENT INFORMATION**

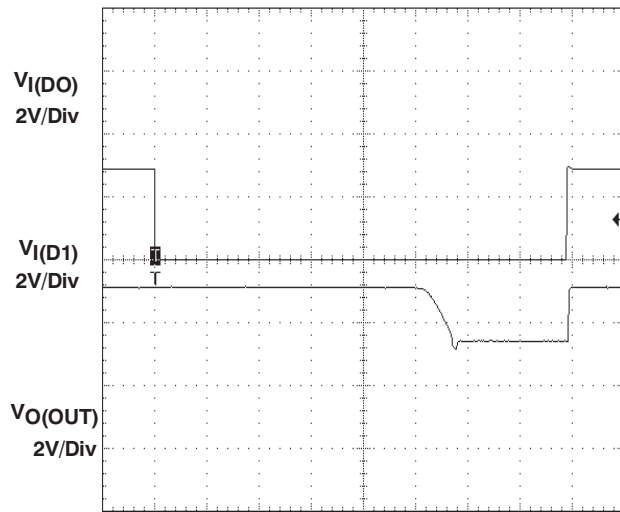


**Figure 1. Propagation Delays and Transition Timing Waveforms**

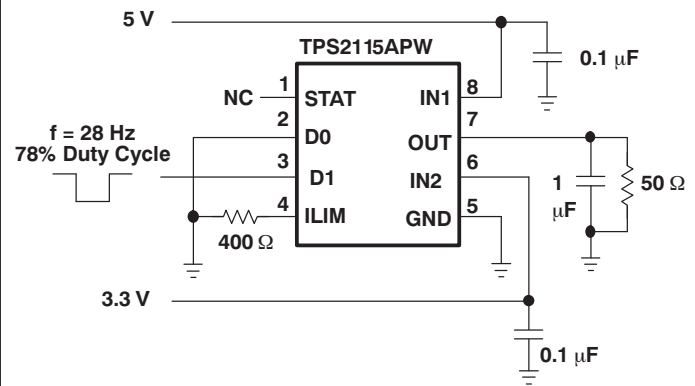


TYPICAL CHARACTERISTICS

OUTPUT SWITCHOVER RESPONSE



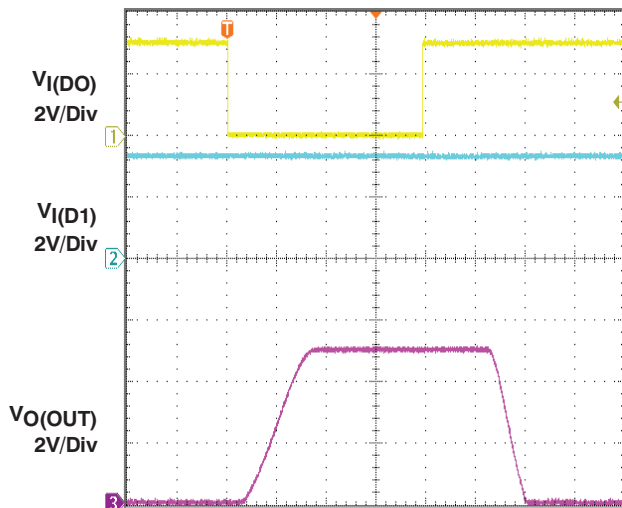
t – Time – 1 ms/div



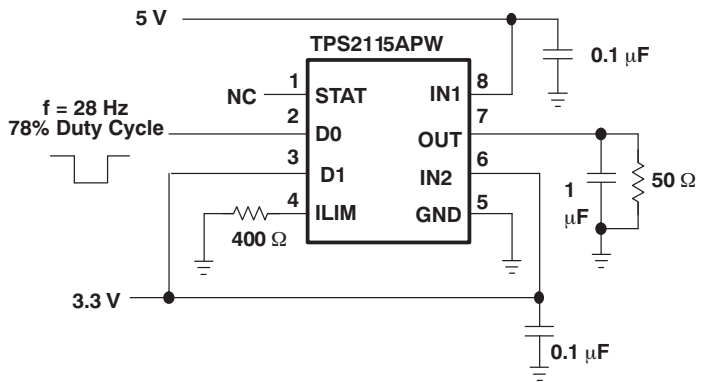
Output Switchover Response Test Circuit

Figure 2.

OUTPUT TURN-ON RESPONSE



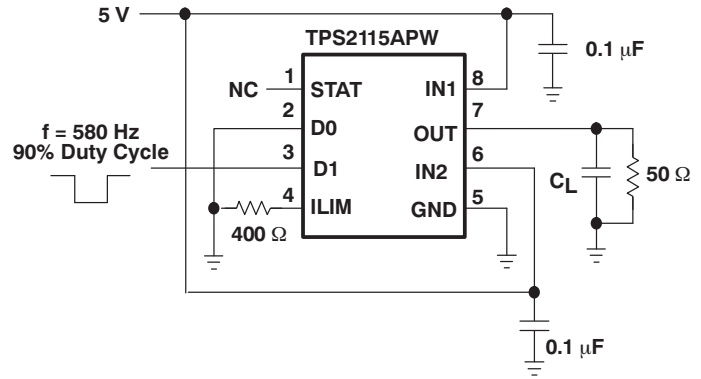
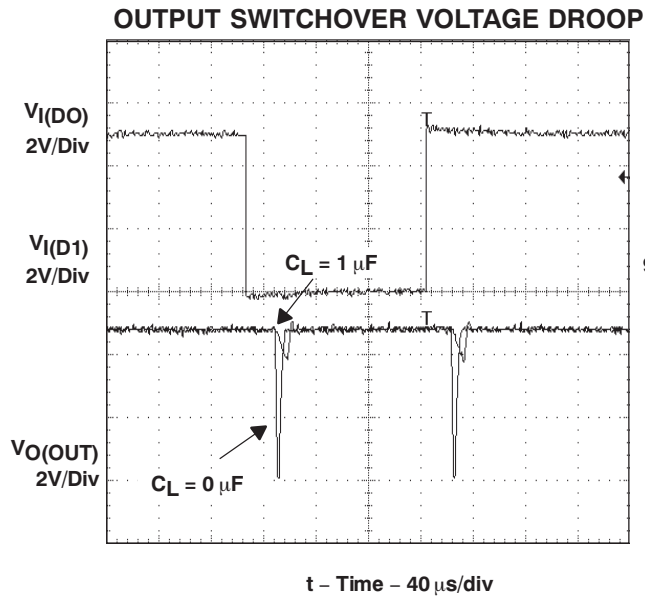
t – Time – 2 ms/div



Output Turn-On Response Test Circuit

Figure 3.

TYPICAL CHARACTERISTICS (continued)

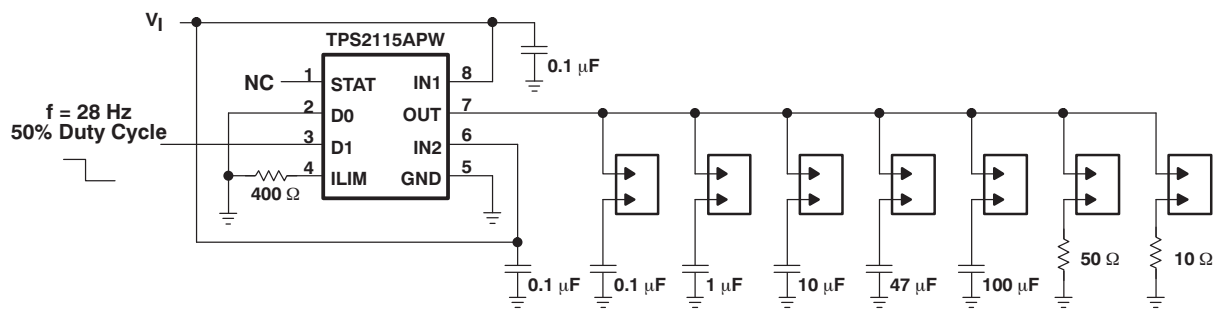
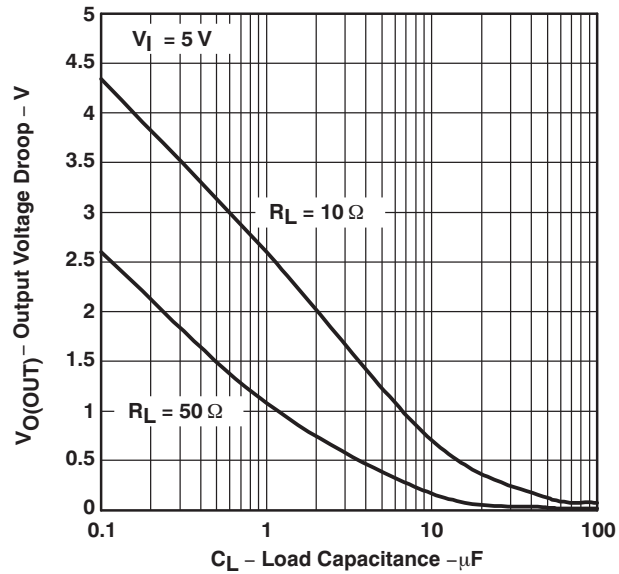


Output Switchover Voltage Droop Test Circuit

Figure 4.

TYPICAL CHARACTERISTICS (continued)

OUTPUT SWITCHOVER VOLTAGE DROOP  
VS  
LOAD CAPACITANCE

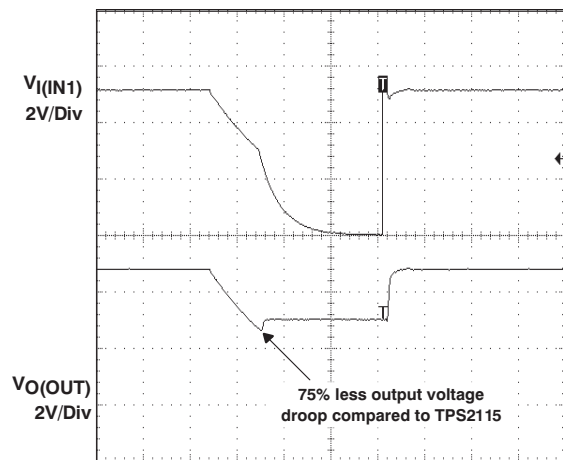


Output Switchover Voltage Droop Test Circuit

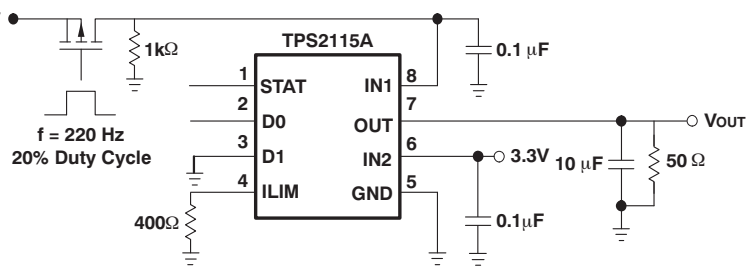
Figure 5.

TYPICAL CHARACTERISTICS (continued)

AUTO SWITCHOVER VOLTAGE DROOP



t – Time – 250  $\mu$ s/div

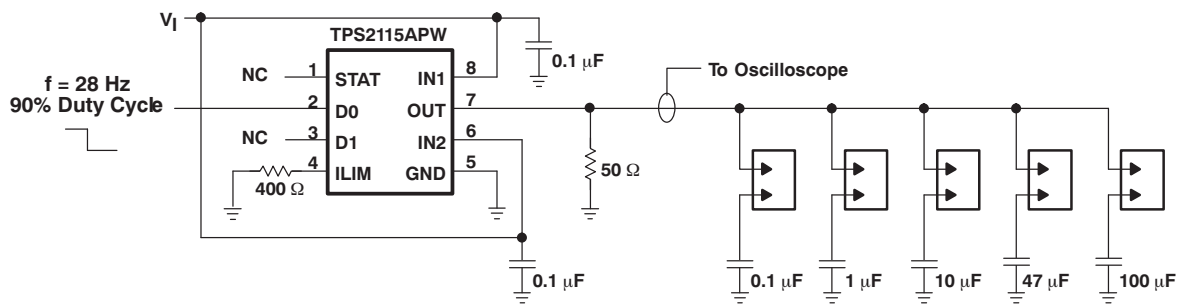
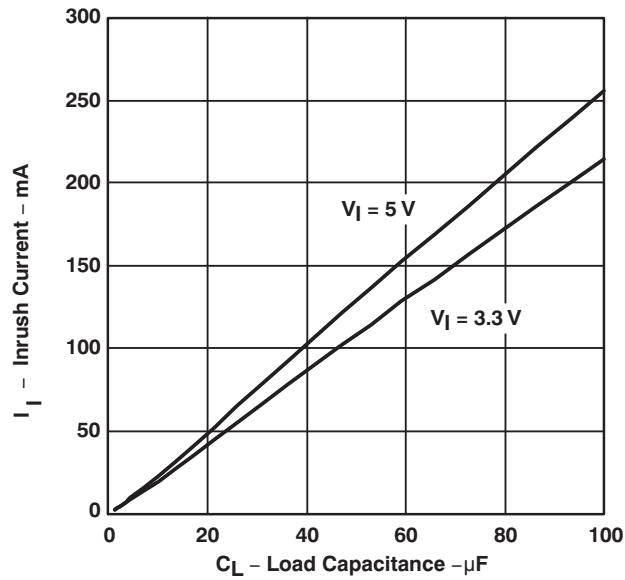


Auto Switchover Voltage Droop Test Circuit

Figure 6.

TYPICAL CHARACTERISTICS (continued)

INRUSH CURRENT  
VS  
LOAD CAPACITANCE



Output Capacitor Inrush Current Test Circuit

Figure 7.

TYPICAL CHARACTERISTICS (continued)

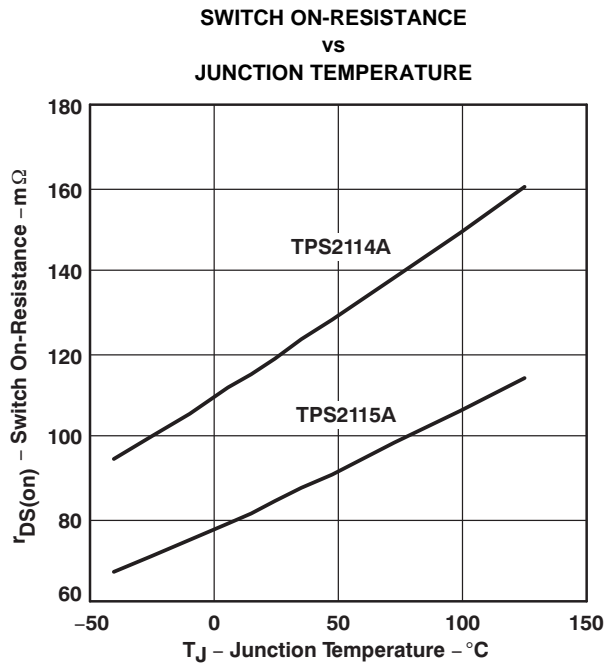


Figure 8.

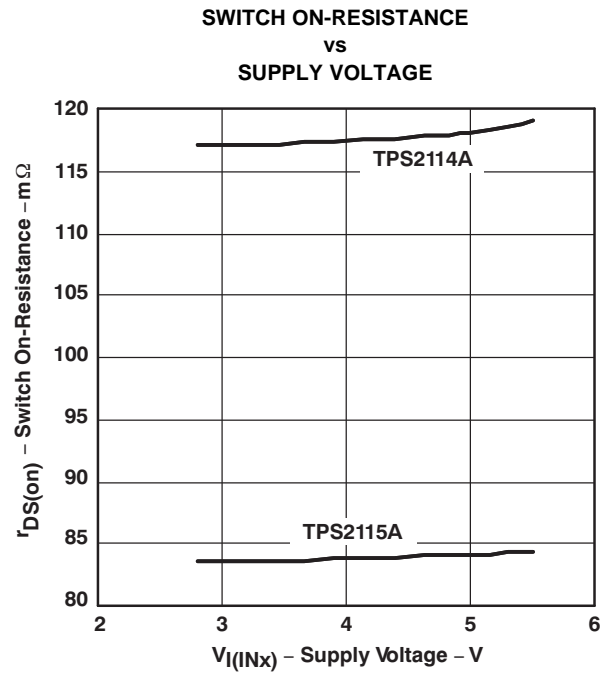


Figure 9.

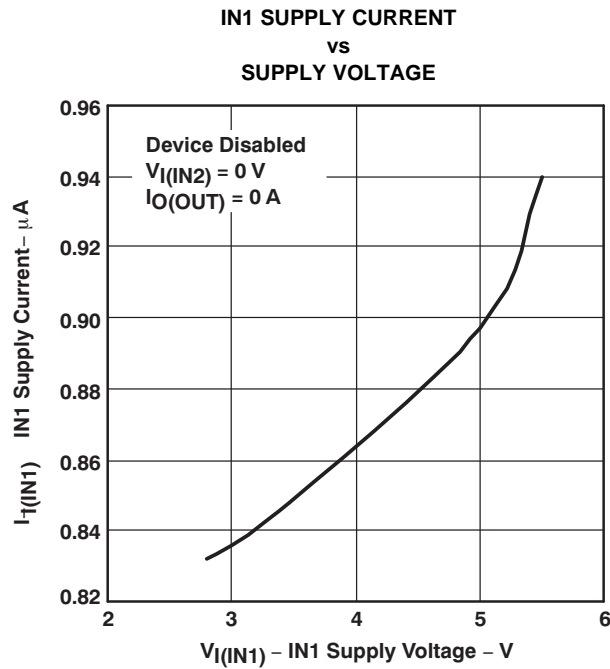


Figure 10.

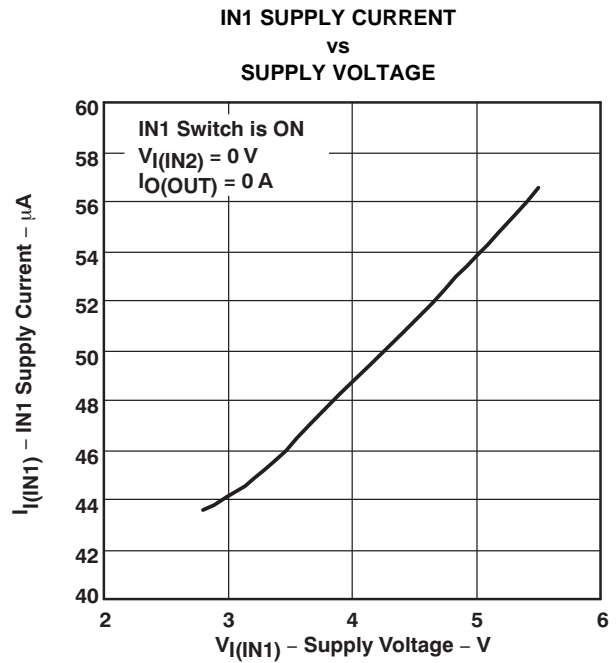


Figure 11.

TYPICAL CHARACTERISTICS (continued)

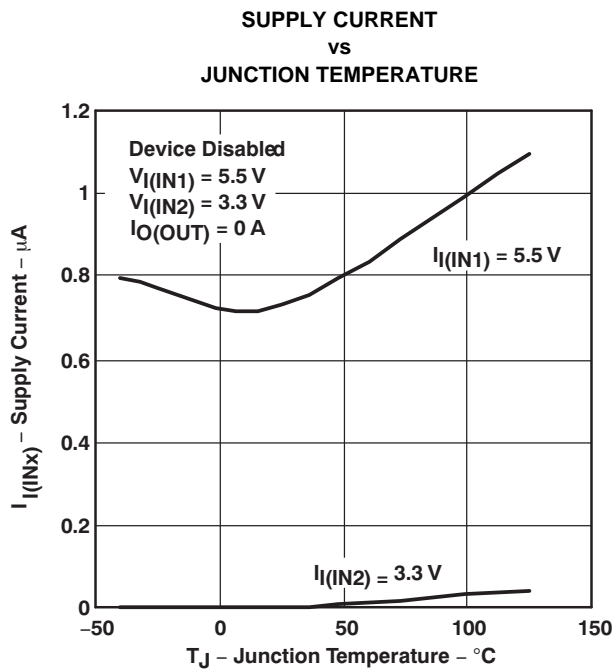


Figure 12.

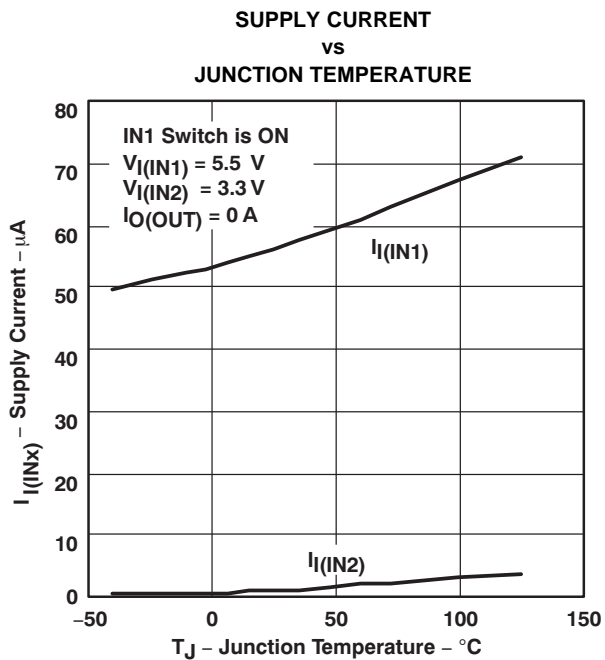


Figure 13.

### APPLICATION INFORMATION

Some applications have two energy sources, one of which should be used in preference to another. Figure 14 shows a circuit that will connect IN1 to OUT until the voltage at IN1 falls below a user-specified value. Once the voltage on IN1 falls below this value, the TPS2114A/5A will select the higher of the two supplies. This usually means that the TPS2114A/5A will swap to IN2.

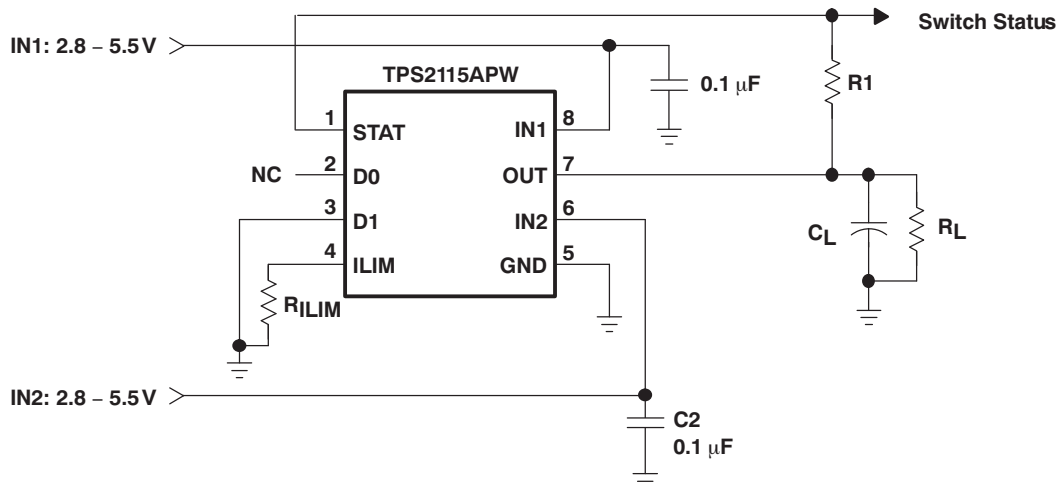


Figure 14. Auto-Selecting for a Dual Power Supply Application

In Figure 15, the multiplexer selects between two power supplies based upon the D1 logic signal. OUT connects to IN1 if D1 is logic 1; otherwise, OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.

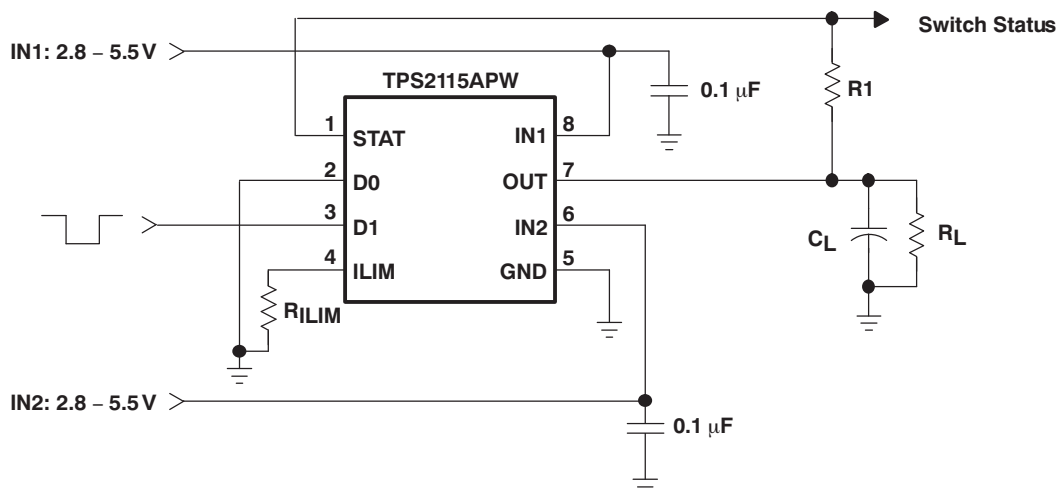


Figure 15. Manually Switching Power Sources



## DETAILED DESCRIPTION

### AUTO-SWITCHING MODE

D0 equal to logic 1 and D1 equal to logic 0 selects the auto-switching mode. In this mode, OUT connects to the higher of IN1 and IN2.

### MANUAL SWITCHING MODE

D0 equal to logic 0 selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic 1, otherwise OUT connects to IN2.

### N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

### CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches will never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

### REVERSE-CONDUCTION BLOCKING

When the TPS211xA switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211xA will not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it will remain connected regardless of output voltage.

### CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

### CURRENT LIMITING

A resistor  $R_{ILIM}$  from ILIM to GND sets the current limit to  $250/R_{ILIM}$  and  $500/R_{ILIM}$  for the TPS2114A and TPS2115A, respectively. Setting resistor  $R_{ILIM}$  equal to zero is not recommended as that disables current limiting.

### OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS2114A/5A slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see [Table 1](#)). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot-plugging a load such as a PCI card. The TPS2114A/5A slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (July 2006) to Revision E</b>	<b>Page</b>
• Updated document to current format .....	1
• Changed title, footnote, and CGF marking in Device Information table .....	2
• Deleted footnote 1 (not tested in production) from Electrical Characteristics: General table .....	4
• Deleted footnote 1 (not tested in production) from Switching Characteristics table .....	5
• Added PAD row to Terminal Functions table .....	6

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
TPS2114APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS2114APWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS2114APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS2114APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS2115ADRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2115ADRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2115ADRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2115ADRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TPS2115APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS2115APWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS2115APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	
TPS2115APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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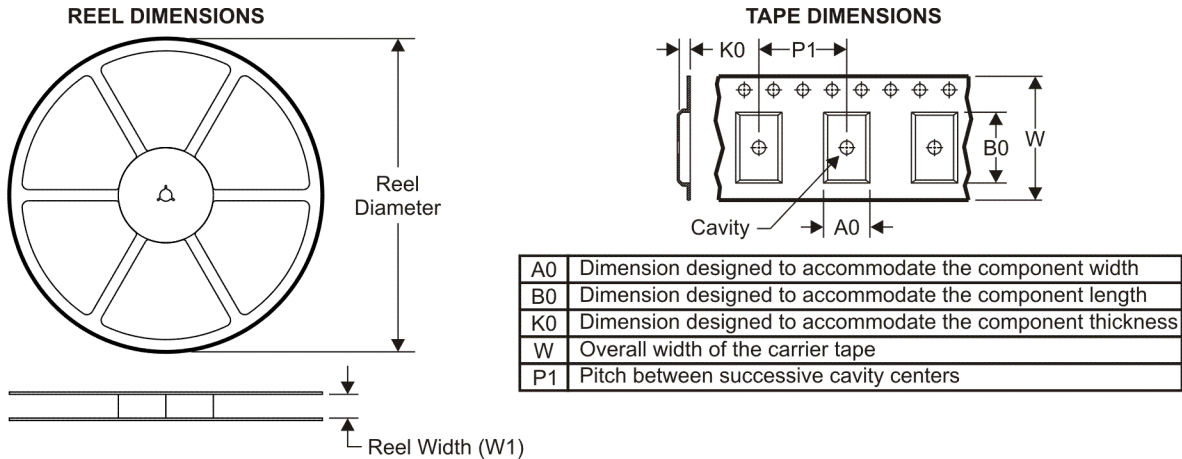
**OTHER QUALIFIED VERSIONS OF TPS2115A :**

- Automotive: [TPS2115A-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2114APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2115ADRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2115ADRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2115APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

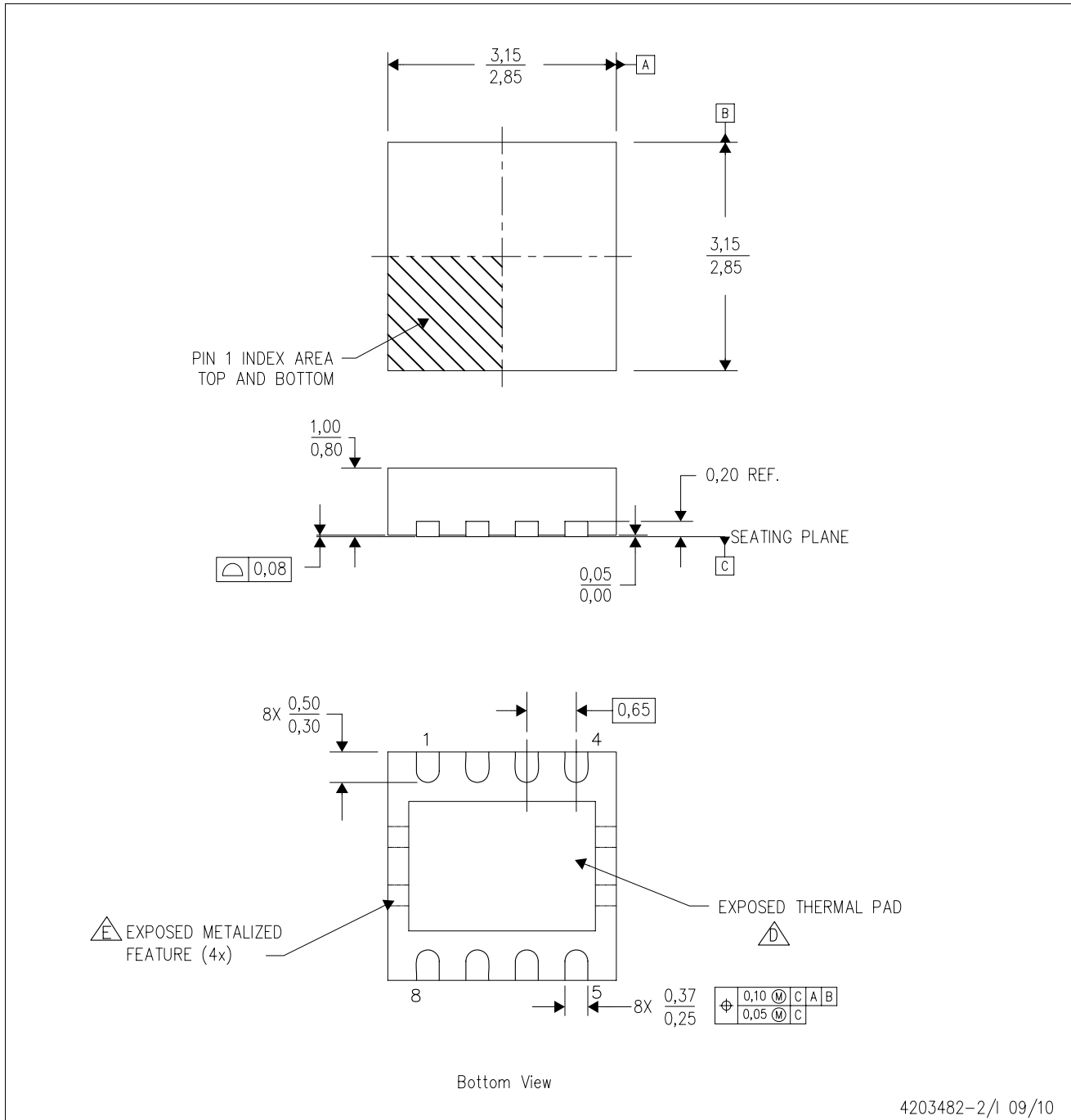
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2114APWR	TSSOP	PW	8	2000	346.0	346.0	29.0
TPS2115ADRBR	SON	DRB	8	3000	346.0	346.0	29.0
TPS2115ADRBT	SON	DRB	8	250	190.5	212.7	31.8
TPS2115APWR	TSSOP	PW	8	2000	346.0	346.0	29.0

DRB (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



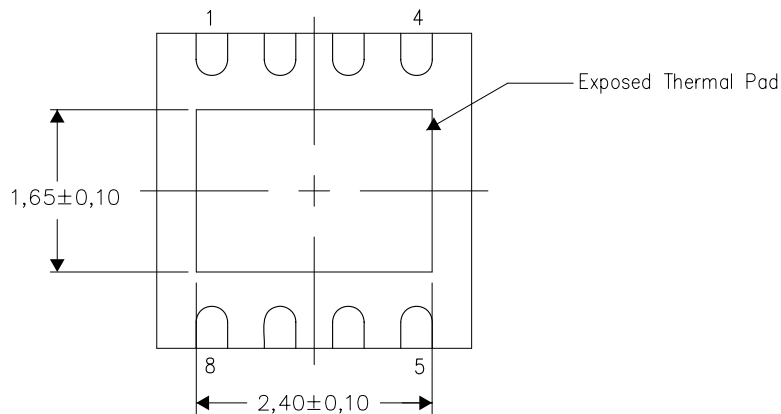
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Small Outline No-Lead (SON) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

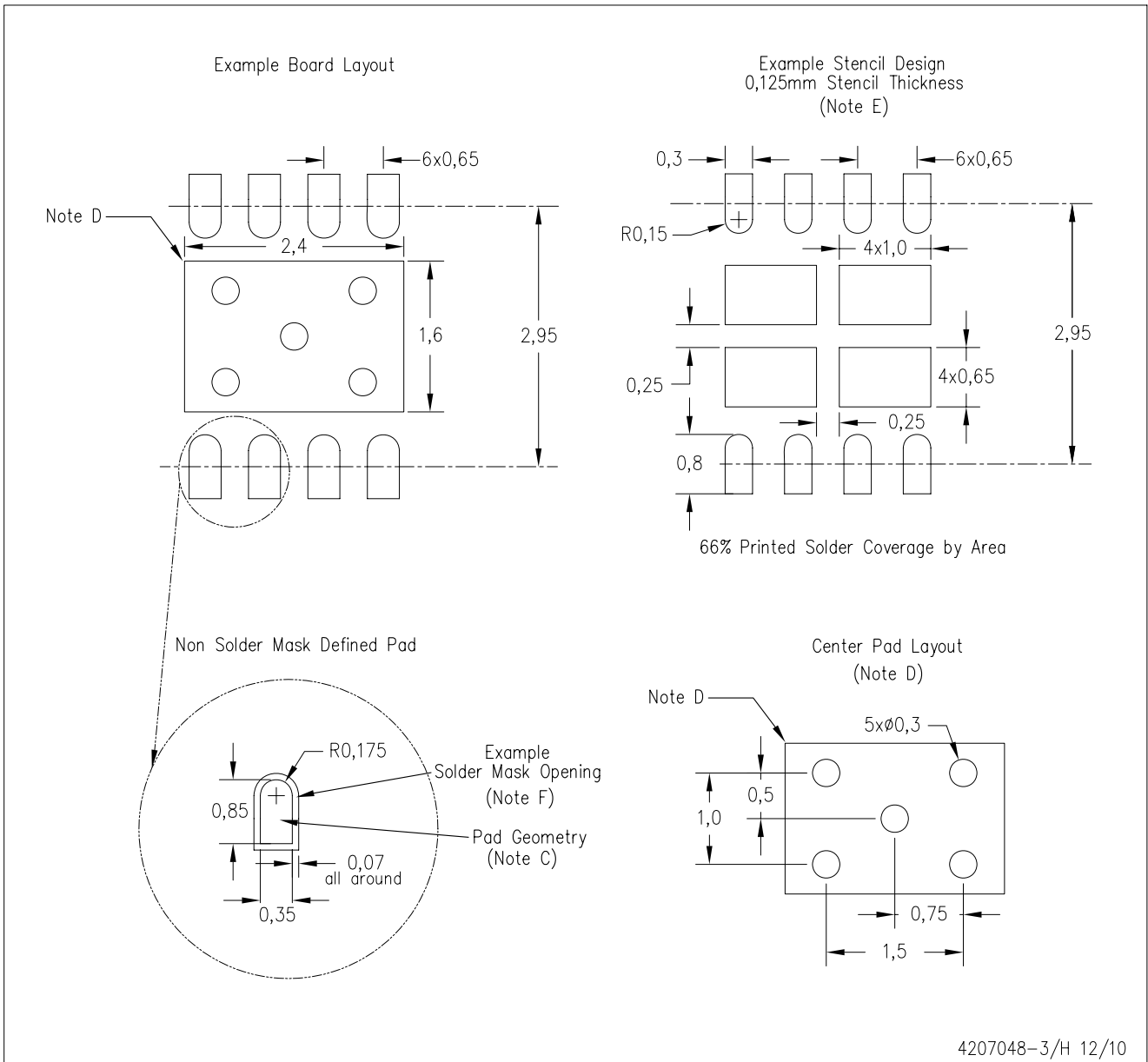
4206340-3/L 12/10

NOTE: A. All linear dimensions are in millimeters



DRB (S-PVSON-N8)

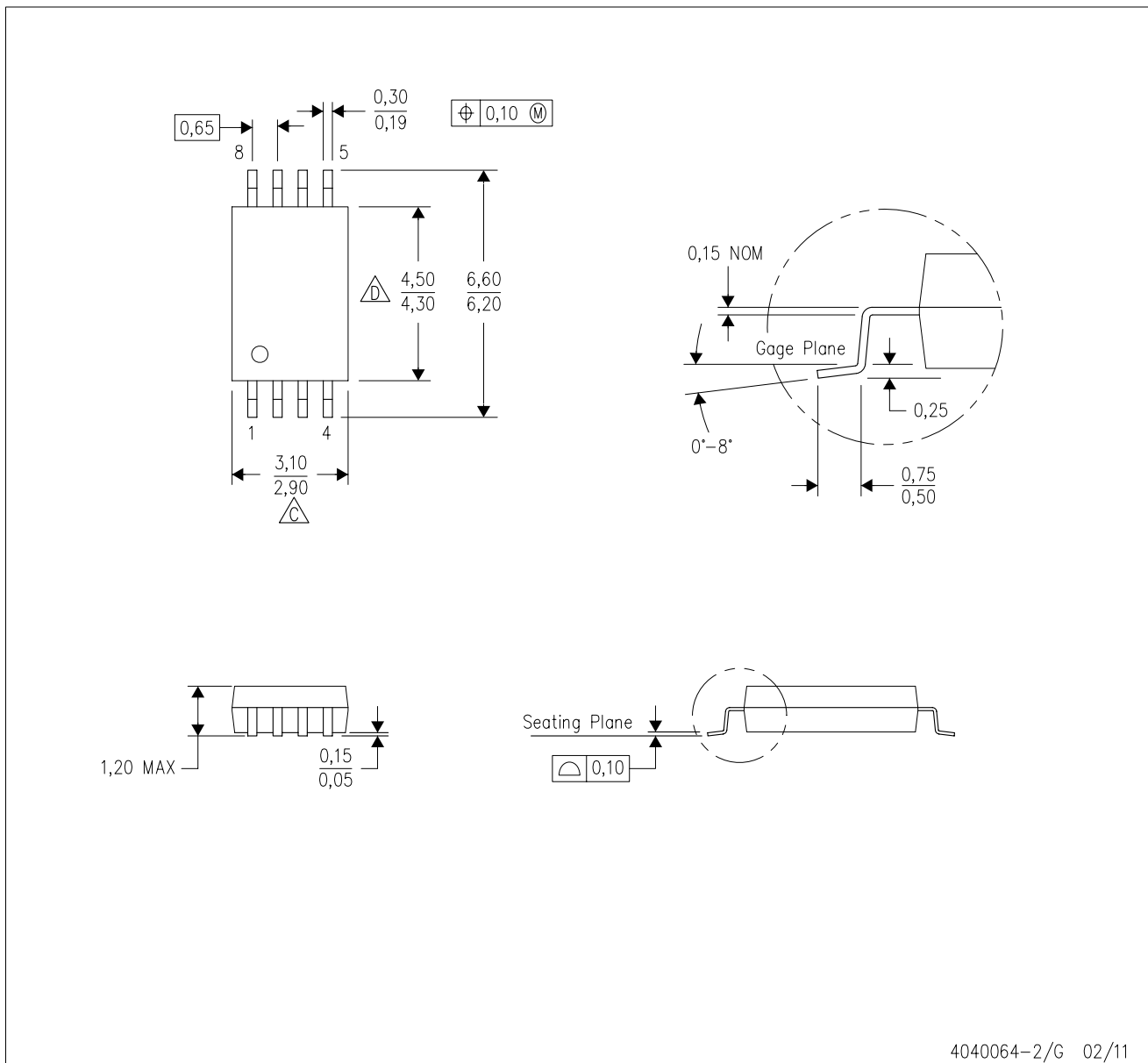
PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for solder mask tolerances.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

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