USB OTG Companion Device with V_{BUS} Over Voltage, Over Current Protection, and Four Channel ESD Clamps

Check for Samples: TPD4S214

FEATURES

- **Input Voltage Protection at V_{BUS} from –7 V to 30 V**
- **Low $R_{DS(ON)}$ N-CH FET Switch for High Efficiency**
- **Compliant with USB2.0 and USB3.0 OTG spec**
- **User Adjustable Current Limit From 250 mA to Beyond 1.2 A**
- **Built-in Soft-start**
- **Reverse Current Blocking**
- **Over Voltage Lock Out for V_{BUS}**
- **Under Voltage Lock Out for V_{OTG_IN}**
- **Thermal Shutdown and Short Circuit Protection**
- **Auto Retry on any Fault; no Latching off States**
- **Integrated V_{BUS} Detection Circuit**
- **Low Capacitance TVS ESD Clamp for USB2.0 High Speed Data Rate**
- **Internal 16ms Startup Delay**
- **ESD Performance D+, D-, ID, V_{BUS} PINS**
  - **±15-kV Contact Discharge (IEC 61000-4-2)**
  - **±15-kV Air Gap Discharge (IEC 61000-4-2)**
- **Space Saving WCSP (12-YFF) Package**

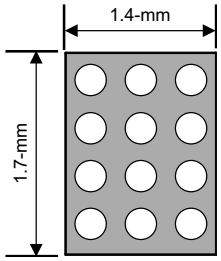
APPLICATIONS

- **Cell Phones**
- **Tablet, eBook**
- **Set-Top Box**
- **Portable Media Players**
- **Digital Camera**

YFF PACKAGE
(TOP SIDE/SEE-THROUGH VIEW)

12-YFF Pin Proposal

	1	2	3
A	V_{OTG_IN}	DET	VBUS
B	V_{OTG_IN}	FLT\	VBUS
C	EN	GND	ID
D	ADJ	D-	D+



PRODUCT PREVIEW

DESCRIPTION

The TPD4S214 is a single-chip protection solution for USB On-the-Go and other current limited USB applications. This device includes an integrated low ($R_{DS(ON)}$) N-channel current limited switch for OTG current supply to peripheral devices. TPD4S214 offers low capacitance TVS ESD clamps for the D+, D-, ID pins for both USB2.0 and USB3.0 applications. The VBUS pin can handle continuous voltage ranging from –7 V to 30 V. The over voltage lock-out (OVLO) at the VBUS pin ensures that if there is a fault condition at the V_{BUS} line, the TPD4S214 is able to isolate it and protects the internal circuitry from damage. Similarly, the under voltage lock out (UVLO) at the V_{OTG_IN} pin ensures that there is no power drain from the internal OTG supply to external V_{BUS} if V_{OTG_IN} droops below safe operating level.

When EN is high, the OTG switch is activated and the $\overline{FLT}$ pin indicates whether there is a fault condition. The soft start feature waits 16 ms to turn on the OTG switch after all operating conditions are met. The $\overline{FLT}$ pin asserts low during any one of the following fault conditions: OVLO ($V_{BUS} > V_{OVLO}$), UVLO condition ($V_{OTG\_IN} < V_{UVLO}$) over temperature, over current, short circuit condition, or reverse-current-condition ($V_{BUS} > V_{OTG\_IN}$). The OTG switch is turned off during any fault condition. Once the switch is turned off, the IC periodically rechecks the faults internally. If the IC returns to normal operating conditions, the switch turns back on and $\overline{FLT}$ is reset to high.

There is also a V_{BUS} detection feature for facilitating USB communication between USB host and peripheral device. See Table 2 for detection scheme. If this is not used, DET pin can be either floating or connected to ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	WCSP – YFF (0.4-mm pitch)	Tape and reel	TPD4S214YFFR	RD214

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

CIRCUIT SCHEMATIC DIAGRAM

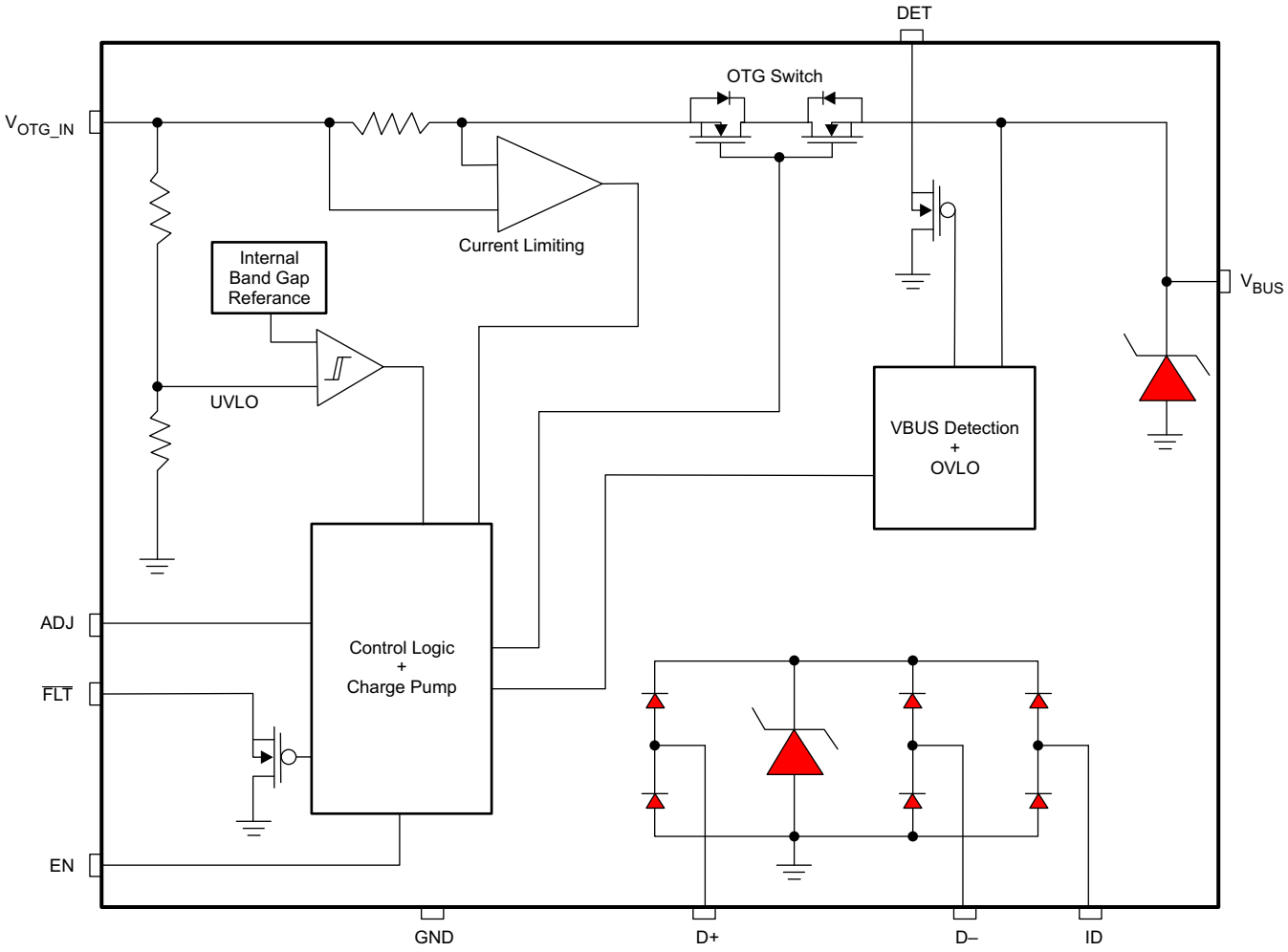


Figure 1. Circuit Schematic

PRODUCT PREVIEW

Table 1. Device Operation

EN	V_{OTG_IN}	V_{BUS}	OCP	OTP	OTG SW	$\overline{FLT}$	FAULT CONDITION
X	0	0	F	F	OFF	L	SW Disabled
X	X	X	X	T	OFF	L	Over Temperature
H	X	X	T	X	OFF	L	Over Current
H	$V_{OTG\_IN} > V_{UVLO}$	$V_{BUS} > V_{OTG\_IN}$	F	F	OFF	L	Reverse-current
H	X	$V_{BUS} > V_{OVLO}$	F	F	OFF	L	V_{BUS} over-voltage
H	$V_{OTG\_IN} < V_{UVLO}$	X	F	F	OFF	L	V_{OTG_IN} under-voltage
H	$V_{OTG\_IN} > V_{BUS}$ and $V_{OTG\_IN} > V_{UVLO}$	$V_{SHORT} < V_{BUS} < V_{OTG\_IN}$ and $V_{SHORT} < V_{BUS} < V_{OVLO}$	F	F	ON	H	Normal (SW Enabled)

Table 2. V_{BUS} Detection Scheme(1)

EN	VOTG_IN (V_{BUS} Detect Power)	V_{BUS}	DET	Condition
X	X	$3V < V_{BUS} < 5.3V$	H	V_{BUS} within V_{BUS_VALID}
X	X	$3V > V_{BUS}$ or $V_{BUS} > 5.3V$	L	V_{BUS} outside of V_{BUS_VALID}

(1) X = Don't Care, H = Signal High, and L = Signal Low

PIN FUNCTIONS

PIN				DESCRIPTION
NAME	YFF	DRC	TYPE	
D–	D2	TBD	I/O	USB data–
D+	D3	TBD	I/O	USB data+
ID	C3	TBD	I/O	USB ID signal
$\overline{FLT}$	B2	TBD	O	Open-Drain Output. Connect a pullup resistor from FLT\ to the supply voltage of the host system.
ADJ	D1	TBD	I	Attach external resistor to adjust the current limit
EN	C1	TBD	I	Enable Input. Drive EN high to enable the OTG switch.
V_{BUS}	A3, B3	TBD	O	USB Power Output
V_{OTG_IN}	A1, B1	TBD	I	USB OTG Supply Input
DET	A2	TBD	O	Open-Drain Output. Connect a pullup resistor from DET to the supply voltage of the host system.
GND	C2	Thermal Pad	Ground	Connect to PCB ground plane

PRODUCT PREVIEW

ABSOLUTE MAXIMUM RATINGS (1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{OTG_IN}, ADJ, EN	Input voltage		–0.5	7	V
V_{BUS}	Output voltage to USB connector		–7	30	
$\overline{FLT}$, DET	Output voltage		–0.5	7	
	Input clamp current	$V_I < 0$		-50	mA
	I_{OUT} Continuous current through $\overline{FLT}$ and DET output			10	mA
	I_{GND} Continuous current through GND			100	mA
	$T_{J(max)}$ maximum junction temperature		–65	150	°C
D+, D-, ID, V_{BUS} pins	IEC 61000-4-2 Contact Discharge			±20	kV
D+, D-, ID, V_{BUS} pins	IEC 61000-4-2 Air-gap Discharge			±20	kV
All pins	Human-Body Model			±2	kV
D+, D-, ID, V_{BUS} pins	Peak Pulse Current (tp = 8/20 µs)			5	A
D+, D-, ID, V_{BUS} pins	Peak Pulse Power (tp = 8/20 µs)			TBD	W

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
T_A	Operating free-air temperature		-40		85	°C
V_{IH}	High-level input voltage EN		1.2			V
V_{IL}	Low-level input voltage EN				0.4	V
t_{EN}	EN ramp rate for proper turn on	Valid ramp rate is between 10us and 100ms, rising and falling	0.01		100	ms
t_{UVLO_SLEW}	V_{OTG_IN} ramp rate for proper UVLO operation	Valid ramp rate is between 10us and 100ms, rising and falling	0.01		100	ms
t_{OVLO_SLEW}	V_{BUS} ramp rate for proper OVLO operation	Valid ramp rate is between 10us and 100ms, rising and falling	0.01		100	ms
$T_{A\_VBUS\_ATT}$	Time to detect V_{BUS} device attachment and turn on DET				200	ms

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRICS (1)			YFF	UNITS
θ_{JA}	Package thermal impedance	Package thermal impedance	89.1	°C/W

(1) The published θ_{JA} was modeled assuming a 76mm x 114mm PCB with 4 copper layers and the exposed land pad of the PCB has thermal vias connecting the exposed center pad of the package to an internal GND plane for maximum heat dissipation. For more information about traditional and new thermal metrics, see the IC Package Metrics application report, SPRA953A.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS FOR EN, $\overline{FLT}$, DET, D+, D–, ID Pins

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IL_EN}	EN pin input leakage current	EN = 3.3 V			1	µA
I_{OL}	FLT\, DET pin output leakage current	$\overline{FLT}$, DET = 3.6 V			1	µA
V_{OL_FLT}	Low-level output voltage FLT\	V_{BUS} or V_{OTG_IN} = 5 V or 0 V I_{OL} = 100 µA			100	mV
V_{OL_DET}	Low-level output voltage DET	V_{BUS} and V_{OTG_IN} = 5 V or 0 V I_{OL} = 100 µA			100	mV
C_{EN}	Enable capacitance	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V_{OTG_IN} = 5 V		2	2.5	pF
V_D	Diode forward voltage D+, D–, ID pins; lower clamp diode	I_O = 8 mA			0.95	V
I_{L_D}	Leakage current on D+, D–, ID Pins	D+, D–, ID = 3.3 V			100	nA
ΔC_{IO}	Differential capacitance between the D+, D– lines	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V_{OTG_IN} = 5 V			0.05	pF
C_{IO}	Capacitance to GND for the D+, D–, ID lines	V_{BIAS} = 1.8 V, f = 1 MHz, 30 mVpp ripple, V_{OTG_IN} = 5 V		2.1		pF
V_{BR}	Breakdown voltage D+, D–, ID pins	I_{br} = 1 mA	8	TBD		V
	Breakdown voltage on Vbus	I_{br} = 1 mA	43			V
R_{DYN}	Dynamic on resistance D+, D–, ID clamps			1		Ω

ELECTRICAL CHARACTERISTICS FOR UVLO / OVLO

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input Under voltage Lockout					
V_{UVLO+}	Under-voltage lock-out, input power detected threshold rising	V_{OTG_IN} increasing from 0 V to 5 V, No load on V_{BUS} pin	3.4	3.6	3.8	V
$V_{UVLO–}$	Under-voltage lock-out, input power detected threshold falling	V_{OTG_IN} decreasing from 5 V to 0 V, No load on V_{BUS} pin	3.0	3.2	3.5	V
$V_{HYS-UVLO}$	Hysteresis on UVLO	Δ of V_{UVLO+} and $V_{UVLO–}$	150	260	550	mV
T_{RUVLO}	Recovery time from UVLO	V_{OTG_IN} increasing from 0V to 5V, No load on V_{BUS} pin; time from V_{OTG_IN} = V_{UVLO+} to $\overline{FLT}$ toggles high		16		ms
T_{RESP_UVLO}	Response time for UVLO	V_{OTG_IN} decreasing from 5V to 0V, No load on V_{BUS} pin; time from V_{OTG_IN} = $V_{UVLO–}$ to FLT\ toggles low		0.25		µs
OUTPUT OVERVOLTAGE LOCKOUT						
V_{OVP+}	OVLO rising threshold	Both V_{OTG_IN} and V_{BUS} increasing from 5 V to 7 V	5.55	6.15	6.45	V
$V_{OVP–}$	OVLO falling threshold	Both V_{OTG_IN} and V_{BUS} decreasing from 7 V to 5 V	5.4	6	6.3	V
$V_{HYS-OVP}$	Hysteresis on OVLO	Δ of V_{UVLO+} and $V_{UVLO–}$	25	100	275	mV
T_{ROVLO}	Recovery time from OVLO	Both V_{OTG_IN} and V_{BUS} decreasing from 7 V to 5 V, V_{OTG_IN} = 5 V; time from V_{BUS} = $V_{OVP–}$ to $\overline{FLT}$ toggles high		8		ms
T_{RESP_OVLO}	Response time for OVLO	Both V_{OTG_IN} and V_{BUS} increasing from 5 V to 7 V, V_{OTG_IN} = 5 V; time from V_{BUS} = V_{OVP+} to $\overline{FLT}$ toggles low		14		µs

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS FOR DET CIRCUITS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS_VALID-}	Valid V_{BUS} voltage detect	V_{BUS} = 7 V to 0 V	2.8	2.9	3	V
V_{BUS_VALID+}	Valid V_{BUS} voltage detect	V_{BUS} = 0 V to 7 V	5.3	5.4	5.45	V
T_{DET_DELAY-}	VBUS detect propagation delay–	VBUS 0 V to 4 V, 200 ns ramp; VBUS = $V_{BUS\_VALID-\ MIN}$ to DET toggles high			2	µs
T_{DET_DELAY+}	VBUS detect propagation delay+	VBUS 6 V to 4 V, 200 ns ramp; VBUS = $V_{BUS\_VALID+\ MAX}$ to DET toggles high			2.5	µs

ELECTRICAL CHARACTERISTICS FOR OTG SWITCH

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{DS_ON}	OTG switch resistance	V_{BUS} = 5 V, IOUT = 500 mA, R_{ADJ} = 75 kΩ			126	220	mΩ
V_{DROP}	OTG switch voltage drop	V_{BUS} = 5 V, IOUT = 500 mA, R_{ADJ} = 75 kΩ			70	105	mV
$I_{OTG\_OFF\_30V}$	Leakage current at 30V	Measured at V_{OTG_IN}	V_{BUS} = 30 V, EN = 0 V, V_{OTG_IN} = 5 V		82		µA
			V_{BUS} = 30 V, EN = 0 V, V_{OTG_IN} = 0 V		135		µA
$I_{OTG\_OFF\_2V}$	Leakage current at–2V		V_{BUS} = -2 V, EN = 0 V, V_{OTG_IN} = 5 V		30		µA
I_{OTG_OFF}	Standby Leakage current		V_{BUS} = 0 V, EN = 0 V, V_{OTG_IN} = 5 V		35		µA
			V_{BUS} = 5 V, EN = 0 V, V_{OTG_IN} = 0 V		4		µA
I_{BUS_REV}	Reverse Leakage current		V_{BUS} = 5 V, EN = 5 V, VOTG_IN=0V		15		µA
			V_{BUS} = 5 V, EN = 5 V, V_{OTG_IN} = 5.5 V		6		µA
T_{ON}	Turn-ON time	RL = 100 Ω, CL = 1 uF, RADJ = 75 kΩ			16		ms
T_{OFF}	Turn-OFF time	RL = 100 Ω, CL = 1 uF, RADJ = 75 kΩ			1		ms
T_{RISE}	Output rise time	RL = 100 Ω, CL = 1 uF, RADJ = 75 kΩ			1		ms
T_{FALL}	Output fall time	RL = 100 Ω, CL = 1 uF, RADJ = 75 kΩ			0.2		ms

ELECTRICAL CHARACTERISTICS FOR CURRENT LIMIT and SHORT CIRCUIT PROTECTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{OCP}	Current−limit threshold (maximum DC output current IOUT delivered to load)	V_{OTG_IN} = 5 V	R_{ADJ} = 226 kΩ (1)	235	250	265	mA
			R_{ADJ} = 75 kΩ (1)	700	750	795	
			R_{ADJ} = 61.9 kΩ (1)	846	900	955	
T_{BLANK}	Blanking time after enable	V_{OTG_IN} = 5 V	RL = 1 Ω, CL = 1 uF, RADJ = 75 kΩ		4		ms
T_{DEGL}	Deglitch time while enabled	V_{OTG_IN} = 5 V, RL = 100 Ω, CL = 1 uF, RADJ = 75 kΩ, apply short to ground			1		ms
T_{DET_SC}	Response time to short circuit				10		µs
T_{REG}	Short circuit regulation time		Hiccup pulse width; auto-retry time	10	12	14	ms
T_{OCP}	Short circuit over current protection time		Hiccup pulse period		144		ms
V_{SHORT}	Short circuit threshold				4		V
I_{INRUSH}	Inrush current during a startup	See Figure 5 under test configuration	RL = 100 Ω, CL = 22 µF, RADJ = 75 kΩ		750		mA

(1) External resistor tolerance is ±1%

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS FOR REVERSE VOLTAGE PROTECTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{REV}	Reverse-voltage comparator trip point (at V_{BUS} port)	$V_{BUS} > V_{OTG\_IN}$		50		mV
T_{RRVP}	Time from reverse-voltage condition to MOSFET switch off and $\overline{FLG}$ = low			16		ms
T_{RREV}	Re-arming time			25		ms

SUPPLY CURRENT CONSUMPTION

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		TYP	MAX	UNIT
$I_{VOTG\_IN}ON$	High-level V_{OTG_IN} operating current consumption	V_{OTG_IN} = 5 V, No load on V_{BUS}, EN = 5 V	RADJ = 75 kΩ		160	µA
			RADJ = 226 kΩ		150	µA

THERMAL SHUTDOWN

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	MAX	UNIT
T_{SHDN+}	Shutdown temp rising		150		°C
$T_{SHDN–}$	Shutdown temp falling		130		°C
T_{HYST}	Thermal-shutdown Hysteresis		20		°C
P_{MAX}	Maximum power dissipation	V_{OTG_IN} = 5 V, R_{load} = 5 Ω, EN = 5 V, R_{ADJ} = 75 KΩ		0.16	W
T_{JMAX}	Junction Temp at max power dissipation			150	°C

APPLICATION DIAGRAM

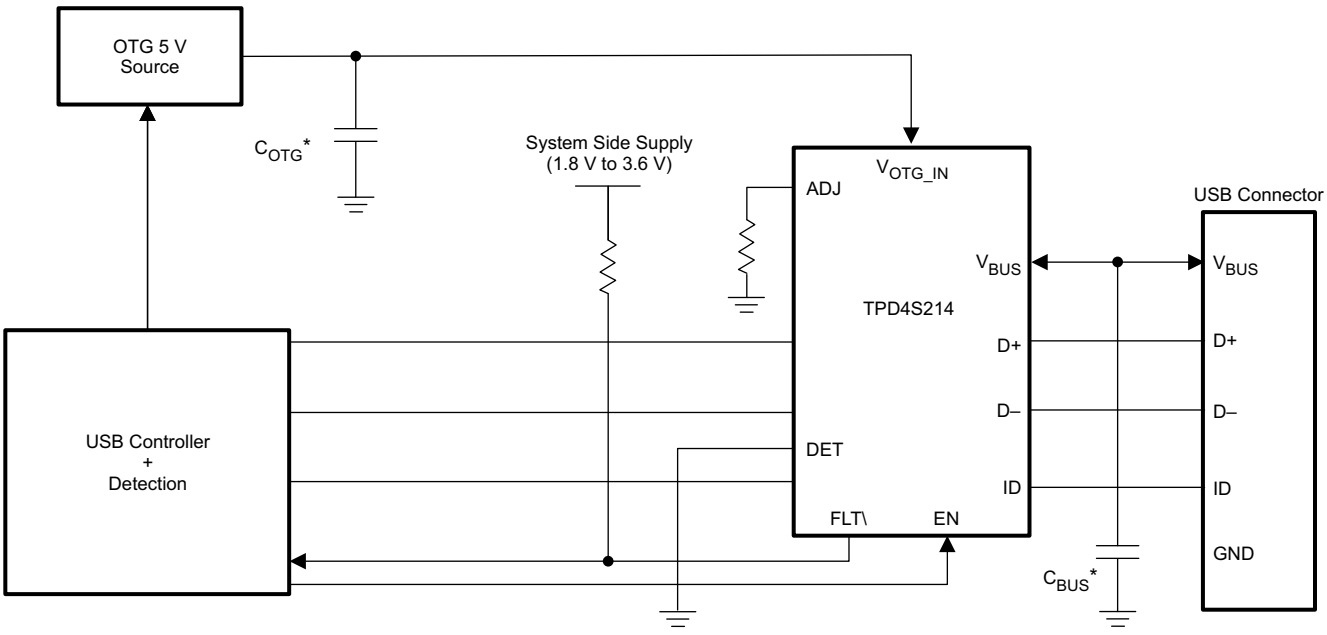


Figure 2. USB2.0 Application Diagram Without Using On-chip V_{BUS} Detect

PRODUCT PREVIEW

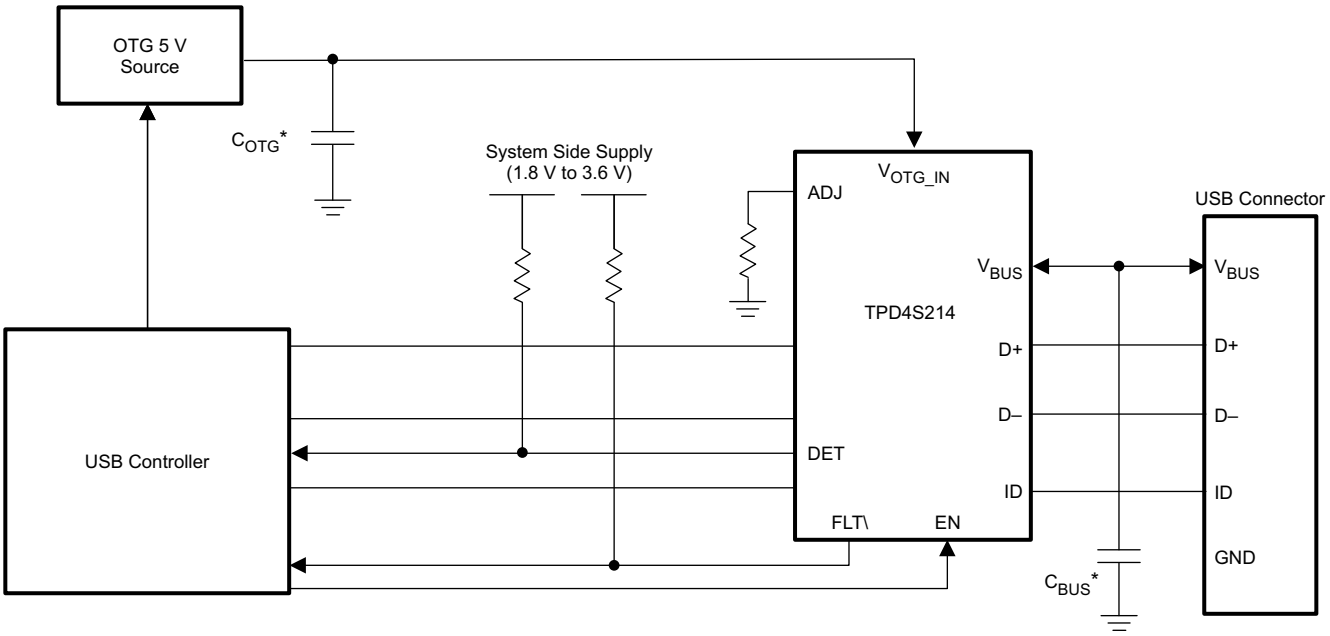
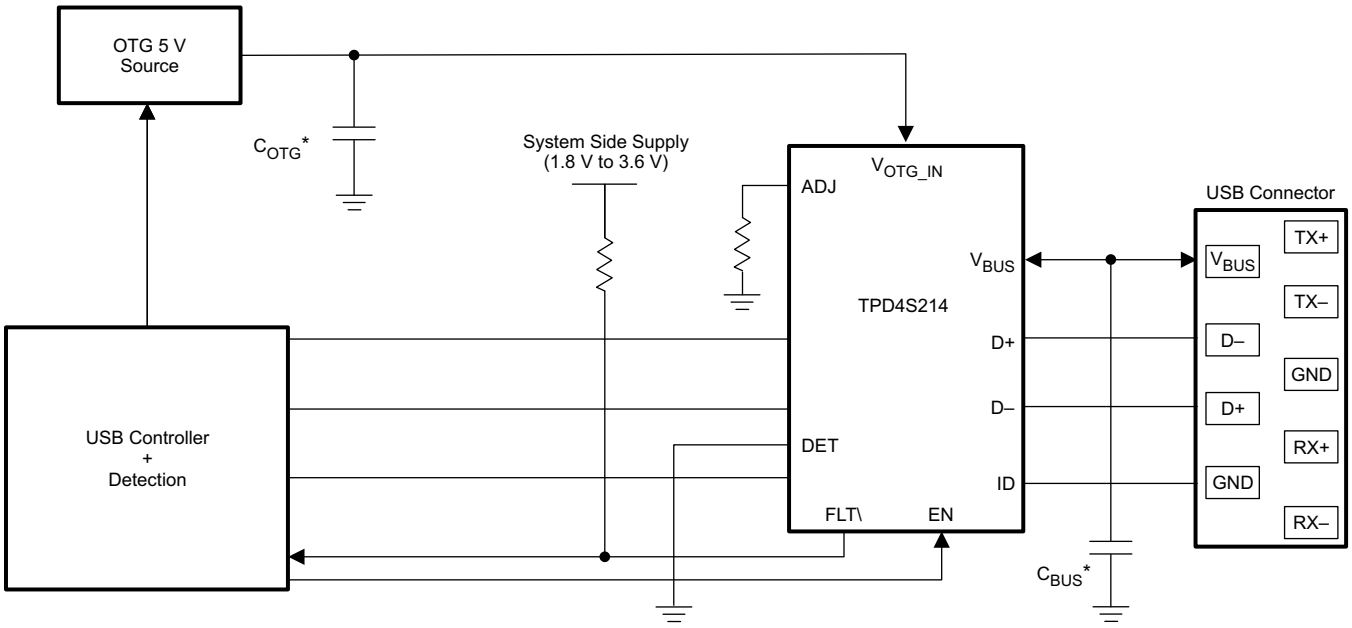


Figure 3. USB 2.0 Application Diagram Using On-chip V_{BUS} Detect



*C_{BUS} and C_{OTG} have minimum recommended values of 1 µF each

Figure 4. USB 3.0 Application Diagram Without Using On-chip V_{BUS} Detect

PRODUCT PREVIEW

TEST CONFIGURATION

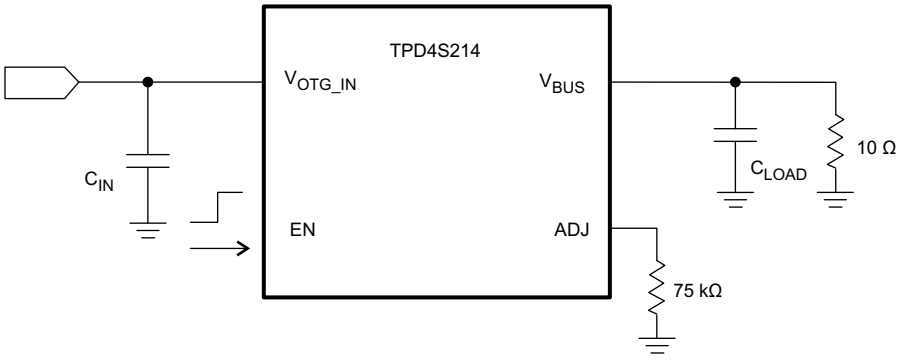


Figure 5. Inrush Current Test Configuration.

Enable is toggled from low to high. See the Application Information section for C_{IN} and C_{LOAD} value recommendations.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS

Figure 6.

Figure 7.

Figure 8.

Figure 9.

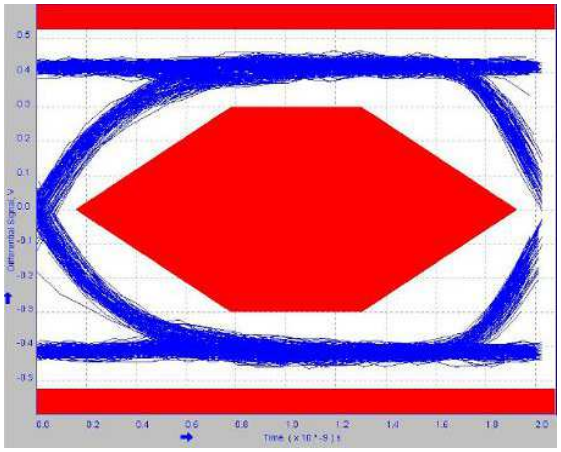


Figure 10.

Figure 11. Eye Diagram with no EVM and no IC, Full USB2.0 Speed at 480 Mbps

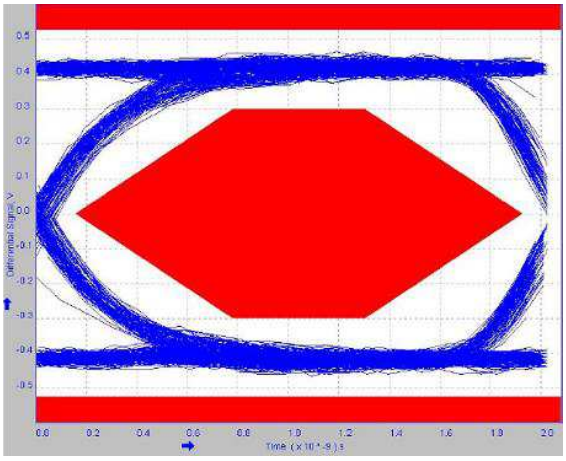


Figure 12. Eye Diagram with TPD4S214EVM but no IC, Full USB2.0 Speed at 480 Mbps

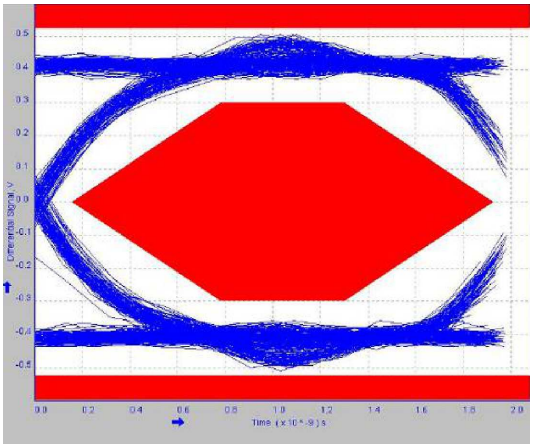


Figure 13. Eye Diagram with TPD4S214EVM and IC, Full USB2.0 Speed at 480 Mbps

APPLICATION INFORMATION

A USB OTG device's one and only connector is the AB receptacle, which accepts either an A or B plug. When an A-plug is inserted, the OTG device is called the A-device and when a B-plug is inserted it is called the B-device. A-device is often times referred to as "Targeted Host" and B-device as "USB peripheral". TPD4S214 supports an OTG device when TPD4S214's system is acting as an A-device and powering the USB interface. The TPD4S214 may also be used in non-OTG applications where it resides on the current source side.

Inrush Current Protection

As soon as TPD4S214 is enabled, its logic block detects the presence of any fault conditions highlighted in Table 1. In the absence of any fault condition, a counter waits for 16 ms, after which a trickle charge of 1 µA slowly turns on the main switch. During the inrush period, the peak inrush current will be limited to no more than the current limit set by the external resistor R_{ADJ}.

INPUT CAPACITOR (OPTIONAL)

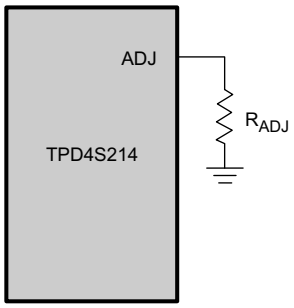
To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between V_{OTG_IN} and GND. A 10-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

OUTPUT CAPACITOR (OPTIONAL)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_{LOAD} is highly recommended. A C_{LOAD} greater than C_{IN} can cause V_{BUS} to exceed V_{OTG_IN} when the system supply is removed. A C_{IN} to C_{LOAD} ratio of 10 to 1 is recommended for minimizing V_{OTG_IN} dip caused by inrush currents during startup.

Current Limit

The TPD4S214 provides current limiting function, which is set by an external resistor connected from the ADJ pin to ground shown in Figure 14. The current limiting threshold I_{OCP} is set by the external resistor R_{ADJ}. Figure 11 shows the minimum, typical, and maximum current limit for a corresponding R_{ADJ} value. Figure 11 is used to determine R_{ADJ} needed to set a minimum I_{OCP}. Figure 12 shows the approximate percentage error from the typical I_{OCP} value to the min and max I_{OCP} values.



$$R_{ADJ} = \frac{55k\Omega \times Amps}{I_{OCP}} \quad (1)$$

Where:

R_{ADJ} = external resistor used to set the current limit
I_{OCP} = current limit set by the external R_{ADJ} resistor

R_{ADJ} is placed between the ADJ pin and ground, shown in the figure above, providing a minimum current limit between 250 mA and 1.2 A.

Figure 14. I_{OCP} versus R_{ADJ}

Figure 15. I_{OCP} Percentage Error versus R_{ADJ}

PRODUCT PREVIEW

V_{BUS} Detection

There are several important protocols defined in [OTG and EH Supplement] that governs communication between Targeted Hosts (A-device) and USB peripherals (B-device). Communication between host and peripheral is usually done on the ID pin only. In case when two OTG devices that could both act as either host or peripheral are connected, measuring voltage level on V_{BUS} will aid in the handshaking process. If an embedded host instead of a USB device is connected to the OTG device, OTG charging would not be required and the system's OTG source should remain off to conserve power. The TPD4S214 V_{BUS} detection block aids power conservation and is powered from V_{BUS}. See figure 3. The DET pin is an open drain PMOS output with default state low.

In the event when an A-plug is attached, the system detects ID pin as FALSE, in which case ID pin resistance to ground is less than 10 Ω. For a B-plug, the system detects ID pin as TRUE and ID pin resistance to ground is greater than 100 kΩ. For the system to power a USB device through OTG switch once it is connected, voltage on V_{BUS} should remain below $V_{BUS\_VALID\ MIN}$ within $T_{A\_VBUS\_ATT}$ of the ID pin becoming FALSE. After this event, the system confirms that the USB device requires power and enables both TPD4S214 and OTG source. However, if V_{BUS_VALID} is detected on V_{BUS} within $T_{A\_VBUS\_ATT}$ of the ID pin becoming FALSE, there is either a system error or the device connected does not require charging. OTG source remains switched off and the entire sequence would restart when the system detects another FALSE on the ID pin.

Table 3. V_{BUS} Detection scheme

EN	V_{OTG_IN} (V_{BUS} Detect Power)	V_{BUS}	DET	Condition
X	X	$3V < V_{BUS} < 5.3V$	H	V_{BUS} within V_{BUS_VALID}
X	X	$3V > V_{BUS}$ or $V_{BUS} > 5.3V$	L	V_{BUS} outside of V_{BUS_VALID}

Figure 16 and Figure 17 shows suggested system level timing diagram for detecting V_{BUS} according to [OTG and EH Supplement]. Figure 3 shows the application diagram. In Figure 16, DET pin remains low after ID pin becomes FALSE, indicating there is not an active voltage source on V_{BUS}. The USB controller proceeds to turn on OTG 5V source and the TPD4S214 respectively; this sequence is recommended because TPD4S214 is powered through the OTG source. After a period of t_{ON}, current starts to flow through the OTG switch and V_{BUS} is ramped to the voltage level of V_{OTG_IN}.

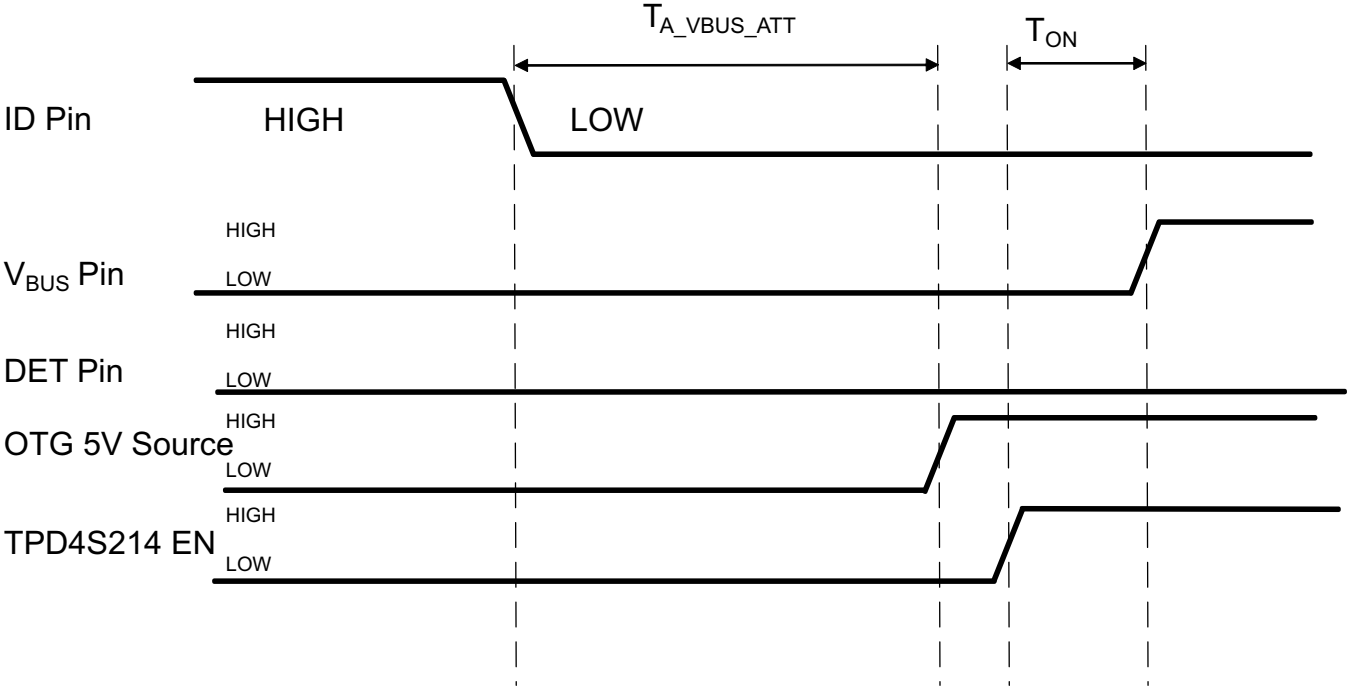


Figure 16. Timing Diagram for Valid USB Device

In Figure 17, DET pin toggles high after an active voltage is detected on V_{BUS} within $T_{A\_VBUS\_ATT}$. This indicates that the USB device attached is not suitable for OTG charging and both OTV 5V source and TPD4S214 remain off.

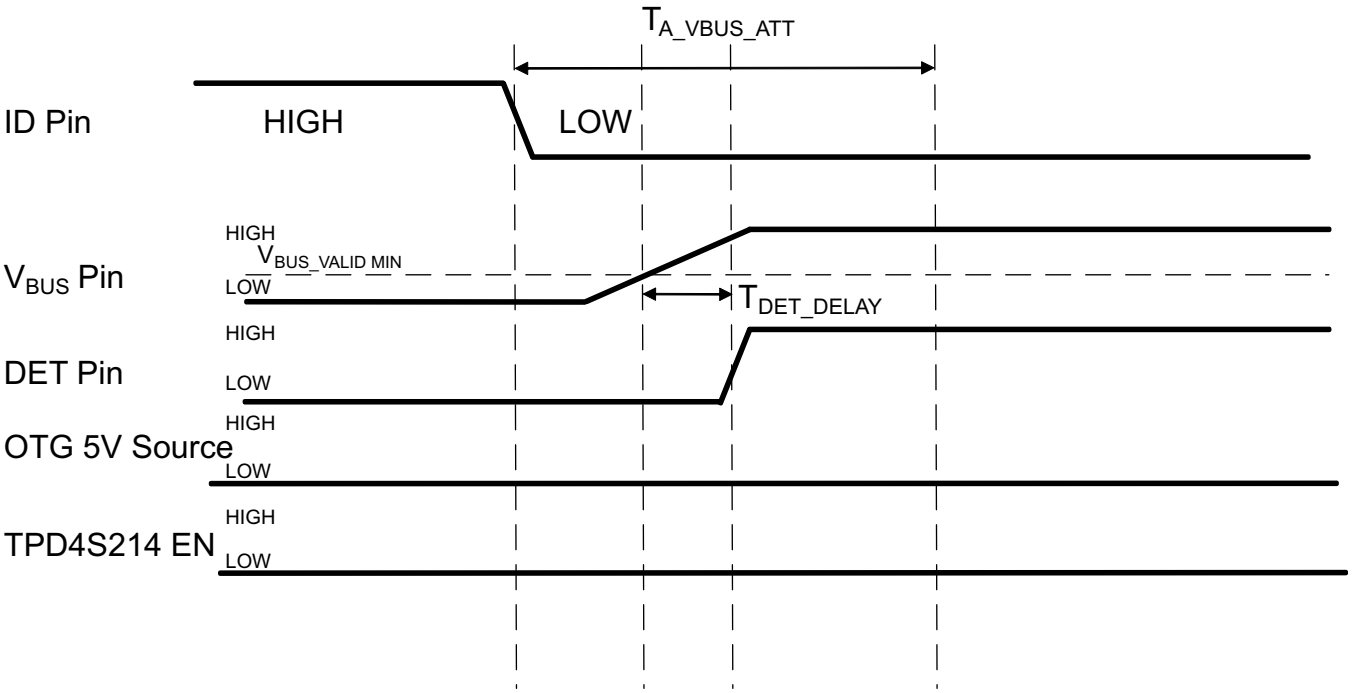


Figure 17. System Level Timing Diagram for invalid USB Device

Related Documents

OTG and EH Supplement] *On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification*, July 14th, 2011. www.usb.org

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPD4S214AYFFR	PREVIEW	DSBGA	YFF	12	3000	TBD	Call TI	Call TI	
TPD4S214YFFR	PREVIEW	DSBGA	YFF	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265