

## Quad Channel High Speed ESD Protection Device

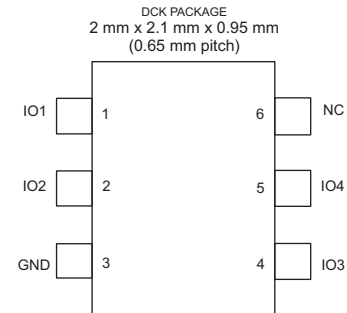
Check for Samples: [TPD4E1B06](#)

### FEATURES

- Provides System Level ESD Protection for Low-Voltage IO Interface
- IEC 61000-4-2 Level 4
  - ±18kV (Contact discharge)
  - ±18kV (Air-gap discharge)
- IO Capacitance 0.8pF (Typ)
- DC Breakdown Voltage 7V (Min)
- Ultra low Leakage Current 10nA (Typ)
- Low ESD Clamping Voltage
- Industrial Temperature Range: –40°C to 125°C
- Small, Easy-to-Route DCK package

### APPLICATIONS

- Cell Phones
- eBook
- Portable Media Players
- Digital Camera



### DESCRIPTION

The TPD4E1B06 is a quad channel ultra low cap ESD protection device. It offers ±18KV IEC air-gap and ±18KV contact ESD protection. Its 0.8pF line capacitance makes it suitable for a wide range of applications. Typical application areas are HDMI, USB2.0, MHL, and DisplayPort.

### ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE <sup>(1)(2)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|---------------------------|---------------|-----------------------|------------------|
| –40°C to 125°C | 3000                      | Tape and reel | TPD4E1B06DCKR         | TBD              |

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).

**PRODUCT PREVIEW**


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**FUNCTIONAL BLOCK DIAGRAM**

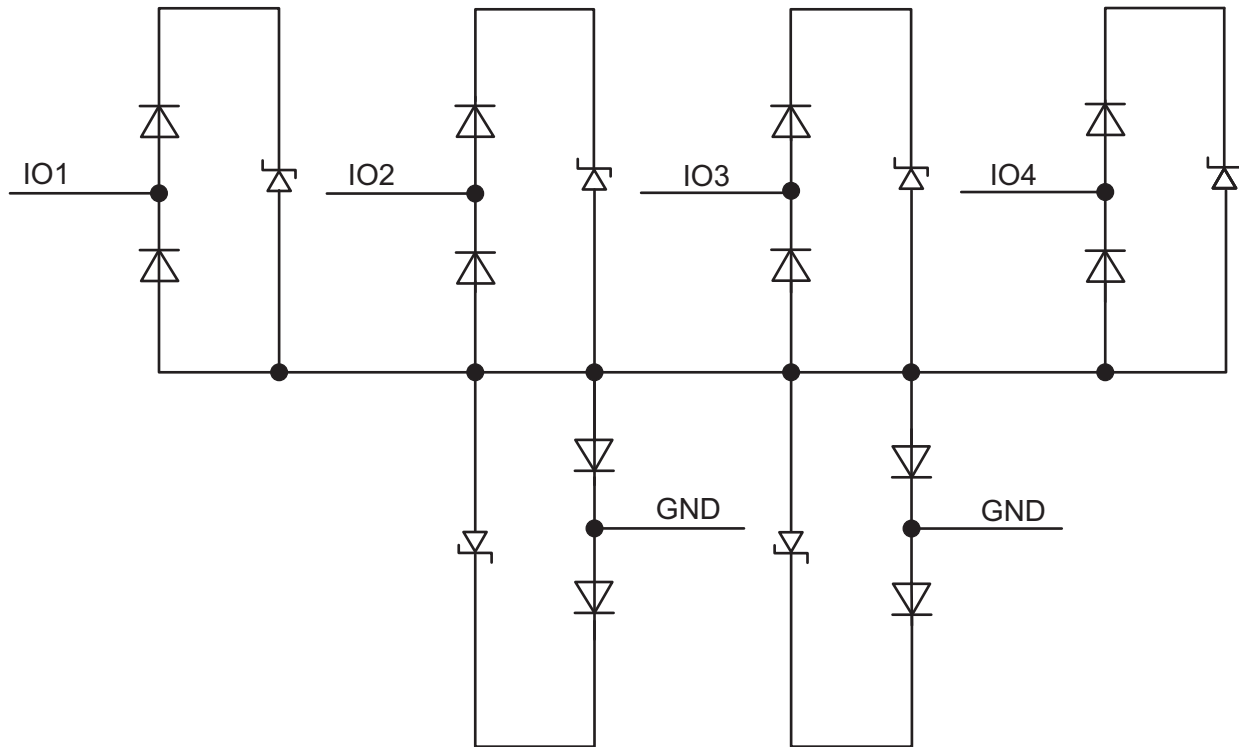


Figure 1. Circuit Schematic Diagram

**TERMINAL FUNCTIONS**

| NAME | PIN    |      | DESCRIPTION           | USAGE  |
|------|--------|------|-----------------------|--|
|      | NUMBER | TYPE |                       |  |
| IO1  | 1      | I/O  | ESD protected channel | Connect to data line as close to the connector as possible |
| IO2  | 2      | I/O  |                       |  |
| IO3  | 4      | I/O  |                       |  |
| IO4  | 5      | I/O  |                       |  |
| NC   | 6      | I/O  | No connect            | Can be left floating, grounded, or connected to Vcc        |
| GND  | 3      | GND  | Ground                | Connect to ground  |

PRODUCT PREVIEW

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

|  | MIN | MAX | UNIT |
|--|-----|-----|------|
| Operating temperature range                          | -40 | 125 | °C   |
| Storage temperature                                  | -65 | 155 | °C   |
| IEC 61000-4-2 contact ESD                            |     | ±18 | kV   |
| IEC 61000-4-2 air-gap ESD                            |     | ±18 | kV   |
| $I_{PP}$ , peak pulse current ( $t_p = 8/20 \mu s$ ) |     | TBD | A    |
| $P_{PP}$ , peak pulse power ( $t_p = 8/20 \mu s$ )   |     | TBD | W    |

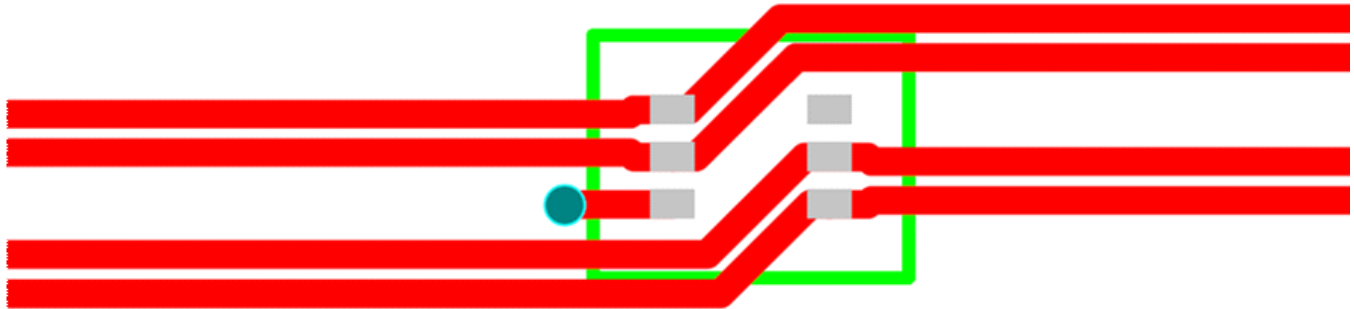
## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER              | TEST CONDITION                           | MIN  | TYP | MAX  | UNIT     |    |
|------------------------|--|--|-----|------|----------|----|
| $V_{RWM}$              | Reverse stand-off voltage                |  |     | 5.5  | V        |    |
| $V_{CLAMP}$            | Clamp voltage with ESD strike, IO to GND | $I_{PP} = 1 \text{ A}$ , $t_p = 8/20 \mu\text{Sec}$ , from I/O to GND                                      |     | 11   | V        |    |
|                        |  | $I_{PP} = 5 \text{ A}$ , $t_p = 8/20 \mu\text{Sec}$ , from I/O to GND                                      |     | 15   | V        |    |
| $R_{DYN}$              | Dynamic resistance                       | $I = 50 \text{ A}$   |     | 1    | $\Omega$ |    |
| $C_L$                  | Line capacitance                         | $f = 1 \text{ GHz}$ , $V_{BIAS} = 0 \text{ V}$   |     | 0.8  | 1        | pF |
|                        |  | $f = 1 \text{ GHz}$ , $V_{BIAS} = 2.5 \text{ V}$   |     | 0.7  | 0.9      | pF |
| $C_{CROSS}$            | Channel to channel input capacitance     | Pin 2 = 0 V, $f = 1 \text{ MHz}$ , $V_{BIAS} = 2.5 \text{ V}$ , between channel pins                       |     | 0.15 | 0.2      | pF |
| $\Delta C_{IO-TO-GND}$ | Variation of channel input capacitance   | Pin 2 = 0V, $f = 1 \text{ MHz}$ , $V_{BIAS} = 2.5 \text{ V}$ , channel_x pin to gnd – channel_y pin to gnd |     | 0.05 | 0.07     | pF |
| $V_{BR}$               | Break-down voltage, IO to GND            | $I_{IO} = 1 \text{ mA}$  |     | 7    | 9.5      | V  |
| $I_{LEAK}$             | Leakage current                          | $V_{IO} = 2.5 \text{ V}$   |     | 1    | 10       | nA |

**APPLICATION INFORMATION**

The TPD4E1B06DCK pin out offers an unique pin out that allows straight through routing with no stubs. [Figure 2](#) shows an example layout. Pins 1 & 2 and pins 4 & 5 are routed differentially. Pin 3 is routed to the ground plane. Pin 6 is not bonded internally in the device and does not need to be routed anywhere on the board.



**Figure 2. TPD4E1B06 Layout Example**

PRODUCT PREVIEW

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish | MSL Peak Temp<br>(3) | Samples<br>(Requires Login) |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|------------------|----------------------|-----------------------------|
| TPD4E1B06DCKR    | PREVIEW       | SC70         | DCK             | 6    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM   |                             |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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|                               |  |
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