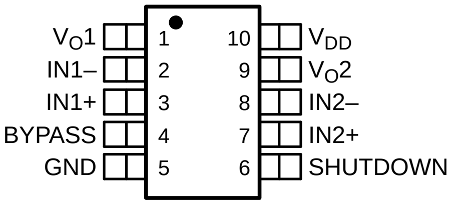
150-mW STEREO AUDIO POWER AMPLIFIER

FEATURES

- **150 mW Stereo Output**
- **Differential Inputs**
- **PC Power Supply Compatible**
  - **Fully Specified for 3.3 V and 5 V Operation**
  - **Operation to 2.5 V**
- **Pop Reduction Circuitry**
- **Internal Mid-Rail Generation**
- **Thermal and Short-Circuit Protection**
- **Surface-Mount Packaging**
  - **PowerPAD™ MSOP**

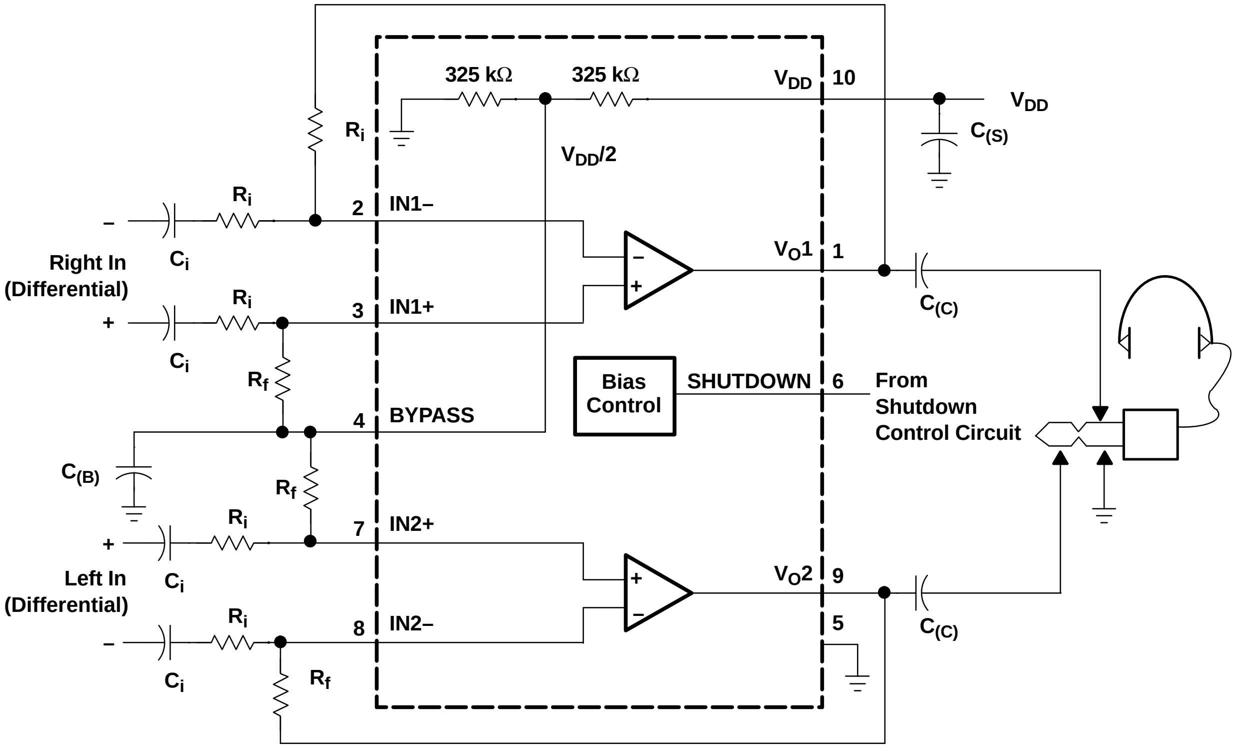
DGQ PACKAGE
(TOP VIEW)



DESCRIPTION

The TPA6112A2 is a stereo audio power amplifier with differential inputs packaged in a 10-pin PowerPAD MSOP package capable of delivering 150 mW of continuous RMS power per channel into 16-Ω loads. Amplifier gain is externally configured by means of two resistors per input channel and does not require external compensation for settings of 1 to 10.

TYPICAL APPLICATION CIRCUIT



PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

THD+N when driving an 16-Ω load from 5 V is 0.03% at 1 kHz, and less than 1% across the audio band of 20 Hz to 20 kHz. For 32-Ω loads, the THD+N is reduced to less than 0.02% at 1 kHz, and is less than 1% across the audio band of 20 Hz to 20 kHz. For 10-kΩ loads, the THD+N performance is 0.005% at 1 kHz, and less than 0.5% across the audio band of 20 Hz to 20 kHz.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICE	MSOP SYMBOLIZATION
	MSOP(1)	
-40°C to 85°C	TPA6112A2DGQ	TI APD

(1) The DGQ package isavailable in left-ended tape and reel only (e.g., TPA6112A2DGQR).

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO		
BYPASS	4	I	Tap to voltage divider for internal mid-supply bias supply. Connect to a 0.1 µF to 1 µF low ESR capacitor for best performance.
GND	5	I	GND is the ground connection.
IN1-	2	I	IN1- is the negative input for channel 1.
IN1+	3	I	IN1+ is the positive input for channel 1.
IN2-	8	I	IN2- is the negative input for channel 2.
IN2+	7	I	IN2+ is the positive input for channel 2.
SHUTDOWN	6	I	Puts the device in a low quiescent current mode when held high.
V_{DD}	10	I	V_{DD} is the supply voltage terminal.
V_O1	1	O	V_O1 is the audio output for channel 1.
V_O2	9	O	V_O2 is the audio output for channel 2.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted(1))

		UNITS
V_{DD}	Supply voltage	6 V
V_I	Input voltage	-0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation	internally limited
T_J	Operating junction temperature range	-40°C to 150°C
T_{stg}	Storage temperature range	-65°C to 150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

(1) Stresses beyond thoselisted under absolute maximum ratings may cause permanent damage to the device.These are stress ratings only, and functional operation of the device at theseor any other conditions beyond those indicated under recommended operatingconditions is not implied. Exposure to absolute-maximum-rated conditions forextended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGQ	2.14 W(1)	17.1 mW/°C	1.37 W	1.11 W

(1) Please see the Texas Instrumentsdocument, *PowerPAD Thermally EnhancedPackage Application Report* (literature number SLMA002), for moreinformation on the PowerPAD package. The thermal data was measured on a PCBlayout based on the information in the section entitled*Texas Instruments Recommended Board forPowerPAD* on page 33 of the before mentioneddocument.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.5	5.5	V
T_A	Operating free-air temperature	-40	85	°C
V_{IH}, (SHUTDOWN)	High-level input voltage	60% x V_{DD}		V
V_{IL}, (SHUTDOWN)	Low-level input voltage		25% x V_{DD}	V

DC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, $V_{DD} = 2.5$ V (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	$A_V = 2$ V/V			15	mV
PSRR	Power supply rejection ratio	$V_{DD} = 3.2$ V to 3.4 V		83		dB
I_{DD}	Supply current	SHUTDOWN = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode	SHUTDOWN = V_{DD}		10	50	µA
Z_i	Input impedance			>1		MΩ

AC OPERATING CHARACTERISTICS

$V_{DD} = 3.3$ V, $T_A = 25°C$, $R_L = 16\ \Omega$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		60		mW
THD+N	Total harmonic distortion + noise	$P_O = 40$ mW, 20 - 20 kHz		0.4%		
B_{OM}	Maximum output power BW	G = 10, THD < 5%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection ratio	f = 1 kHz		71		dB
	Channel/channel output separation	f = 1 kHz		89		dB
SNR	Signal-to-noise ratio	$P_O = 50$ mW, $A_V = 1$		100		dB
V_n	Noise output voltage	$A_V = 1$		11		µV(rms)

DC ELECTRICAL CHARACTERISTICS

At $T_A = 25°C$, $V_{DD} = 5\ .5$ V (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OO}	Output offset voltage	$A_V = 2$ V/V			15	mV
PSRR	Power supply rejection ratio	$V_{DD} = 4.9$ V to 5.1 V		76		dB
I_{DD}	Supply current	SHUTDOWN = 0 V		1.5	3	mA
$I_{DD(SD)}$	Supply current in SHUTDOWN mode	SHUTDOWN = V_{DD}		60	100	µA
$\|I_{IH}\|$	High-level input current (SHUTDOWN)	$V_{DD} = 5.5$ V, $V_I = V_{DD}$			1	µA
$\|I_{IL}\|$	Low-level input current (SHUTDOWN)	$V_{DD} = 5.5$ V, $V_I = 0$ V			1	µA
Z_i	Input impedance			>1		MΩ

AC OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 16 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		150		mW
THD+N	Total harmonic distortion + noise	P_O = 100 mW, 20 - 20 kHz		0.6%		
B_{OM}	Maximum output power BW	G = 10, THD < 5%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection ratio	f = 1 kHz		61		dB
	Channel/channel output separation	f = 1 kHz		90		dB
SNR	Signal-to-noise ratio	P_O = 100 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11.7		µV(rms)

AC OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		40		mW
THD+N	Total harmonic distortion + noise	P_O = 30 mW, 20 - 20 kHz		0.4%		
B_{OM}	Maximum output power BW	A_V = 10, THD < 2%		> 20		kHz
	Phase margin	Open loop		96°		
	Supply ripple rejection ratio	f = 1 kHz		71		dB
	Channel/channel output separation	f = 1 kHz		95		dB
SNR	Signal-to-noise ratio	P_O = 40 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11		µV(rms)

AC OPERATING CHARACTERISTICS

V_{DD} = 5 V, T_A = 25°C, R_L = 32 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power (each channel)	THD≤ 0.1%, f = 1 kHz		90		mW
THD+N	Total harmonic distortion + noise	P_O = 60 mW, 20 - 20 kHz		0.4%		
B_{OM}	Maximum output power BW	A_V = 10, THD < 2%		> 20		kHz
	Phase margin	Open loop		97°		
	Supply ripple rejection ratio	f = 1 kHz		61		dB
	Channel/channel output separation	f = 1 kHz		98		dB
SNR	Signal-to-noise ratio	P_O = 90 mW, A_V = 1		100		dB
V_n	Noise output voltage	A_V = 1		11.7		µV(rms)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
THD+N	Total harmonic distortion plus noise	vs Frequency	1, 3, 5, 6, 7, 9, 11, 13,
		vs Output power	2, 4, 8, 10, 12, 14
	Supply ripple rejection ratio	vs Frequency	15, 16
V_n	Output noise voltage	vs Frequency	17, 18
	Crosstalk	vs Frequency	19 - 24
	Shutdown attenuation	vs Frequency	25, 26
	Open-loop gain and phase margin	vs Frequency	27, 28
	Output power	vs Load resistance	29, 30,
I_{DD}	Supply current	vs Supply voltage	31
SNR	Signal-to-noise ratio	vs Voltage gain	32
	Power dissipation/amplifier	vs Load power	33, 34

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

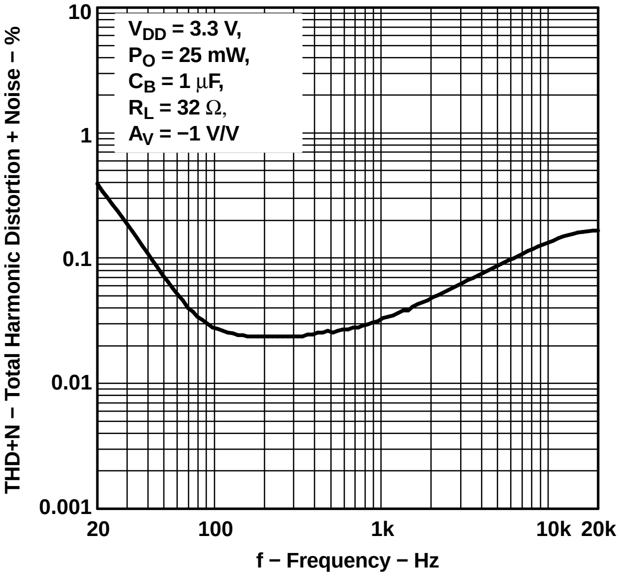


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

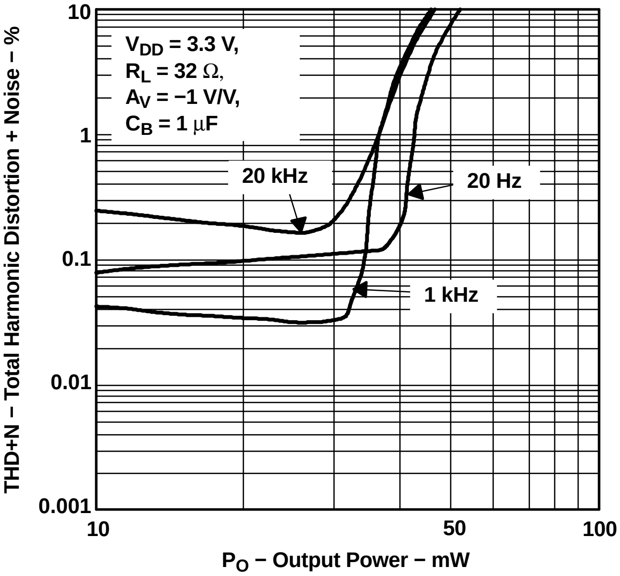


Figure 2.

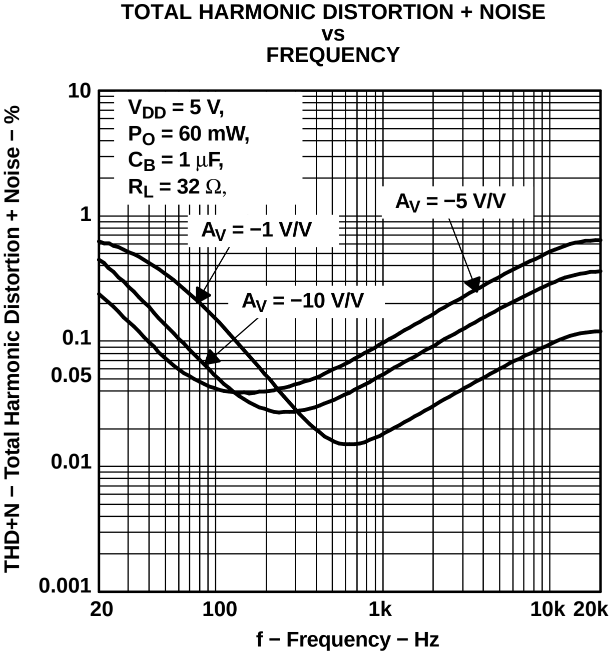


Figure 3.

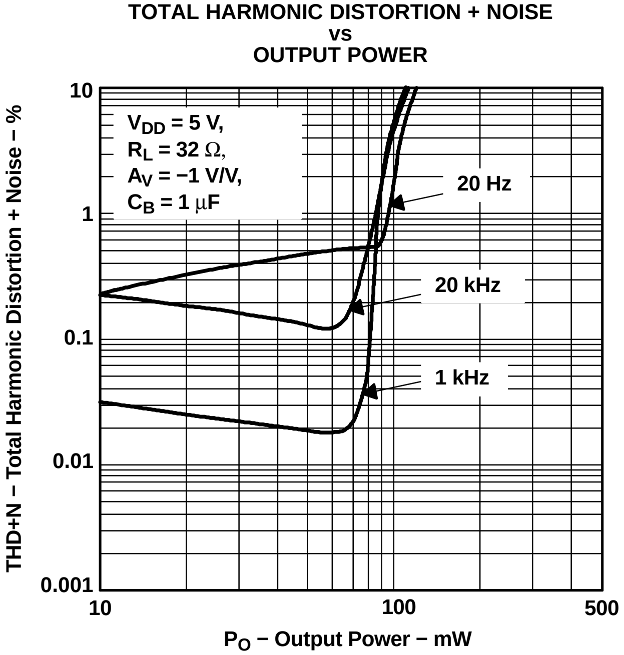


Figure 4.

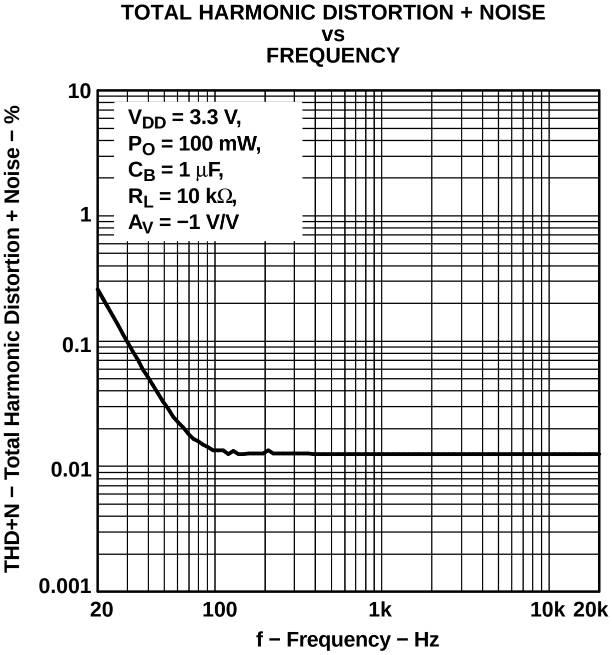


Figure 5.

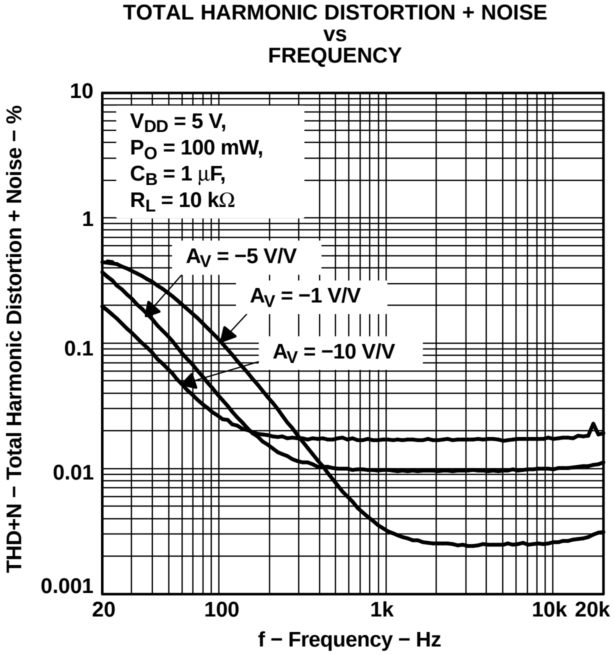


Figure 6.

**TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY**

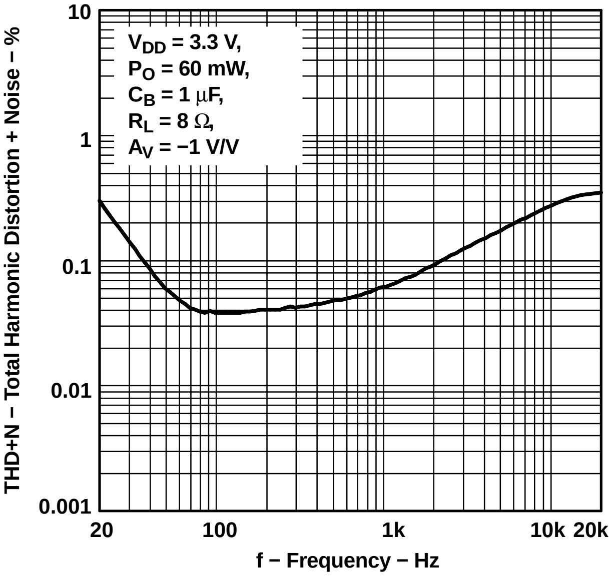


Figure 7.

**TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER**

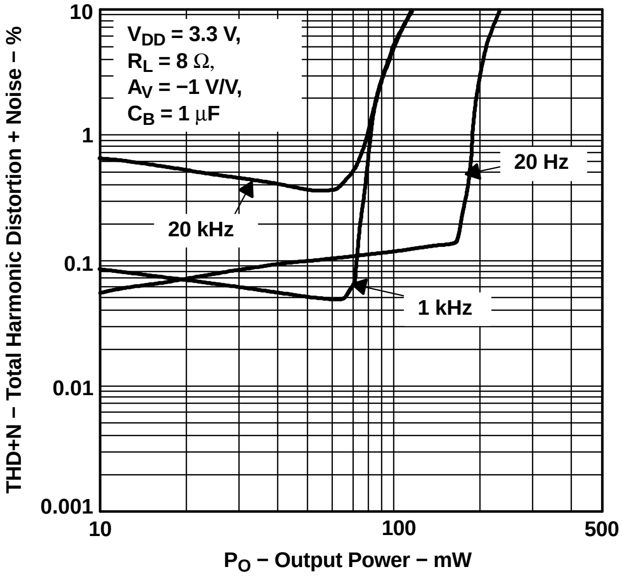


Figure 8.

**TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY**

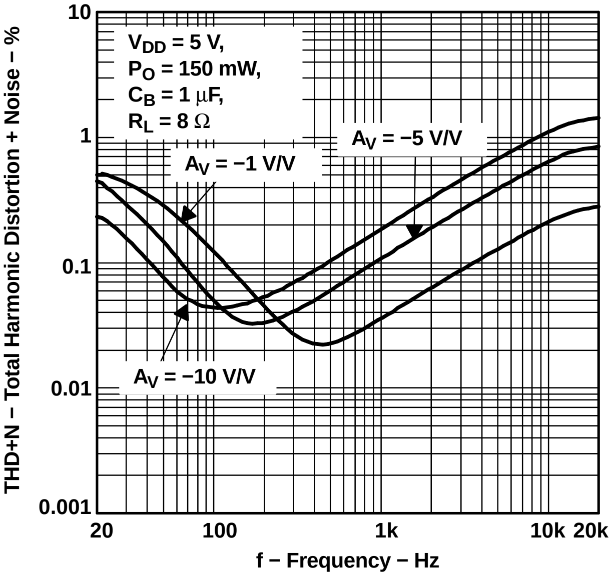


Figure 9.

**TOTAL HARMONIC DISTORTION + NOISE
vs
OUTPUT POWER**

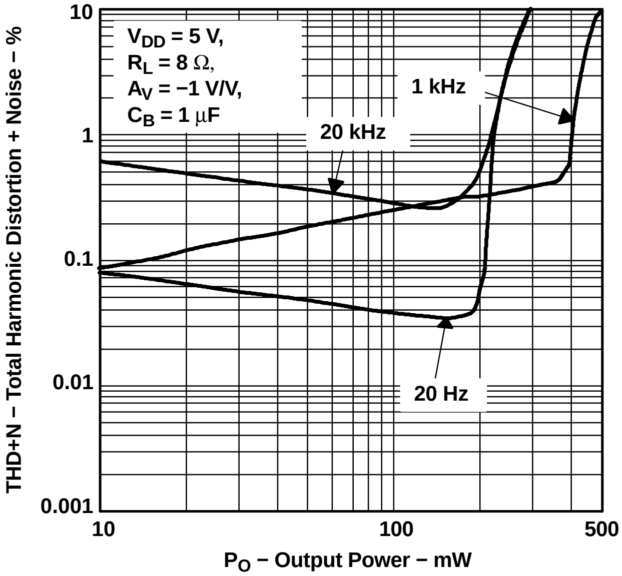


Figure 10.

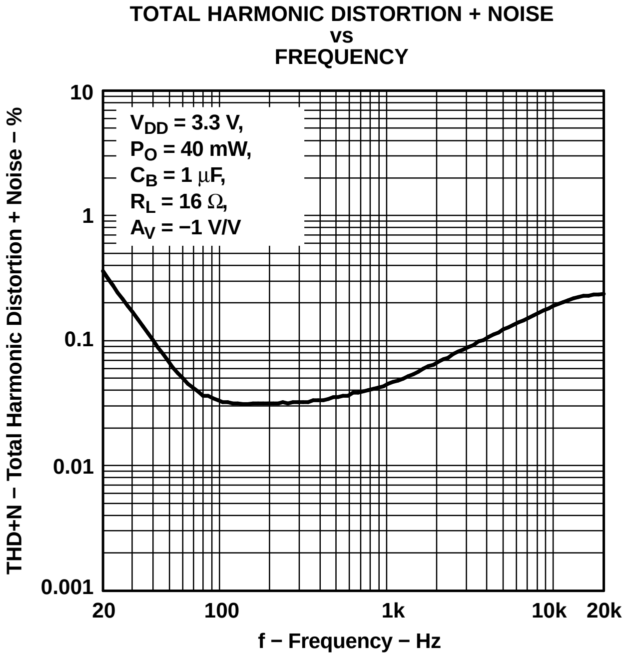


Figure 11.

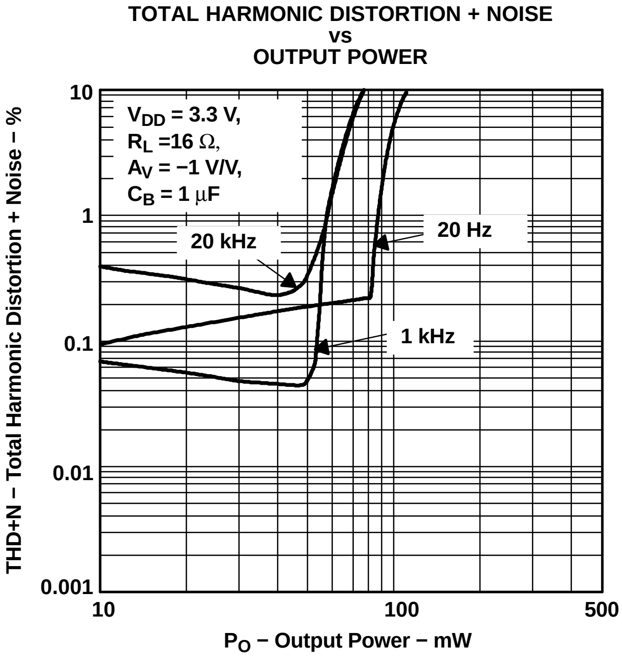


Figure 12.

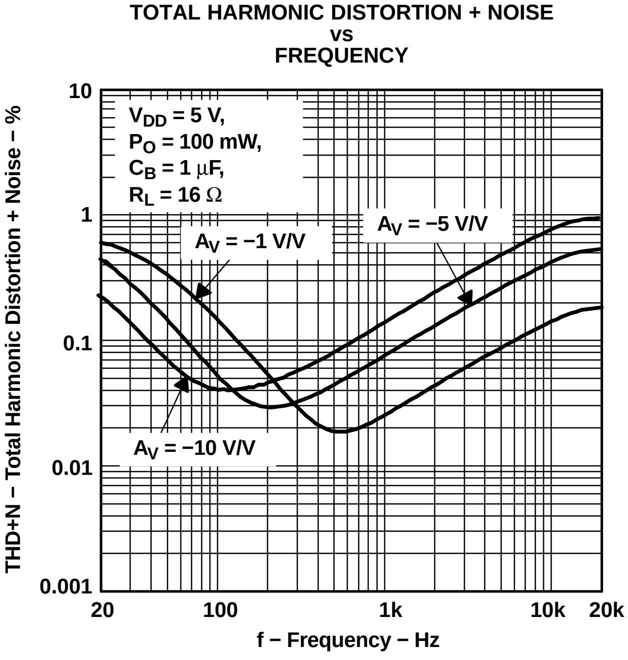


Figure 13.

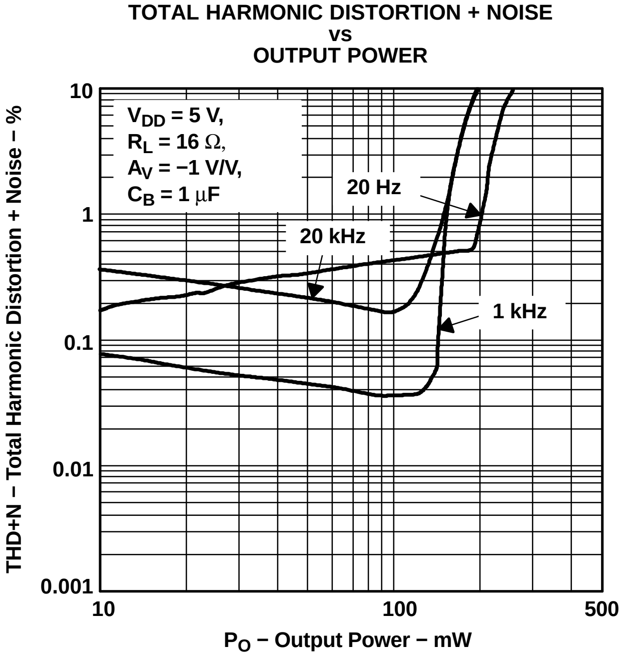


Figure 14.

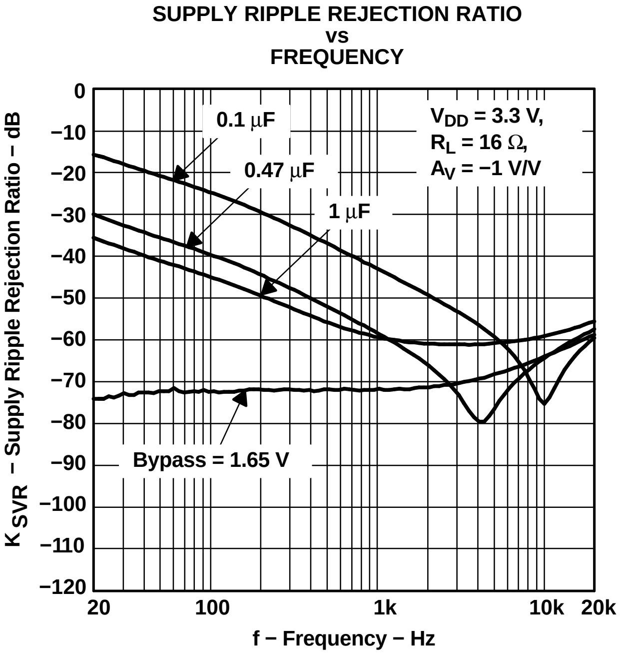


Figure 15.

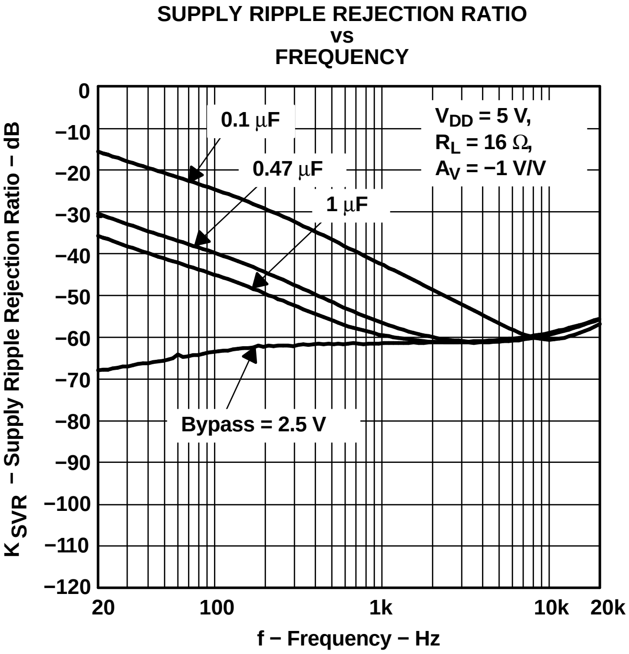


Figure 16.

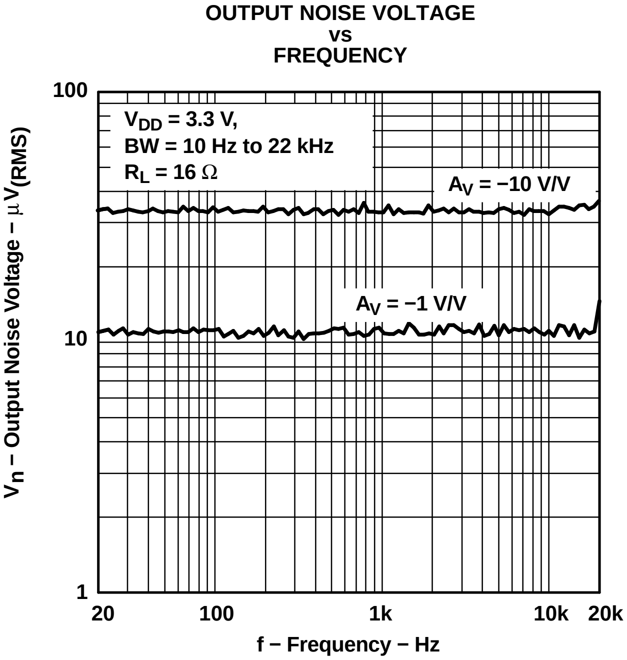


Figure 17.

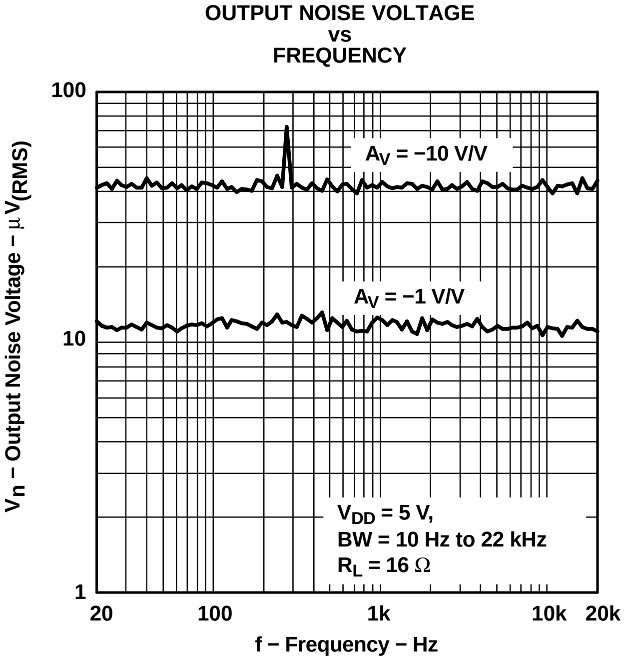


Figure 18.

CROSSTALK
vs
FREQUENCY

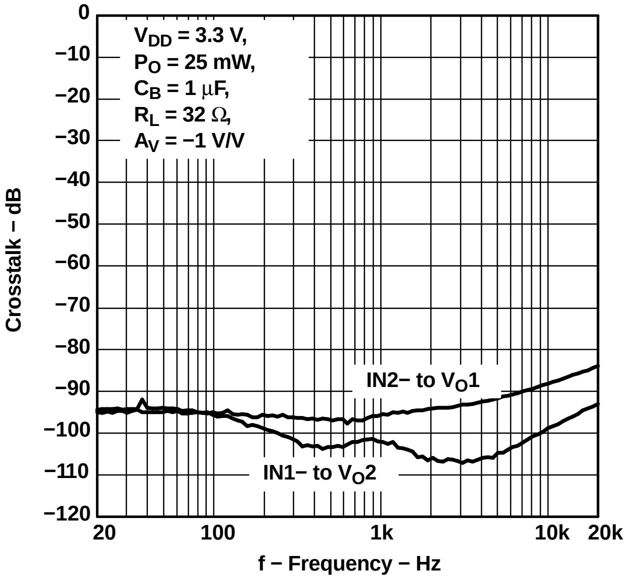


Figure 19.

CROSSTALK
vs
FREQUENCY

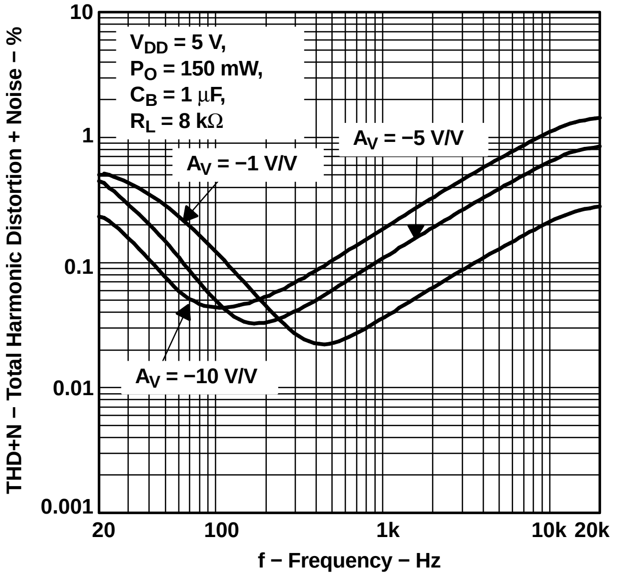


Figure 20.

CROSSTALK
vs
FREQUENCY

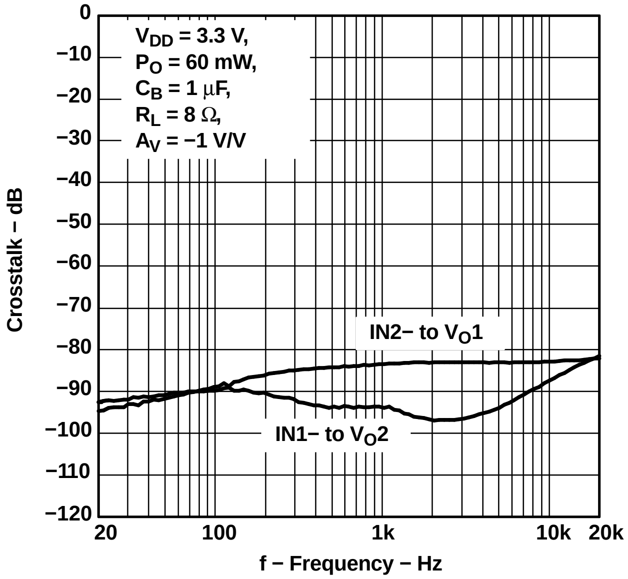


Figure 21.

CROSSTALK
vs
FREQUENCY

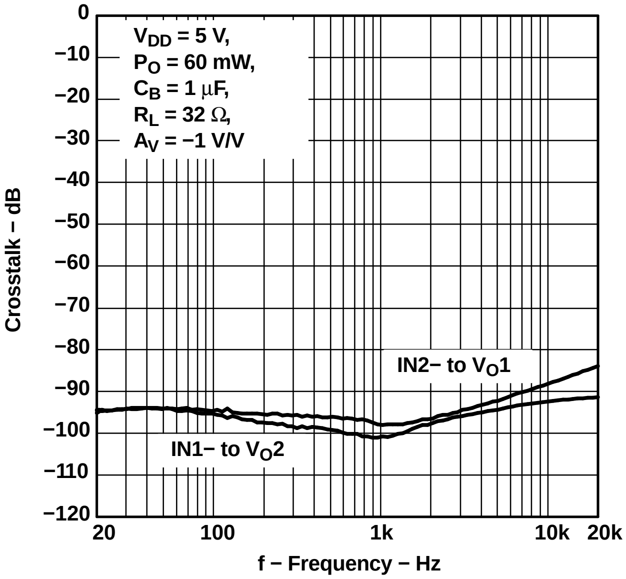


Figure 22.

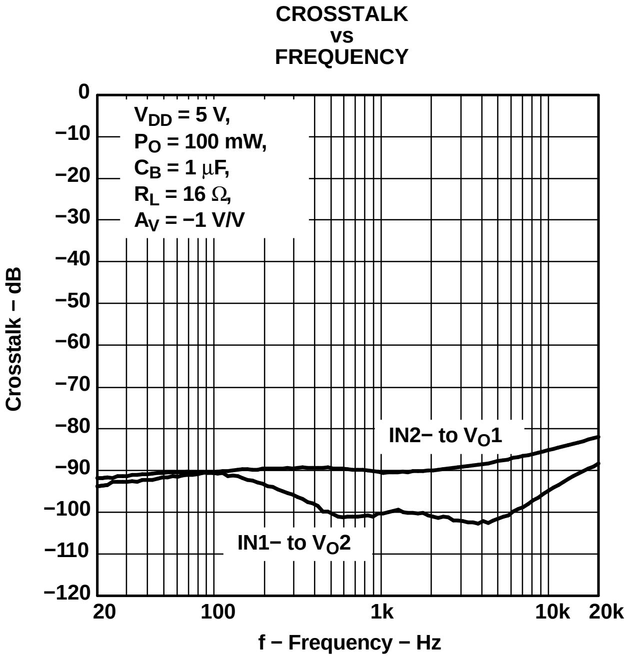
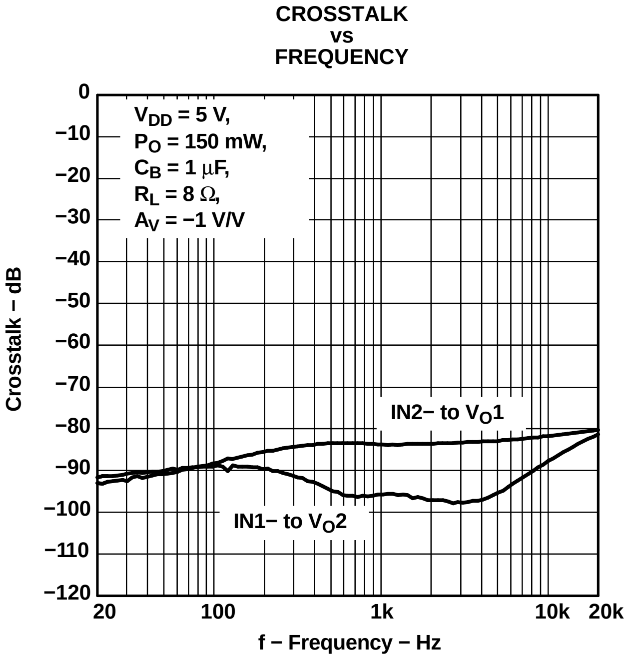


Figure 23.



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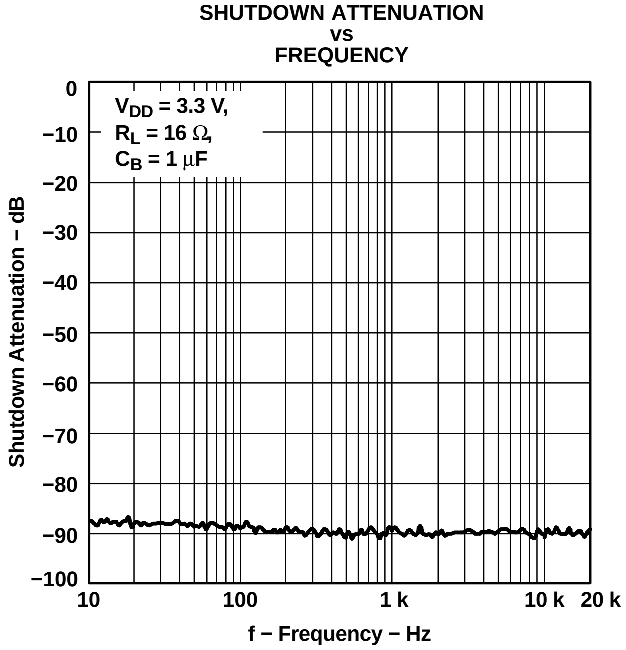

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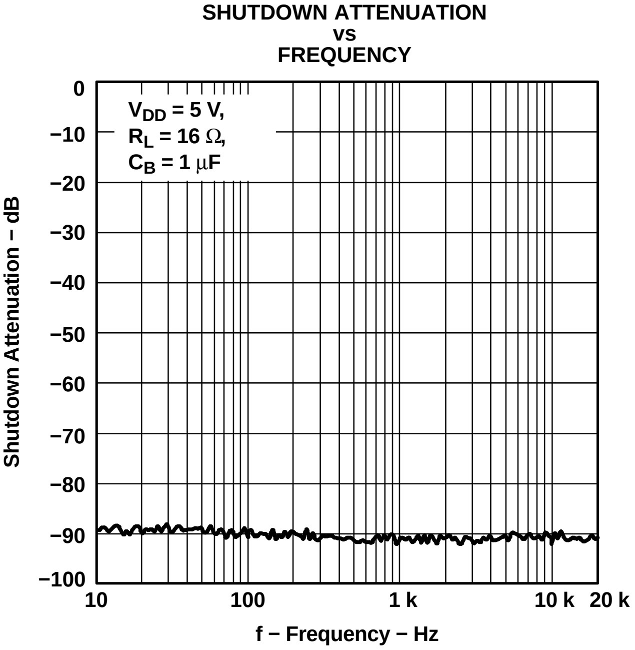


Figure 26.

OPEN-LOOP GAIN AND PHASE MARGIN
vs
FREQUENCY

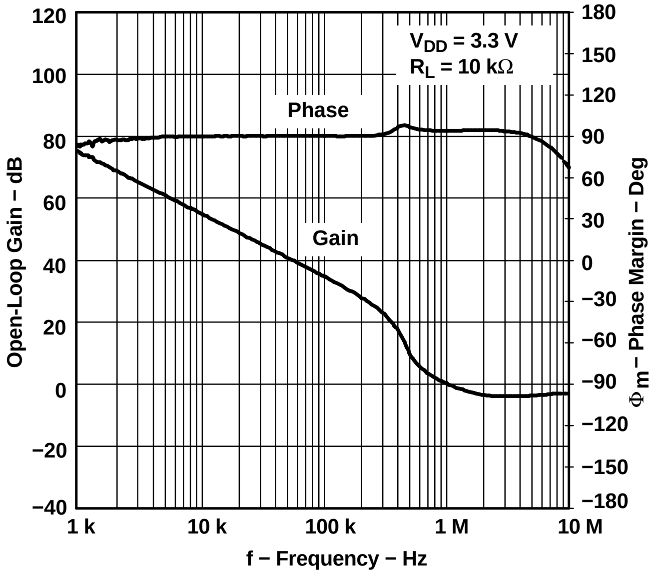


Figure 27.

OPEN-LOOP GAIN AND PHASE MARGIN
vs
FREQUENCY

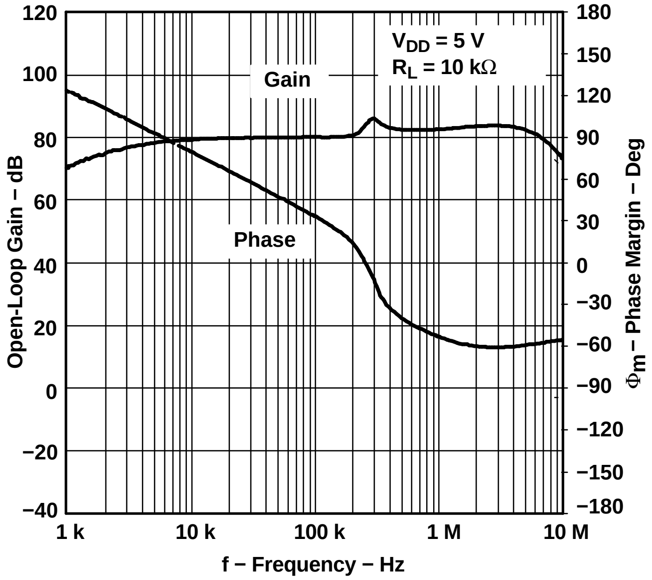


Figure 28.

OUTPUT POWER
vs
LOAD RESISTANCE

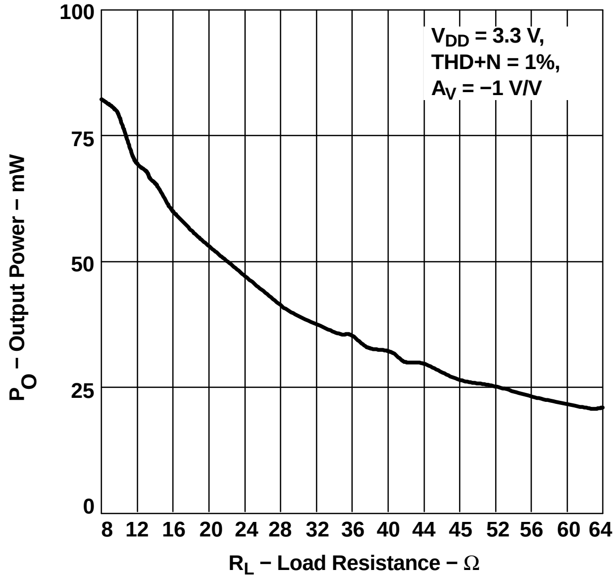


Figure 29.

OUTPUT POWER
vs
LOAD RESISTANCE

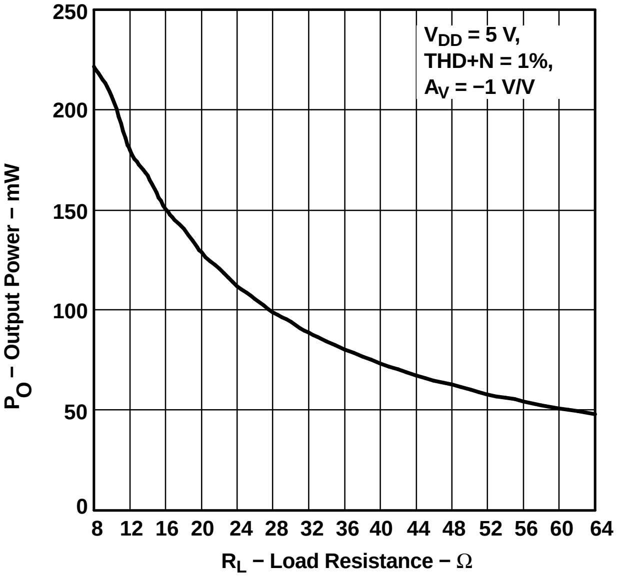


Figure 30.

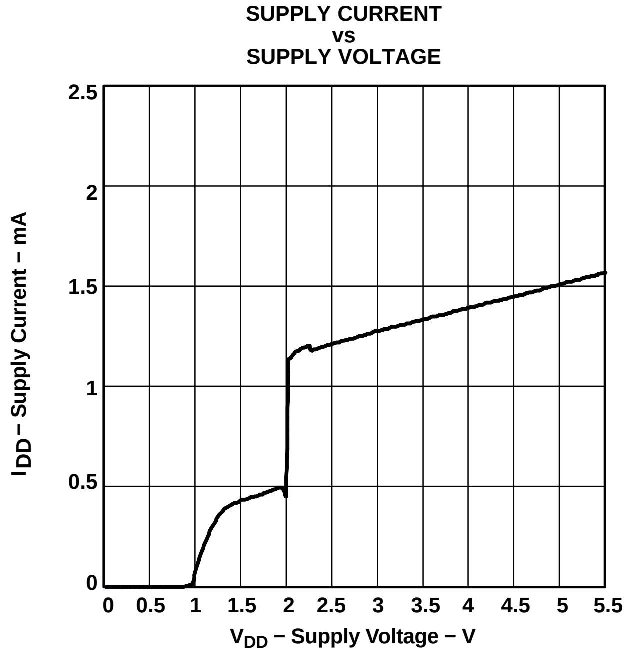

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

Figure 31.

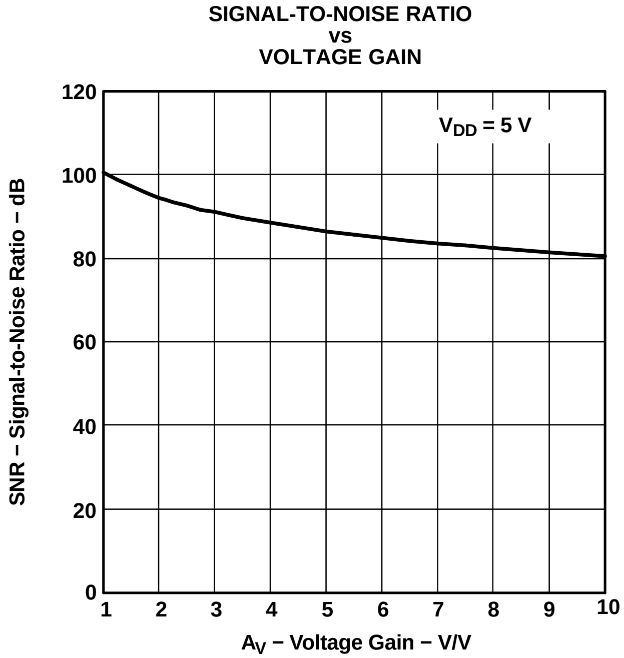

SIGNAL-TO-NOISE RATIO
vs
VOLTAGE GAIN

Figure 32.

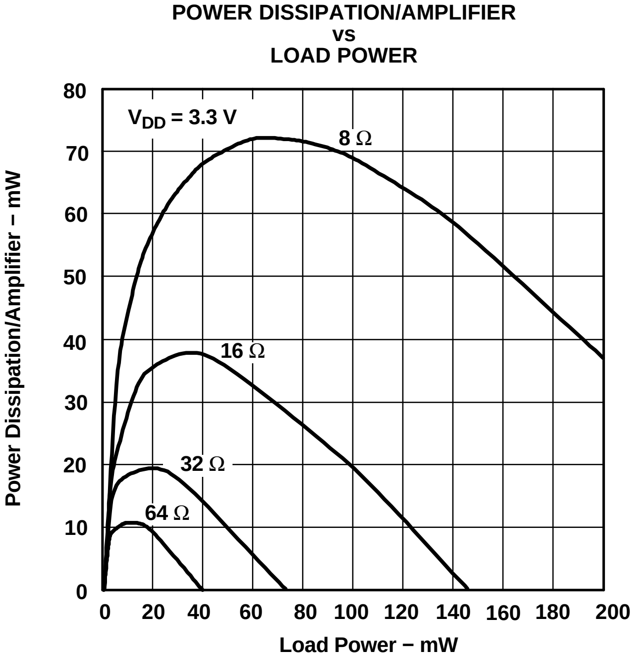

POWER DISSIPATION/AMPLIFIER
vs
LOAD POWER

Figure 33.

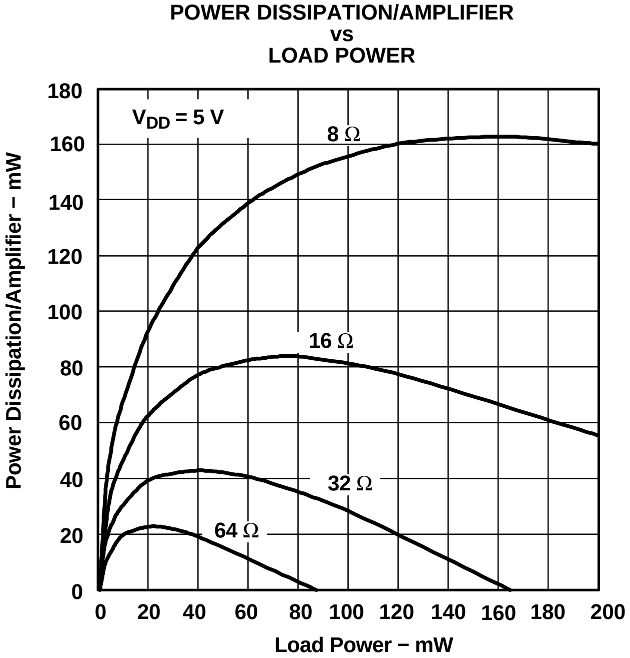

POWER DISSIPATION/AMPLIFIER
vs
LOAD POWER

Figure 34.

APPLICATION INFORMATION

GAIN SETTING RESISTORS, R_f and R_i

The gain for the TPA6112A2 is set by resistors R_f and R_i according to Equation 1.

$$\text{Gain} \leq \times \frac{R_f}{R_i}\Bigg) \tag{1}$$

Given that the TPA6112A2 is a MOS amplifier, the input impedance is very high. Consequently input leakage currents are not generally a concern. However, noise in the circuit increases as the value of R_f increases. In addition, a certain range of R_f values is required for proper start-up operation of the amplifier. Considering these factors, it is recommended that the effective impedance seen by the inverting node of the amplifier be set between 5 kΩ and 20 kΩ. The effective impedance is calculated using Equation 2.

$$\text{Effective Impedance} \leq \frac{R_f R_i}{R_f \times R_i} \tag{2}$$

For example, if the input resistance is 20 kΩ and the feedback resistor is 20 kΩ, the gain of the amplifier is -1, and the effective impedance at the inverting terminal is 10 kΩ, a value within the recommended range.

For high performance applications, metal-film resistors are recommended because they tend to have lower noise levels than carbon resistors. For values of R_f above 50 kΩ, the amplifier tends to become unstable due to a pole formed from R_f and the inherent input capacitance of the MOS input structure. For this reason, a small compensation capacitor of approximately 5 pF should be placed in parallel with R_f. This, in effect, creates a low-pass filter network with the cutoff frequency defined by Equation 3.

$$f_{c(lowpass)} \times \frac{1}{2\pi R_f C_F} \tag{3}$$

For example, if R_f is 100 kΩ and C_F is 5 pF then $f_{c(lowpass)}$ is 318 kHz, which is well outside the audio range.

INPUT CAPACITOR, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and R_i form a high-pass filter with the corner frequency determined in Equation 4.

$$f_{c(highpass)} \times \frac{1}{2\pi R_i C_i} \tag{4}$$

The value of C_i directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 20 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 4 is reconfigured as Equation 5.

$$C_i \times \frac{1}{2\pi R_i f_{c(highpass)}} \tag{5}$$

In this example, C_i is 0.40 µF, so one would likely choose a value in the range of 0.47 µF to 1 µF. A further consideration for this capacitor is the leakage path from the input source through the input network formed by R_i, C_i, and the feedback resistor (R_f) to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high-gain applications (gain >10). For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, connect the positive side of the capacitor to the amplifier input in most applications. The dc level there is held at $V_{DD}/2$—likely higher than the source dc level. It is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING, $C_{(S)}$

The TPA6112A2 is a high-performance CMOS audio amplifier that requires adequate power-supply decoupling to minimize the output total harmonic distortion (THD). Power-supply decoupling also prevents oscillations when long lead lengths are used between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 µF, placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the power amplifier is recommended.

MIDRAIL BYPASS CAPACITOR, $C_{(B)}$

The midrail bypass capacitor, $C_{(B)}$, serves several important functions. During start up, $C_{(B)}$ determines the rate at which the amplifier starts up. This helps to push the start-up pop noise into the subaudible range (so low it can not be heard). The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier. The capacitor is fed from a 230-kΩ source inside the amplifier. To keep the start-up pop as low as possible, maintain the relationship shown in Equation 6.

$$\frac{1}{\left(C_{(B)} \times 230\ \text{k}\Omega\right)} \leq \frac{1}{\left(C_i R_i\right)} \tag{6}$$

Consider an example circuit where $C_{(B)}$ is 1 µF, C_i is 1 µF, and R_i is 20 kΩ. Subsitituting these values into the equation 9 results in: 6.25 ≤ 50 which satisfies the rule. Bypass capacitor, $C_{(B)}$, values of 0.1 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance.

OUTPUT COUPLING CAPACITOR, $C_{(C)}$

In a typical single-supply, single-ended (SE) configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 7.

$$f_c \times \frac{1}{2\pi R_L C_{(C)}} \tag{7}$$

The main disadvantage, from a performance standpoint, is that the typically-small load impedance drives the low-frequency corner higher. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 68 µF is chosen and loads vary from 32 Ω to 47 kΩ. Table 1 summarizes the frequency response characteristics of each configuration.

Table 1. Common Load Impedances vs Low-Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	LOWEST FREQUENCY
32 Ω	68 µF	73 Hz
10,000 Ω	68 µF	0.23 Hz
47,000 Ω	68 µF	0.05 Hz

As Table 1 indicates, headphone response is adequate, and drive into line level inputs (a home stereo for example) is very good.

The output coupling capacitor required in single-supply SE mode also places additional constraints on the selection of other components in the amplifier circuit. With the rules described earlier still valid, add the following relationship:

$$\frac{1}{\left(C_{(B)} \times 230\ \text{k}\Omega\right)} \leq \frac{1}{\left(C_i R_i\right)} \ll \frac{1}{R_L C_{(C)}} \tag{8}$$

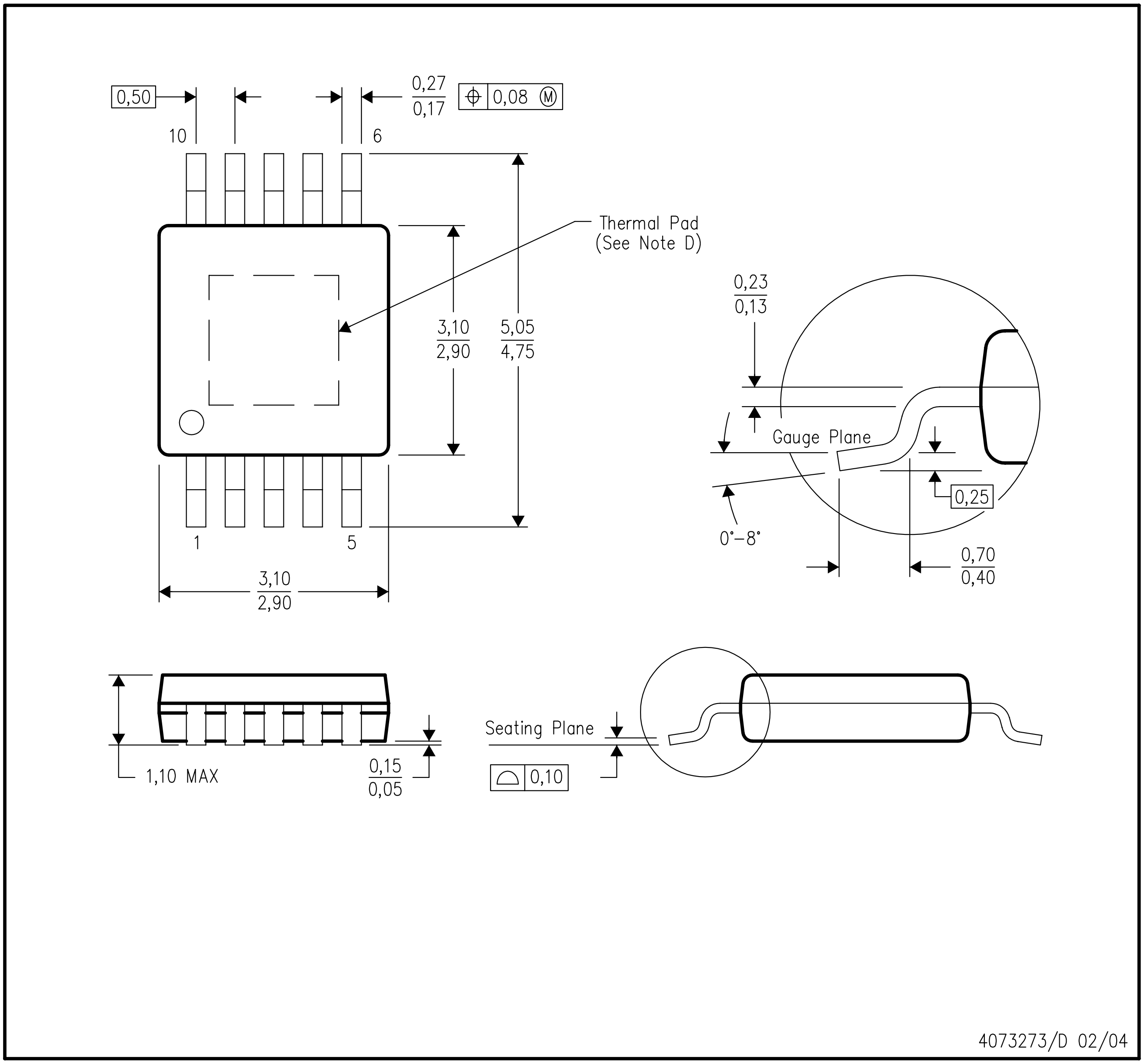
USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application. A real capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

5-V VERSUS 3.3-V OPERATION

The TPA6112A2 was designed for operation over a supply range of 2.5 V to 5.5 V. This data sheet provides full specifications for 5-V and 3.3-V operation, since these are considered to be the two most common supply voltages. There are no special considerations for 3.3-V versus 5-V operation as far as supply bypassing, gain setting, or stability. The most important consideration is that of output power. Each amplifier in theTPA6112A2 can produce a maximum voltage swing of V_{DD}– 1 V. This means, for 3.3-V operation, clipping starts to occur when $V_{O(PP)}$ = 2.3 V as opposed when $V_{O(PP)}$ = 4 V while operating at 5 V. The reduced voltage swing subsequently reduces maximum output power into the load before distortion becomes significant.

DGQ (S-PDSO-G10) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. Falls within JEDEC MO-187 variation BA-T.

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