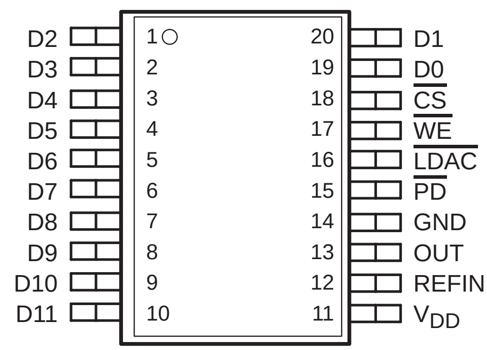
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of −40°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree**†
- **Single Supply 2.7-V to 5.5-V Operation**
- **±0.4 LSB Differential Nonlinearity (DNL), ±1.5 LSB Integral Nonlinearity (INL)**
- **12-Bit Parallel Interface**
- **Compatible With TMS320 DSP**
- **Internal Power On Reset**
- **Settling Time 1 µs Typ**
- **Low Power Consumption:**
  - **8 mW for 5-V Supply**
  - **4.3 mW for 3-V Supply**
- **Reference Input Buffers**
- **Voltage Output**
- **Monotonic Over Temperature**
- **Asynchronous Update**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

applications

- **Battery Powered Test Instruments**
- **Digital Offset and Gain Adjustment**
- **Battery Operated/Remote Industrial Controls**
- **Machine and Motion Control Devices**
- **Cordless and Wireless Telephones**
- **Speech Synthesis**
- **Communication Modulators**
- **Arbitrary Waveform Generation**

DW PACKAGE
(TOP VIEW)



description

The TLV5619 is a 12-bit voltage output DAC with a microprocessor and TMS320 compatible parallel interface. The 12 data bits are double buffered so that the output can be updated asynchronously using the $\overline{\text{LDAC}}$ pin. During normal operation, the device dissipates 8 mW at a 5-V supply and 4.3 mW at a 3-V supply. The power consumption can be lowered to 50 nW by setting the DAC to power-down mode.

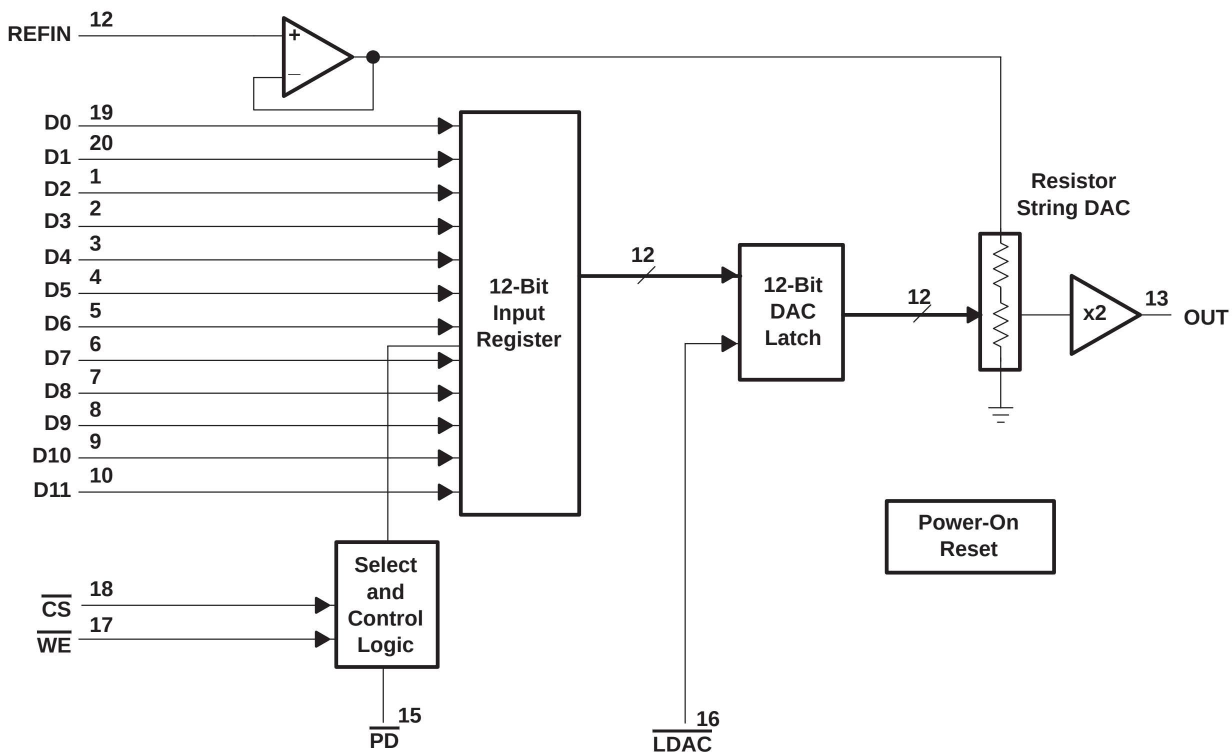
The output voltage is buffered by a ×2 gain rail-to-rail amplifier, which features a Class A output stage to improve stability and reduce settling time.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOP − DW	Tape and reel	TLV5619QDWREP	TLV5619QEP

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
$\overline{CS}$	18	I	Chip select
D0 (LSB)−D11 (MSB)	19, 20, 1 − 10	I	Parallel data input
GND	14		Ground
$\overline{LDAC}$	16	I	Load DAC
OUT	13	O	Analog output
$\overline{PD}$	15	I	When low, disables all buffer amplifier voltages to reduce supply current
REFIN	12	I	Voltage reference input
V_{DD}	11		Positive power supply
$\overline{WE}$	17	I	Write enable

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage (V_{DD} to GND) . . . 7 V
Analog input voltage range . . . − 0.3 V to V_{DD} + 0.3 V
Reference input voltage . . . V_{DD} + 0.3 V
Digital input voltage range to GND . . . − 0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A: . . . −40°C to 125°C
Storage temperature range, T_{stg} . . . −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (5-V Supply)		4.5	5	5.5	V
Supply voltage, V_{DD} (3-V Supply)		2.7	3	3.3	V
High-level digital input voltage, V_{IH}	V_{DD} = 2.7 V	2			V
	V_{DD} = 5.5 V	2.4			
Low-level digital input voltage, V_{IL}	V_{DD} = 2.7 V			0.6	V
	V_{DD} = 5.5 V			0.8	
Reference voltage, V_{ref} to REFIN terminal (5-V Supply)		0	2.048	V_{DD} − 1.5	V
Reference voltage, V_{ref} to REFIN terminal (3-V Supply)		0	1.024	V_{DD} − 1.5	V
Load resistance, R_L		2	10		kΩ
Load capacitance, C_L				100	pF
Operating free-air temperature, T_A		−40		125	°C

NOTES: 1. The recommended operating levels for both V_{IH} and V_{IL} apply to all valid values of V_{DD}.
2. Reference input voltages greater than V_{DD}/2 will cause output saturation for large DAC codes.

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

static DAC specifications

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Resolution		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V		12			bits
	Integral nonlinearity (INL)		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See Note 3		±1.5	±4	LSB
	Differential nonlinearity (DNL)		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See Note 4		± 0.4	± 1	LSB
E_{ZS}	Zero-scale error (offset error at zero scale)		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See Note 5		±3	±20	mV
	Zero-scale-error temperature coefficient		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See Note 6		3		ppm/°C
E_G	Gain error		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See Note 7		±0.25	±0.5	% of FS voltage
	Gain error temperature coefficient		$V_{ref(REFIN)}$ = 2.048 V at 5 V, 1.024 V at 3 V,	See Note 8		1		ppm/°C
PSRR	Power-supply rejection ratio	Zero scale	See Notes 9 and 10			65		dB
		Gain				65		

NOTES: 3. The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.
4. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
5. Zero-scale error is the deviation from zero voltage output when the digital input code is zero.
6. Zero-scale-error temperature coefficient is given by: E_{ZS} TC = [E_{ZS} (T_{max}) − E_{ZS} (T_{min})]/V_{ref} × 10^6/(T_{max} − T_{min}).
7. Gain error is the deviation from the ideal output (2 × V_{ref} − 1 LSB) with an output load of 10 kΩ excluding the effects of the zero-error.
8. Gain temperature coefficient is given by: E_G TC = [E_G(T_{max}) − E_G (T_{min})]/V_{ref} × 10^6/(T_{max} − T_{min}).
9. Zero-scale-error rejection ratio (EZS-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the zero-code output voltage.
10. Gain-error rejection ratio (EG-RR) is measured by varying the V_{DD} from 4.5 V to 5.5 V dc and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

output specifications

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Voltage output range	R_L = 10 kΩ		0		V_{DD}−0.4	V
	Output load regulation accuracy	$V_{O(OUT)}$ = 4.096 V, 2.048 V	R_L = 2 kΩ		0.1	0.29	% of FS voltage
$I_{OSC(source)}$	Output short circuit source current	$V_{O(OUT)}$ = 0 V, Full scale code	5-V Supply		100		mA
			3-V Supply		25		
$I_{O(source)}$	Output source current	R_L = 100 Ω	5-V Supply		10		mA
			3-V Supply		10		

electrical characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

reference input (REFIN)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ref}	Reference input voltage	See Note 11	0		V_{DD}−1.5	V
R_i	Reference input resistance			10		MΩ
C_i	Reference input capacitance			5		pF
	Reference feed through	REFIN = 1 V_{pp} at 1 kHz + 1.024 V dc (see Note 12)		−60		dB
	Reference input bandwidth	REFIN = 0.2 V_{pp} + 1.024 V dc at −3 dB		1.4		MHz

NOTES: 11. Reference input voltages greater than V_{DD}/2 will cause output saturation for large DAC codes.
12. Reference feedthrough is measured at the DAC output with an input code = 0x000 and a $V_{ref(REFIN)}$ input = 1.024 V dc + 1 V_{pp} at 1 kHz.

digital inputs (D0 − D11, $\overline{CS}$, $\overline{WE}$, $\overline{LDAC}$, $\overline{PD}$)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	High-level digital input current	$V_I = V_{DD}$			1	µA
I_{IL}	Low-level digital input current	V_I = 0 V			−1	µA
C_i	Input capacitance			8		pF

power supply

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{DD}	Power supply current	No load, All inputs 0 V or V_{DD}	5-V Supply		1.6	3	mA
			3-V Supply		1.44	2.7	mA
	Power down supply current				0.01	10	µA

operating characteristics over recommended operating free-air temperature range, supply voltages, and reference voltages (unless otherwise noted)

analog output dynamic performance

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
SR	Slew rate	C_L = 100 pF, R_L = 10 kΩ, Code 32 to code 4095, Code 4095 to code 32,	$V_{ref(REFIN)}$ = 2.048 V, 1.024 V, V_O from 10% to 90% 90% to 10%	5-V Supply	8	12		V/µs
				3-V Supply	6	9		V/µs
t_s	Output settling time (full scale)	To ±0.5 LSB, R_L = 10 kΩ,	C_L = 100 pF, See Note 13			1	3	µs
	Glitch energy	DIN = all 0s to all 1s				5		nV−s
S/N	Signal to noise	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF,	f_{OUT} = 1 kHz, R_L = 10 kΩ T_A = 25°C, See Note 14	5-V Supply	65	78		dB
S/(N+D)	Signal to noise + distortion	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF,	f_{OUT} = 1 kHz, R_L = 10 kΩ, T_A = 25°C, See Note 14	5-V Supply	58	67		dB
				3-V Supply	58	69		dB
	Total harmonic distortion	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF,	f_{OUT} = 1 kHz, R_L = 10 kΩ, T_A = 25°C, See Note 14			−68	−60	dB
	Spurious free dynamic range	f_s = 480 kSPS, BW = 20 kHz, C_L = 100 pF,	f_{OUT} = 1 kHz, R_L = 10 kΩ, T_A = 25°C, See Note 14		60	72		dB

NOTES: 13. Settling time is the time for the output signal to remain within ±0.5 LSB of the final measured value for a digital input code change of 0x020 to 0x3DF or 0x3DF to 0x020. Limits are ensured by design and characterization, but are not production tested.
14. 1 kHz sinewave generated by DAC, reference voltage = 1.024 V at 3 V and 2.048 V at 5 V.

timing requirement

digital inputs

		MIN	NOM	MAX	UNIT
$t_{su(CS-WE)}$	Setup time, $\overline{CS}$ low before positive $\overline{WE}$ edge	13			ns
$t_{su(D)}$	Setup time, data ready before positive $\overline{WE}$ edge	9			ns
$t_{h(D)}$	Hold time, data held after positive $\overline{WE}$ edge	0			ns
$t_{su(WE-LD)}$	Setup time, positive $\overline{WE}$ edge before $\overline{LDAC}$ low	0			ns
$t_{wh(WE)}$	Pulse width, $\overline{WE}$ high	25			ns
$t_{w(LD)}$	Pulse width, $\overline{LDAC}$ low	25			ns

PARAMETER MEASUREMENT INFORMATION

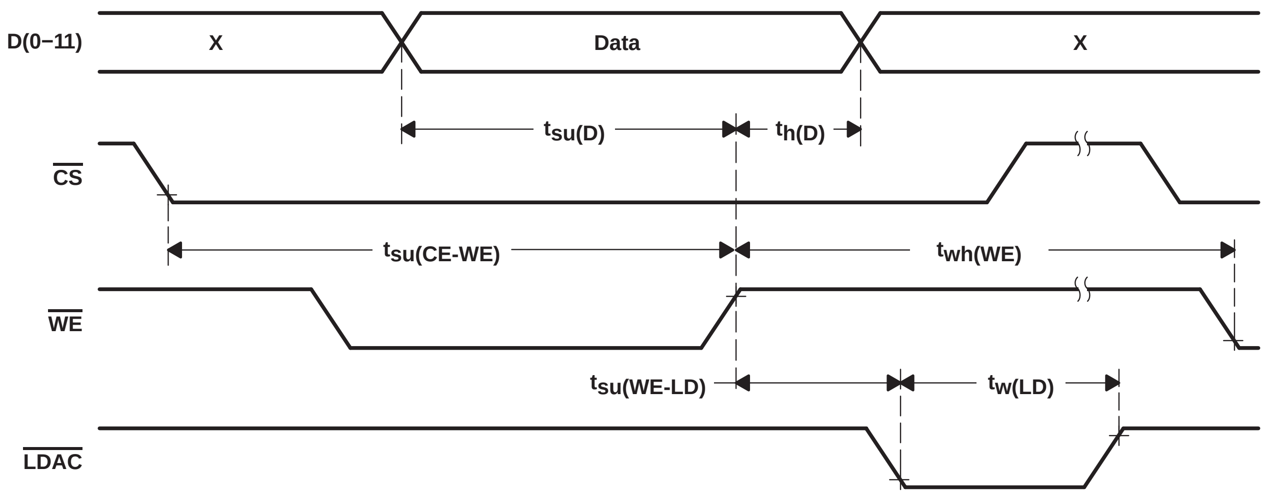


Figure 1. Timing Diagram

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT VOLTAGE vs LOAD

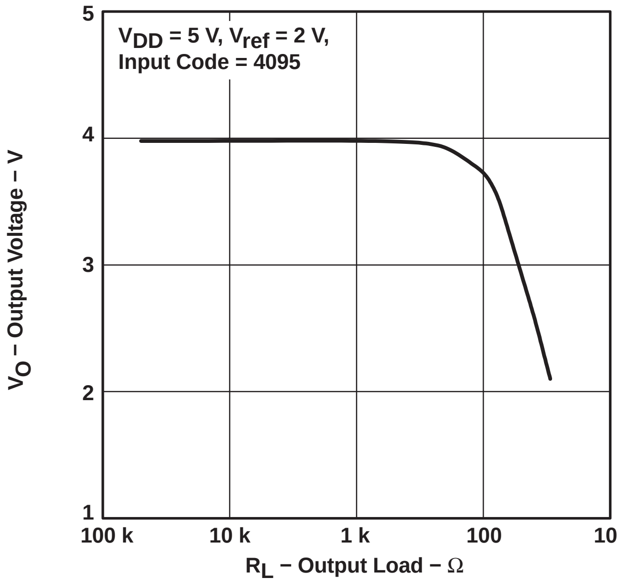


Figure 2

MAXIMUM OUTPUT VOLTAGE vs LOAD

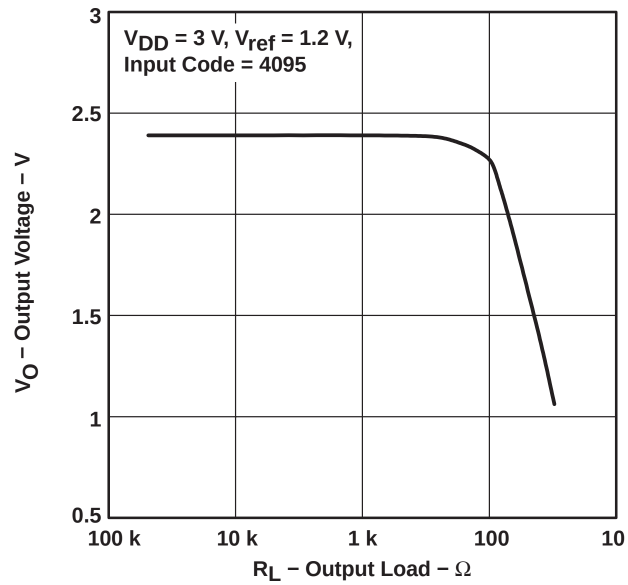


Figure 3

TOTAL HARMONIC DISTORTION vs LOAD

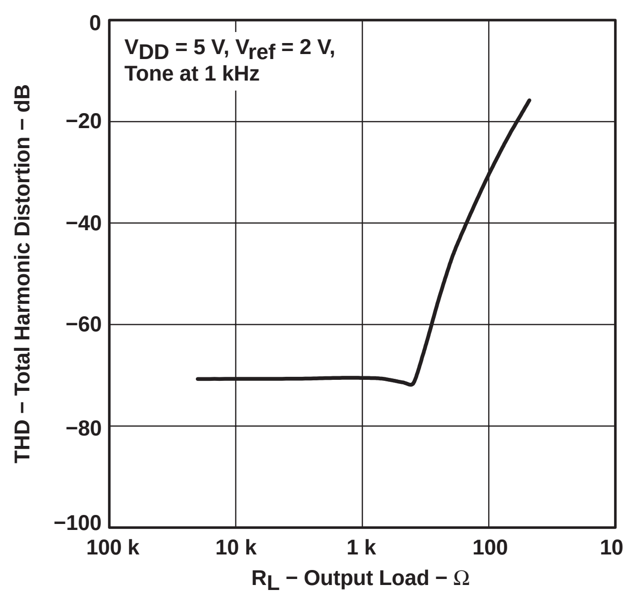


Figure 4

TOTAL HARMONIC DISTORTION vs FREQUENCY

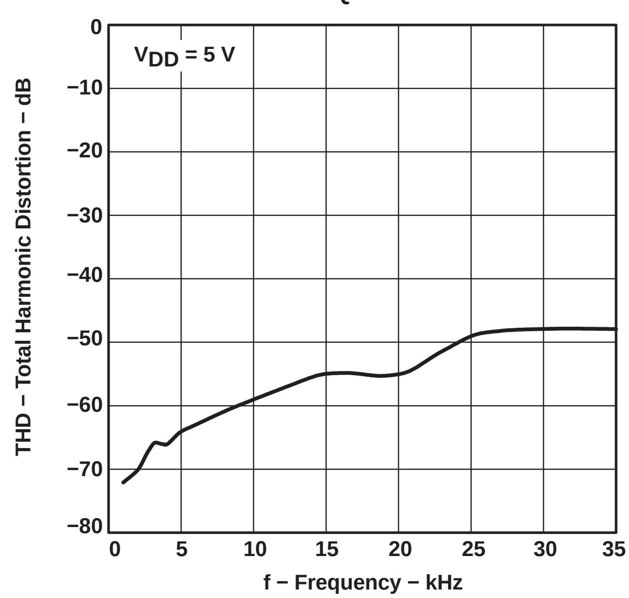


Figure 5

TYPICAL CHARACTERISTICS

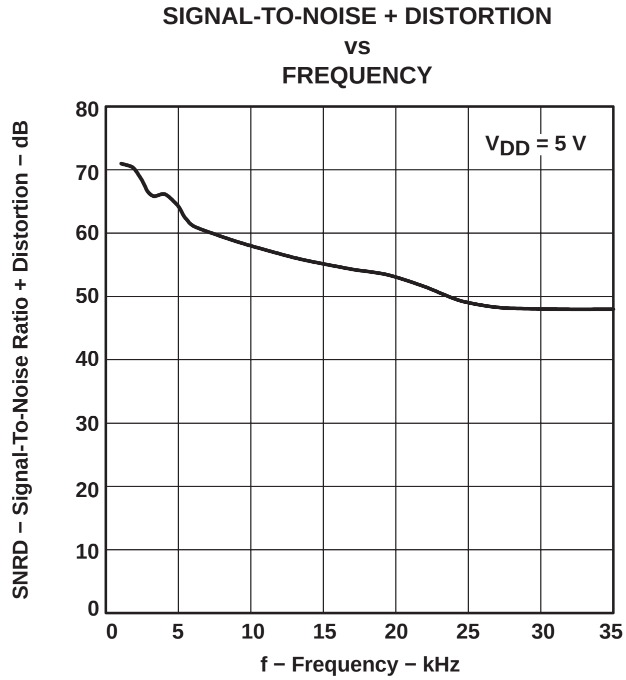


Figure 6

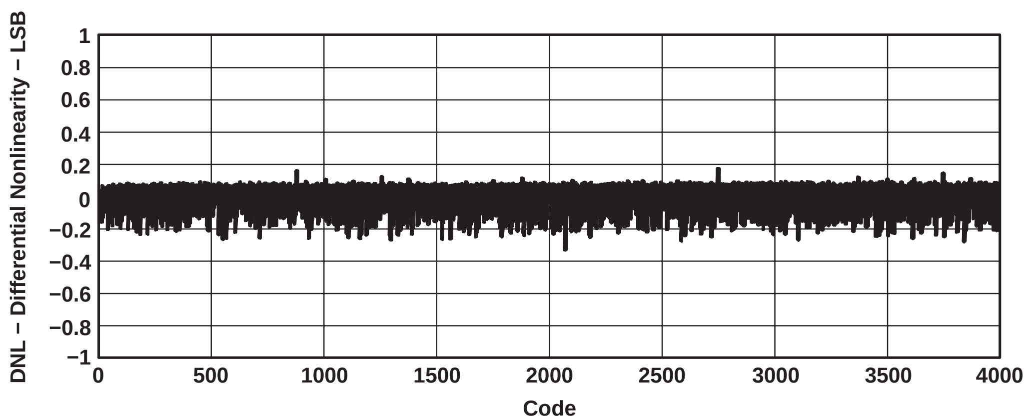


Figure 7. Differential Nonlinearity

TYPICAL CHARACTERISTICS

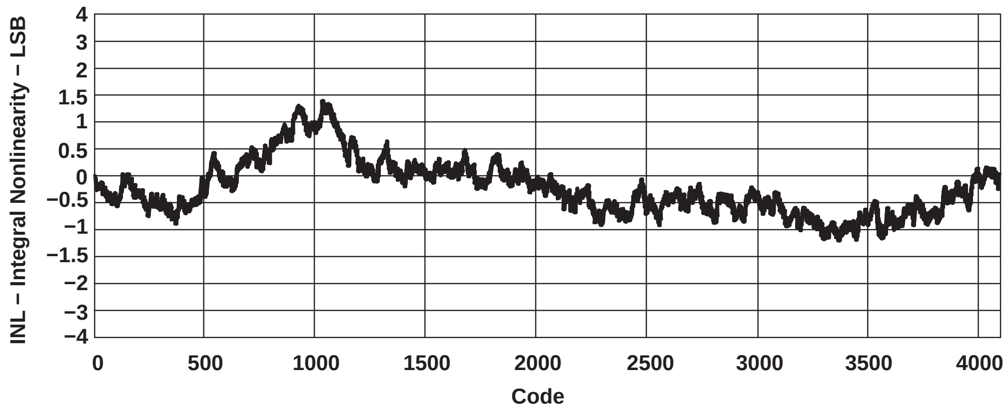


Figure 8. Integral Nonlinearity

**POWER DOWN SUPPLY CURRENT
vs
TIME**

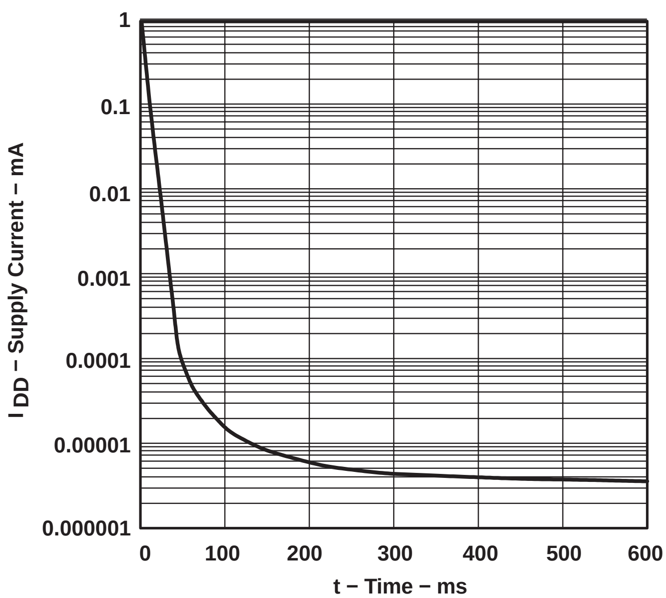


Figure 9

APPLICATION INFORMATION

definitions of specifications and terminology

integral nonlinearity (INL)

The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation of the output from the line between zero and full scale excluding the effects of zero code and full-scale errors.

differential nonlinearity (DNL)

The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal 1 LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.

zero-scale error (E_{ZS})

Zero-scale error is defined as the deviation of the output from 0 V at a digital input value of 0.

gain error (E_G)

Gain error is the error in slope of the DAC transfer function.

signal-to-noise ratio + distortion (S/N+D)

S/N+D is the ratio of the rms value of the output signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

spurious free dynamic range (SFDR)

SFDR is the difference between the rms value of the output signal and the rms value of the largest spurious signal within a specified bandwidth. The value for SFDR is expressed in decibels.

total harmonic distortion (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the fundamental signal and is expressed in decibels.

APPLICATION INFORMATION

linearity, offset, and gain error using single end supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive below ground and clamps the output at 0 V.

The output voltage remains at zero until the input code value produces a sufficient positive output voltage to overcome the negative offset voltage, resulting in the transfer function shown in Figure 10.

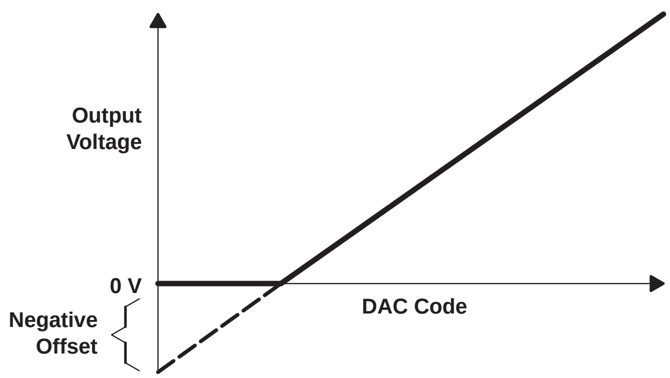


Figure 10. Effect of Negative Offset (Single Supply)

This offset error, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive below the ground rail.

For a DAC, linearity is measured between zero input code (all inputs 0) and full scale code (all inputs 1) after offset and full scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the offset is negative due to the breakpoint in the transfer function. So the linearity is measured between full scale code and the lowest code that produces a positive output voltage.

general function

The TLV5619 is a 12-bit, single supply DAC, based on a resistor string architecture. It consists of a parallel interface, a power down control logic, a resistor string, and a rail-to-rail output buffer. The output voltage (full scale determined by reference) is given by:

$$2\ \text{REF}\ \frac{\text{CODE}}{\text{0x1000}}\ [\text{V}]$$

Where REF is the reference voltage and CODE is the digital input value, range 0x000 to 0xFFF. A power on reset initially puts the internal latches to a defined state (all bits zero).

APPLICATION INFORMATION

parallel interface

The device latches data on the positive edge of $\overline{\text{WE}}$. It must be enabled with $\overline{\text{CS}}$ low. $\overline{\text{LDAC}}$ low updates the DAC with the value in the holding latch. $\overline{\text{LDAC}}$ is an asynchronous input and can be held low, if a separate update is not necessary. However, to control the DAC using the load feature, $\overline{\text{LDAC}}$ can be driven low after the positive $\overline{\text{WE}}$ edge.

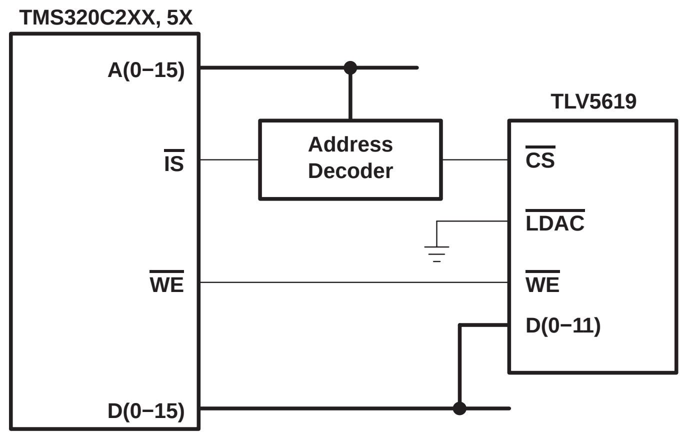


Figure 11. Proposed Interface Between TLV5619 and TMS320C2XX, 5X DSPs

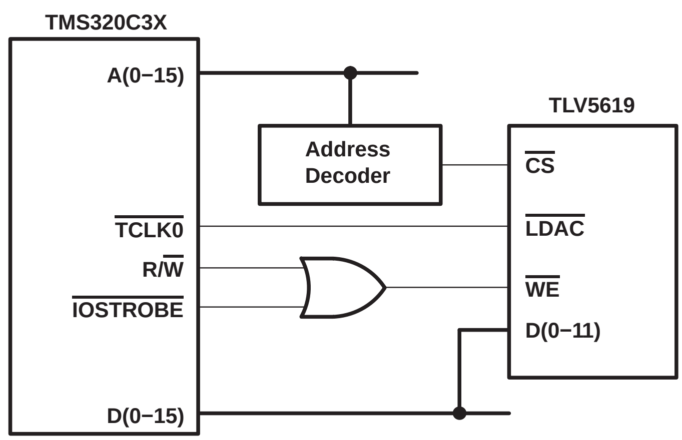


Figure 12. Proposed Interface Between TLV5619 and TMS320C3X DSPs

APPLICATION INFORMATION

TLV5619 interfaced to TMS320C203 DSP

hardware interface

Figure 13 shows an example of the connection between the TLV5619 and the TMS320C203 DSP. The only other device that is needed in addition to the DSP and the DAC is the 74AC138 address decoding circuit . Using this configuration, the DAC address is 0x0084 within the I/O memory space of the TMS320C203.

$\overline{LDAC}$ is held low so that the output voltage is updated with the rising $\overline{WE}$ edge. The power down mode is deactivated permanently by pulling $\overline{PD}$ to V_{DD}.

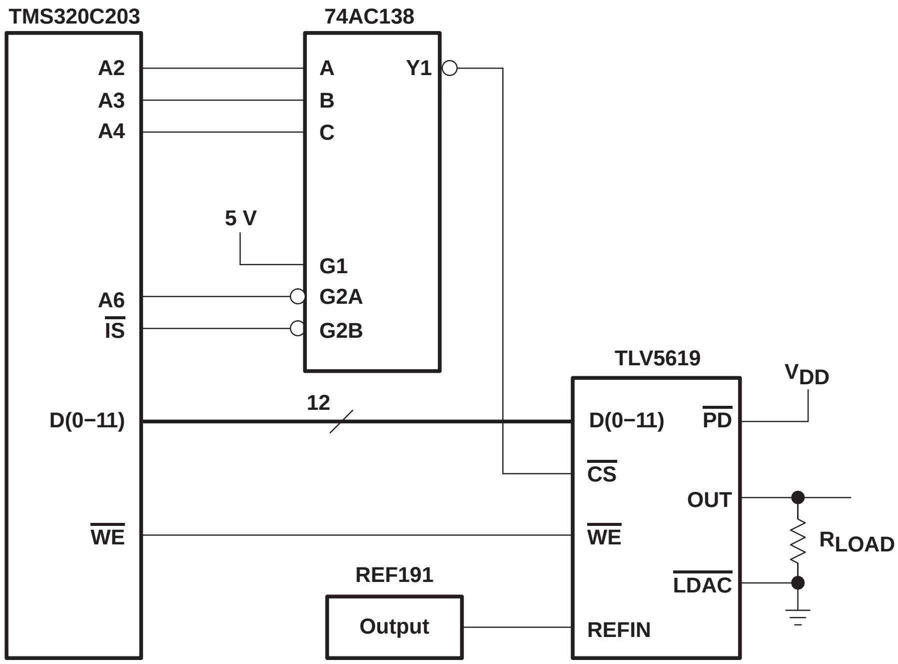


Figure 13. TLV5619 to TMS320C203 DSP Interface Connection

software

No setup procedure is needed to access the TLV5619. The output voltage can be set using one command:

```
out data_addr,  DAC_addr
```

Where `data_addr` points to the address location (in this example 0x0060) holding the new output voltage data and `DAC_addr` is the I/O space address of the TLV5619 (in this example 0x0084).

The following code shows, how to use the timer of the TMS320C203 as a time base to generate a voltage ramp with the TLV5619. A timer interrupt is generated every 205 µs. The corresponding interrupt service routine increments the output code (stored at 0x0060) for the DAC and writes the new code to the TLV5619. Only the 12 LSBs of the data in 0x0060 are used by the DAC, so that the resulting period of the saw waveform is:

$\tau = 4096 \times 205\ \text{E-6 s} = 0.84\ \text{s}$

APPLICATION INFORMATION

software listing

```
; File: ramp.asm
; Description: This program generates a ramp.

;------------- I/O and memory mapped regs -----------
          .include “regs.asm”
TLV5619   .equ   0084h
;------------ vectors ------------------------------
          .ps    0h
          b      start
          b      INT1
          b      INT23
          b      TIM_ISR

**********************************************************************
* Main Program
**********************************************************************

          .ps    1000h
          .entry
start:
          ldp    #0     ; set data page to 0
; disable interrupts
          setc   INTM   ; disable maskable interrupts
          splk   #0ffffh,  IFR
          splk   #0004h,   IMR

; set up the timer
          splk   #0000h,   60h
          splk   #0042h,   61h
          out    61h, PRD
          out    60h, TIM
          splk   #0c2fh,   62h
          out    62h,   TCR

; enable interrupts
          clrc   INTM   ; enable maskable interrupts

; loop forever!
next      idle          ; wait for interrupt

          b         next
; all else fails stop here
done      b         done ; hang there

**********************************************************************
* Interrupt Service Routines
**********************************************************************

INT1:     ret           ; do nothing and return

INT23:    ret           ; do nothing and return

TIM_ISR:
       ; useful code
          add       #1h  ; increment accumulator
          sacl      60h
          out          60h, TLV5619  ; write to DAC
          clrc      intm ; re-enable interrupts
          ret            ; return from interrupt
          .end
```

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLV5619QDWREP	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/03615-01XE	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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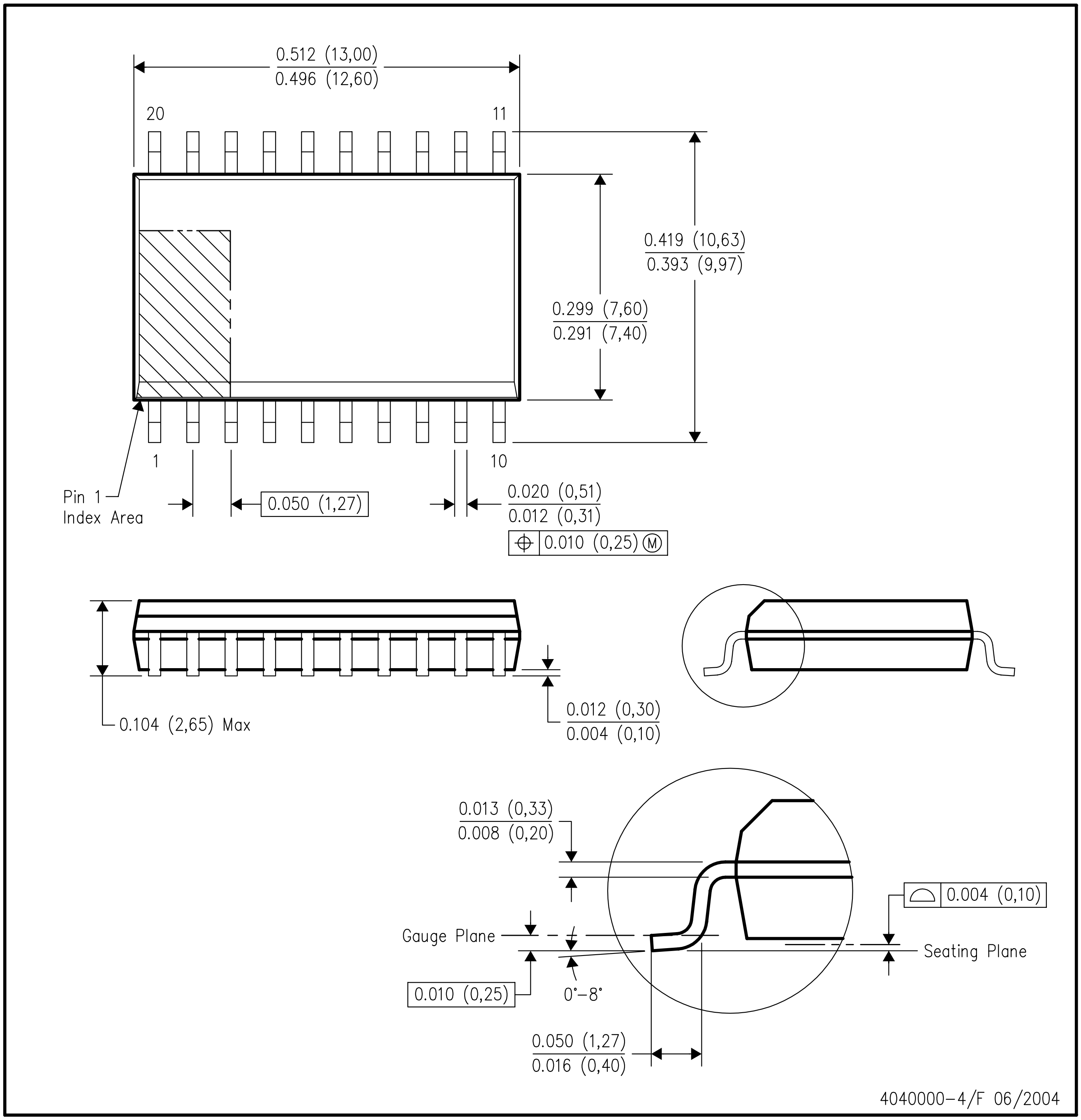
DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.