



STW45NM50

N-channel 550 V @ T_{jmax} , 0.08 Ω , 45 A, TO-247
MDmesh™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on) max}	I _D
STW45NM50FD	500 V	< 0.1 Ω	45 A

- 100% avalanche tested
- High dv/dt and avalanche capabilities
- Low input capacitance and gate charge
- Low gate input resistance

Application

- Switching applications

Description

The MDmesh™ is a new revolutionary Power MOSFET technology that associates the Multiple Drain process with the company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competitor's products.

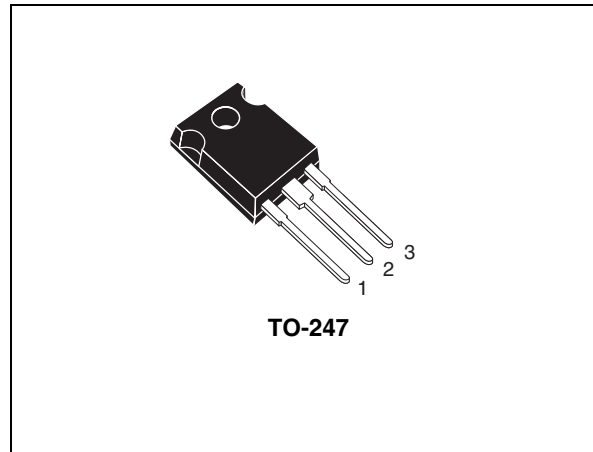


Figure 1. Internal schematic diagram

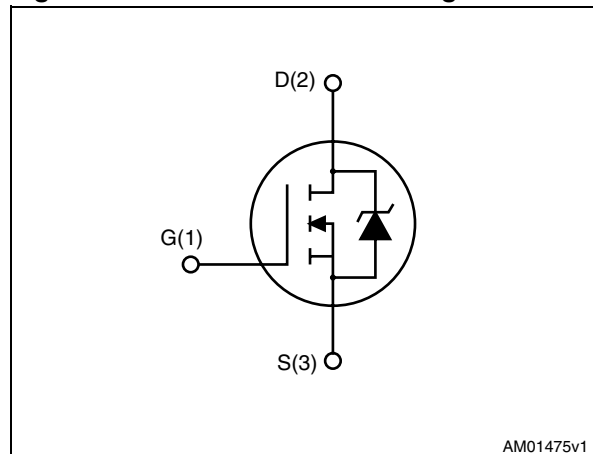


Table 1. Device summary

Order code	Marking	Package	Packaging
STW45NM50	W45NM50	TO-247	Tube

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	45	A
I_D	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	28.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	417	W
	Derating factor	2.08	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	-65 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2. $I_{SD} \leq 45\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\%V_{(BR)DSS}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.3	$^\circ\text{C}/\text{W}$
R_{thj-a}	Thermal resistance junction-ambient max	30	$^\circ\text{C}/\text{W}$
T_I	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	20	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	810	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250 μA, V _{GS} = 0	500			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating, V _{DS} = Max rating @ 125 °C			10 100	μA μA
I _{GSS}	Gate body leakage current (V _{DS} = 0)	V _{GS} = ± 30 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	4	5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 22.5 A		0.08	0.1	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} > I _{D(on)} × R _{DS(on)max} I _D = 22.5 A	-	20		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	3700 610 80		pF pF pF
C _{oss eq.} ⁽²⁾	Equivalent output capacitance	V _{GS} = 0, V _{DS} = 0 to 400 V	-	325		pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	V _{DD} = 400 V, I _D = 45 A V _{GS} = 10 V <i>Figure 14</i>	-	87 23 42	117	nC nC nC
R _G	Gate input resistance	f = 1 MHz Gate DC Bias = 0 test signal level = 20 mV open drain	-	1.7		Ω

1. Pulsed: pulse duration = 300 μs, duty cycle 1.5%
2. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=250\text{ V}$, $I_D=22.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ Figure 15	-	26.5 107.5	-	ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	$V_{DD}=400\text{ V}$, $I_D=45\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=10\text{ V}$ Figure 15	-	21.6 87.7 110.9	-	ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=45\text{ A}$, $V_{GS}=0$	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=45\text{ A}$, $V_{DD}=100\text{ V}$ $di/dt=100\text{ A}/\mu\text{s}$, (see Figure 18)	-	200 1600 16		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=45\text{ A}$, $T_j=150\text{ }^\circ\text{C}$ $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=100\text{ V}$, (see Figure 18)	-	324 4017 24.8		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

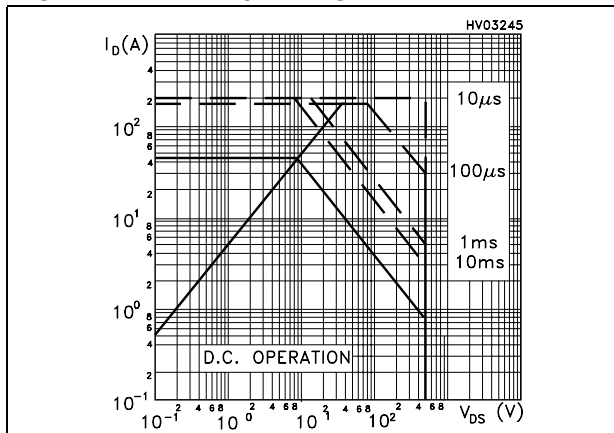


Figure 3. Thermal impedance

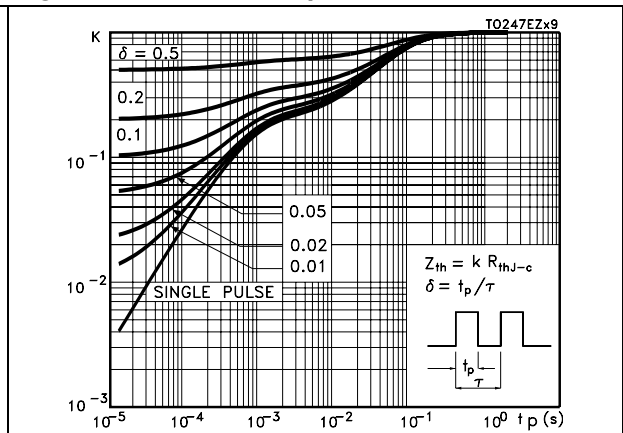


Figure 4. Output characteristics

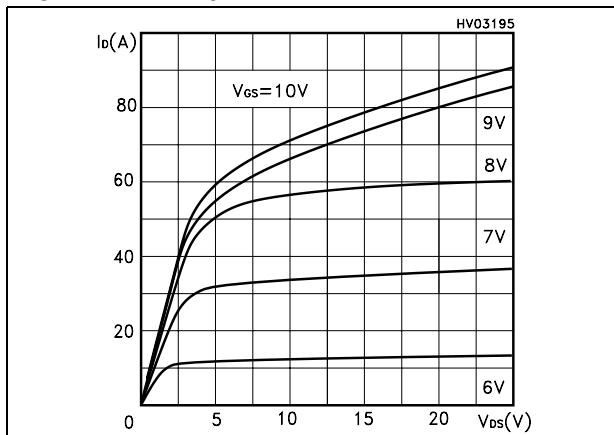


Figure 5. Transfer characteristics

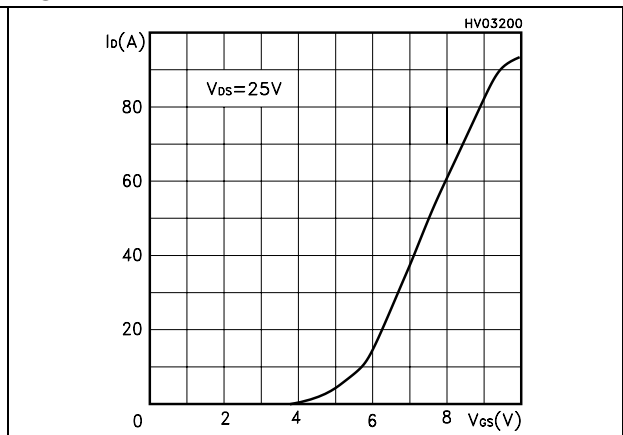


Figure 6. Transconductance

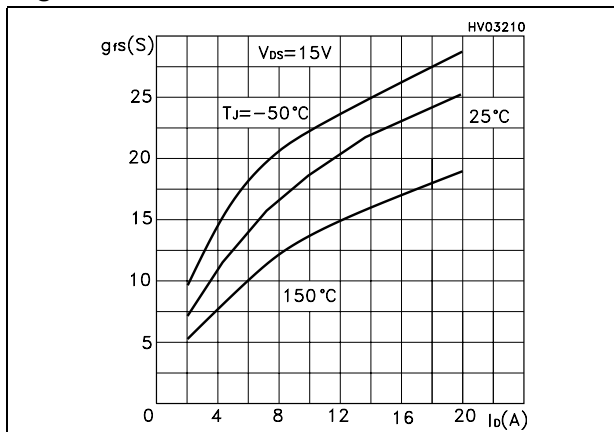


Figure 7. Static drain-source on resistance

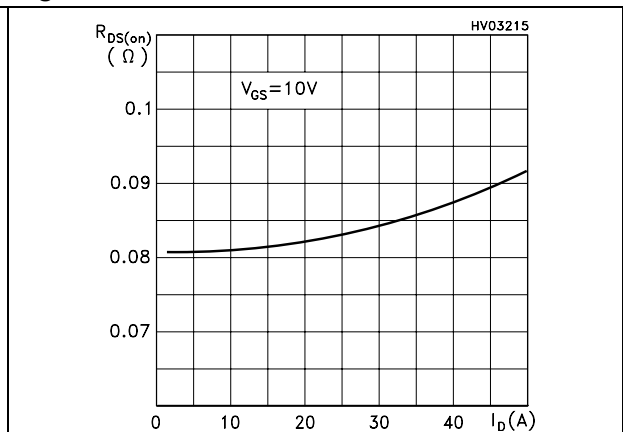


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

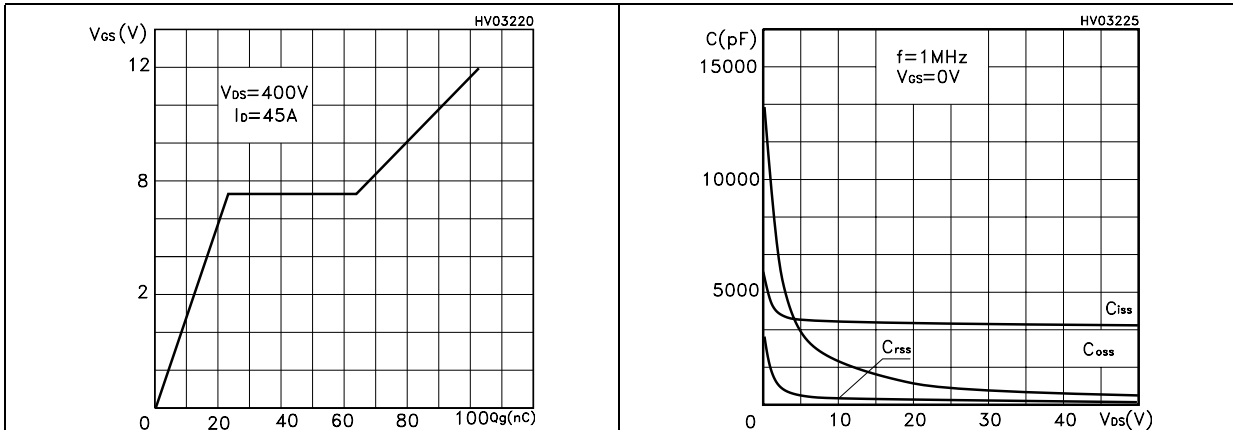


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

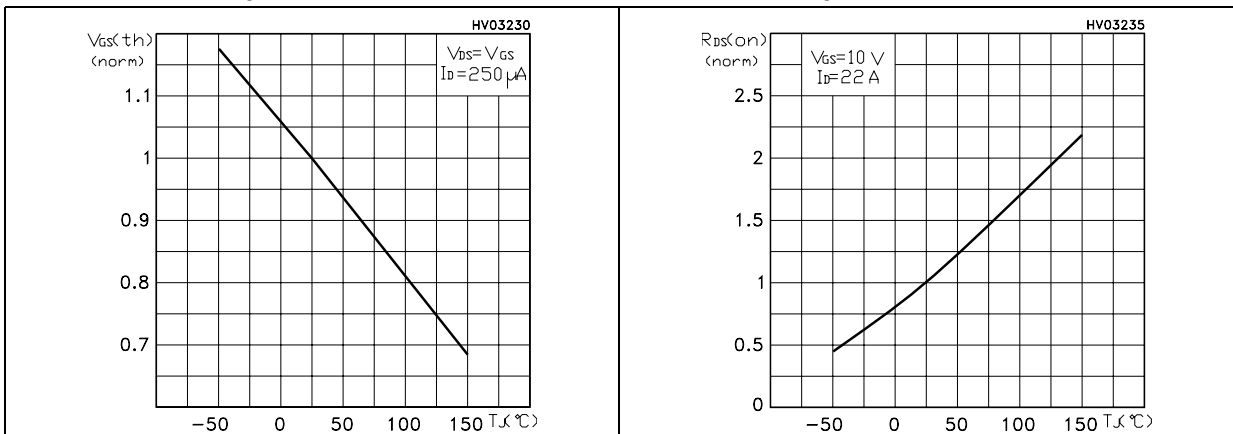
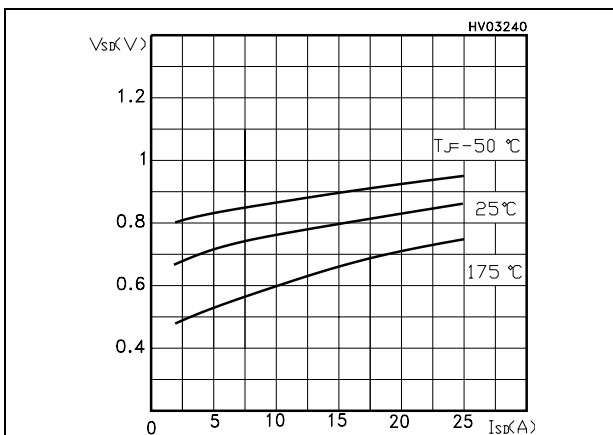


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

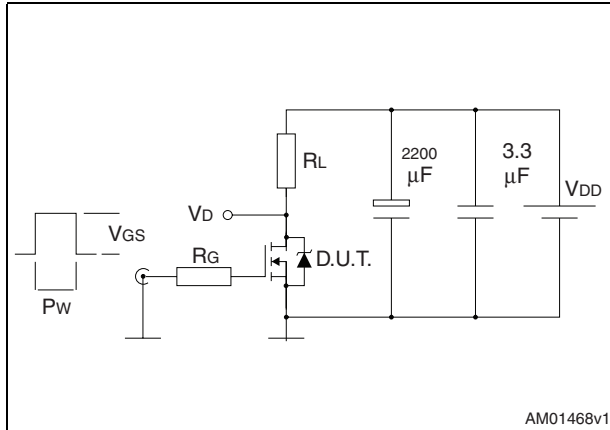


Figure 14. Gate charge test circuit

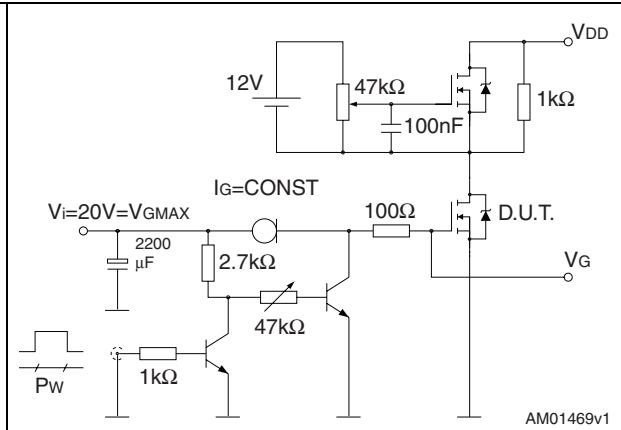


Figure 15. Test circuit for inductive load switching and diode recovery times

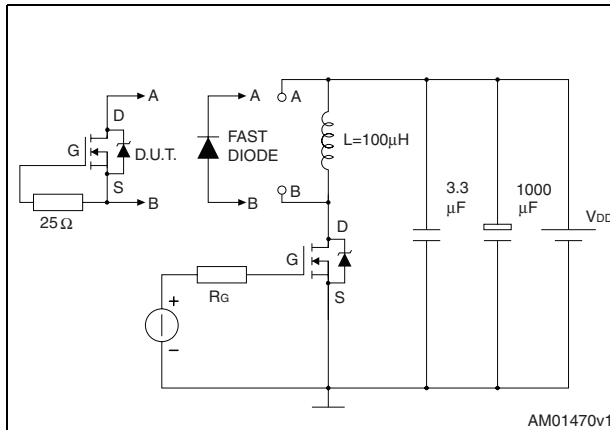


Figure 16. Unclamped inductive load test circuit

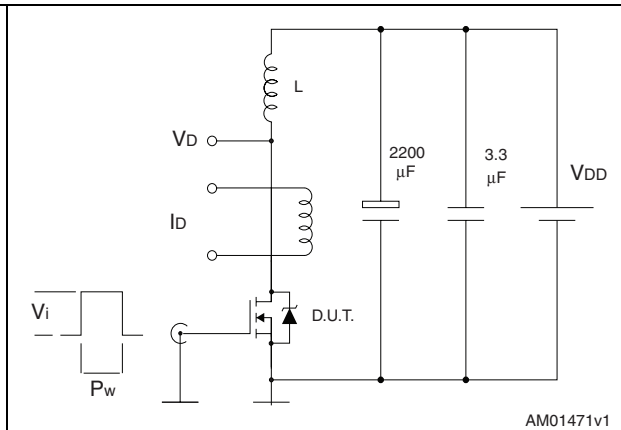


Figure 17. Unclamped inductive waveform

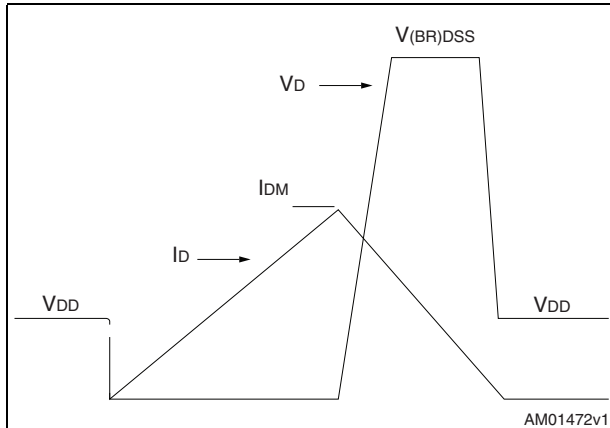
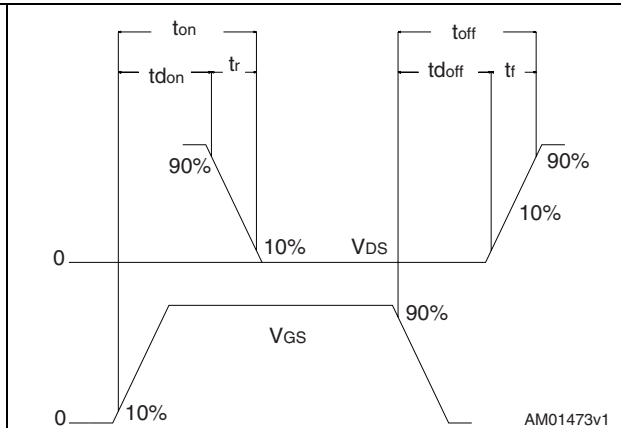


Figure 18. Switching time waveform

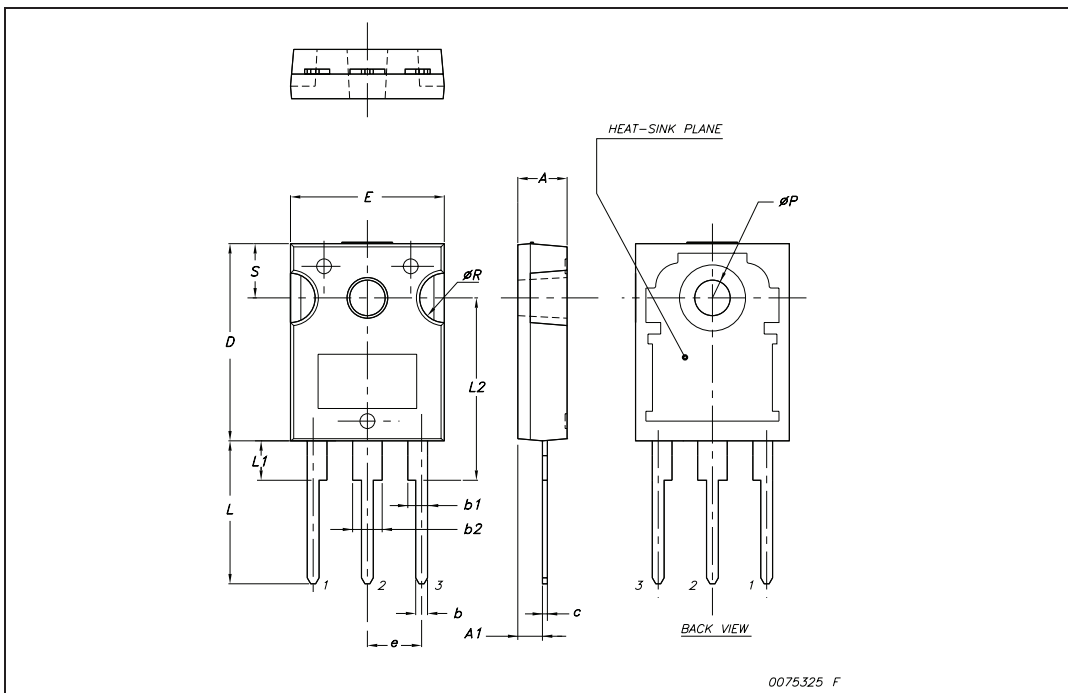


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
30-Mar-2005	4	Modified value on <i>Source drain diode</i>
23-Jul-2009	5	Modified values on <i>Switching times</i>

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