description

The SN75160B 8-channel general-purpose interface bus (GPIB) transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the passive-pullup or 3-state mode. If talk enable (TE) is high, these ports have the characteristics of passive-pullup outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 mA of sink current.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when $VCC = 0$. When combined with the SN75161B or SN75162B management bus transceivers, the pair provides the complete 16-wire interface for the IEEE-488 bus.

The SN75160B is characterized for operation from 0°C to 70°C.

Function Tables

```
<table>
<thead>
<tr>
<th>EACH DRIVER</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUTS</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>TE</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>L</td>
</tr>
</tbody>
</table>

H = high level, L = low level, X = irrelevant, Z = high impedance
† This is the high-impedance state of a normal 3-state output modified by the internal resistors to $VCC$ and GND.
```

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
SN75160B
OCTAL GENERAL-PURPOSE
INTERFACE BUS TRANSCEIVER

SLLS004B – OCTOBER 1985 – REVISED MAY 1995

logic symbol†

logic diagram (positive logic)

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
▽ Designates 3-state outputs
⚙ Designates passive-pullup outputs
schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

EQUIVALENT OF ALL INPUT/OUTPUT PORTS

Driver output $R_{eq} = 30 \ \Omega$ NOM
Receiver output $R_{eq} = 110 \ \Omega$ NOM
Circuit inside dashed lines is on the driver outputs only.

$R_{eq}$ = equivalent resistor

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC}$ (see Note 1) .......................................................... 7 V
Input voltage, $V_I$ .......................................................... 5.5 V
Low-level driver output current, $I_{OL}$ .................................................. 100 mA
Continuous total power dissipation ........................................ See Dissipation Rating Table
Operating free-air temperature range, $T_A$ ........................................... 0°C to 70°C
Storage temperature range, $T_{stg}$ .................................................. −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds .............. 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

<table>
<thead>
<tr>
<th>PACKAGE</th>
<th>$T_A \leq 25^\circ C$ POWER RATING</th>
<th>DERATING FACTOR ABOVE $T_A = 25^\circ C$</th>
<th>$T_A = 70^\circ C$ POWER RATING</th>
</tr>
</thead>
<tbody>
<tr>
<td>DW</td>
<td>1125 mW</td>
<td>9.0 mW/°C</td>
<td>720 mW</td>
</tr>
<tr>
<td>N</td>
<td>1150 mW</td>
<td>9.2 mW/°C</td>
<td>736 mW</td>
</tr>
</tbody>
</table>
recommended operating conditions

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, ( V_{CC} )</td>
<td></td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>High-level input voltage, ( V_{IH} )</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Low-level input voltage, ( V_{IL} )</td>
<td></td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>High-level output current, ( I_{OH} )</td>
<td>Bus ports with pullups active</td>
<td>–5.2</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Terminal ports</td>
<td>–800</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Low-level output current, ( I_{OL} )</td>
<td>Bus ports</td>
<td>48</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Terminal ports</td>
<td>16</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Operating free-air temperature, ( T_A )</td>
<td></td>
<td>0</td>
<td></td>
<td>70</td>
<td>°C</td>
</tr>
</tbody>
</table>

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP†</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IK} ) Input clamp voltage</td>
<td>( I_I = –18 ) mA</td>
<td>–0.8</td>
<td>–1.5</td>
<td>–1.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{hy} ) Hysteresis voltage ( (V_{IT+} – V_{IT–}) )</td>
<td>Bus</td>
<td>See Figure 8</td>
<td>0.4</td>
<td>0.65</td>
<td>V</td>
</tr>
<tr>
<td>( V_{OH} ) High-level output voltage</td>
<td>Terminal ( I_{OH} = –800 ) µA, ( TE ) at 0.8 V</td>
<td>2.7</td>
<td>3.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Bus ( I_{OH} = –5.2 ) mA, ( PE ) and ( TE ) at 2 V</td>
<td>2.5</td>
<td>3.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{OL} ) Low-level output voltage</td>
<td>Terminal ( I_{OL} = 16 ) mA, ( TE ) at 0.8 V</td>
<td>0.3</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Bus ( I_{OL} = 48 ) mA, ( TE ) at 2 V</td>
<td>0.35</td>
<td>0.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_I ) Input current at maximum</td>
<td>Terminal ( V_I = 5.5 ) V</td>
<td>0.2</td>
<td>100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>input voltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{IH} ) High-level input current</td>
<td>Terminal ( V_I = 2.7 ) V</td>
<td>0.1</td>
<td>20</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( I_{IL} ) Low-level input current</td>
<td>Terminal ( V_I = 0.5 ) V</td>
<td>–10</td>
<td>–100</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>( V_{I/O(bus)} ) Voltage at bus port</td>
<td>Driver disabled ( I_I(bus) = 0 )</td>
<td>2.5</td>
<td>3.0</td>
<td>3.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>( I_I(bus) = –12 ) mA</td>
<td></td>
<td></td>
<td>–1.5</td>
<td></td>
</tr>
<tr>
<td>( I_{I/O(bus)} ) Current into bus</td>
<td>Power on ( V_I(bus) = –1.5 ) V to 0.4 V</td>
<td>–1.3</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>port</td>
<td>Driver disabled ( V_I(bus) = 0.4 ) V to 2.5 V</td>
<td>0</td>
<td>–3.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_I(bus) = 2.5 ) V to 3.7 V</td>
<td>2.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_I(bus) = 3.7 ) V to 5 V</td>
<td>0</td>
<td>2.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>( V_I(bus) = 5 ) V to 5.5 V</td>
<td>0.7</td>
<td>2.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{OS} ) Short-circuit output</td>
<td>Terminal ( V_{CC} = 0 ), ( V_I(bus) = 0 ) to 2.5 V</td>
<td>–40</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>current</td>
<td>Bus ( V_I(bus) = 0 ) to 2.5 V</td>
<td>–15</td>
<td>–35</td>
<td>–75</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{OC} ) Supply current</td>
<td>No load Receivers low and enabled</td>
<td>70</td>
<td>90</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Receivers low and enabled 85</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{I/O(bus)} ) Bus-port capacitance</td>
<td>( V_{CC} = 0 ) to 5 V, ( f = 1 ) MHz</td>
<td>16</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

† All typical values are at \( V_{CC} = 5 \) V, \( T_A = 25 \)°C.
switching characteristics, $V_{CC} = 5$ V, $C_L = 15$ pF, $T_A = 25^\circ$C (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>FROM (INPUT)</th>
<th>TO (OUTPUT)</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{PLH}$</td>
<td>Terminal</td>
<td>Bus</td>
<td>$C_L = 30$ pF, See Figure 1</td>
<td>10</td>
<td>14</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>Bus</td>
<td>Terminal</td>
<td>$C_L = 30$ pF, See Figure 2</td>
<td>15</td>
<td>14</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLH}$</td>
<td>Bus</td>
<td>Terminal</td>
<td>$C_L = 30$ pF, See Figure 2</td>
<td>10</td>
<td>14</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHL}$</td>
<td>Terminal</td>
<td>Bus</td>
<td>$C_L = 30$ pF, See Figure 1</td>
<td>15</td>
<td>14</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>TE</td>
<td>BUS</td>
<td>See Figure 3</td>
<td>25</td>
<td>22</td>
<td>32</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PHZ}$</td>
<td>TE</td>
<td>Terminal</td>
<td>See Figure 4</td>
<td>20</td>
<td>19</td>
<td>30</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>TE</td>
<td>Terminal</td>
<td>See Figure 4</td>
<td>19</td>
<td>15</td>
<td>22</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PZH}$</td>
<td>Terminal</td>
<td>Bus</td>
<td>See Figure 5</td>
<td>13</td>
<td>14</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{PLZ}$</td>
<td>Terminal</td>
<td>Bus</td>
<td>See Figure 5</td>
<td>15</td>
<td>13</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{en}$</td>
<td>PE</td>
<td>Bus</td>
<td>See Figure 5</td>
<td>15</td>
<td>13</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{dis}$</td>
<td>PE</td>
<td>Bus</td>
<td>See Figure 5</td>
<td>15</td>
<td>13</td>
<td>20</td>
<td>ns</td>
</tr>
</tbody>
</table>
PARAMETER MEASUREMENT INFORMATION

NOTES:  
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, \( t_f \leq 6 \) ns, \( t_f \leq ns, Z_O = 50 \) Ω  
B. \( C_L \) includes probe and jig capacitance.

Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms

NOTES:  
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, \( t_f \leq 6 \) ns, \( t_f \leq ns, Z_O = 50 \) Ω  
B. \( C_L \) includes probe and jig capacitance.

Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms
PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT

NOTES:
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, τ_r ≤ 6 ns, τ_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms

NOTES:
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, τ_r ≤ 6 ns, τ_f ≤ ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms
PARAMETER MEASUREMENT INFORMATION

NOTES:
A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, \( t_r \leq 6 \text{ ns} \), \( t_f \leq 1 \text{ ns} \), \( Z_O = 50 \Omega \).
B. \( C_L \) includes probe and jig capacitance.

Figure 5. PE-to-Bus Pullup Test Circuit and Voltage Waveforms
TYPICAL CHARACTERISTICS

TERMINAL I/O PORTS
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

Figure 6

TERMINAL I/O PORTS
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

Figure 7

TERMINAL I/O PORTS
OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

Figure 8
TYPICAL CHARACTERISTICS

**Figure 9**

**GPIB I/O PORTS**

**HIGH-LEVEL OUTPUT VOLTAGE**

vs

**HIGH-LEVEL OUTPUT CURRENT**

\[ V_{OH} - \text{High-Level Output Voltage} - \text{V} \]

\[ I_{OH} - \text{High-Level Output Current} - \text{mA} \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_{A} = 25^\circ \text{C} \]

**Figure 10**

**GPIB I/O PORTS**

**LOW-LEVEL OUTPUT VOLTAGE**

vs

**LOW-LEVEL OUTPUT CURRENT**

\[ V_{OL} - \text{Low-Level Output Voltage} - \text{V} \]

\[ I_{OL} - \text{Low-Level Output Current} - \text{mA} \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_{A} = 25^\circ \text{C} \]

**Figure 11**

**GPIB I/O PORTS**

**OUTPUT VOLTAGE**

vs

**THERMAL INPUT VOLTAGE**

\[ V_{O} - \text{Output Voltage} - \text{V} \]

\[ V_{I} - \text{Thermal Input Voltage} - \text{V} \]

\[ V_{CC} = 5 \text{ V} \]

\[ \text{No Load} \]

\[ T_{A} = 25^\circ \text{C} \]

**Figure 12**

**GPIB I/O PORTS**

**CURRENT**

vs

**VOLTAGE**

\[ I_{I/O} - \text{Current} - \text{mA} \]

\[ V_{I/O} - \text{Voltage} - \text{V} \]

\[ V_{CC} = 5 \text{ V} \]

\[ T_{A} = 25^\circ \text{C} \]

The Unshaded Area Conforms to Paragraph 3.5.3 of IEEE Standard 488-1978
**PACKAGING INFORMATION**

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp (3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75160BDW</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>SN75160BDWE4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>SN75160BDWG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>SN75160BDWR</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>SN75160BDWRE4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>SN75160BDWRG4</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
</tr>
<tr>
<td>SN75160BN</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>20</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
</tr>
<tr>
<td>SN75160BNE4</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>20</td>
<td>20</td>
<td>Pb-Free (RoHS)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [http://www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

![Reel Dimensions Diagram](image)

#### TAPE DIMENSIONS

- **K0**: Dimension designed to accommodate the component width
- **B0**: Dimension designed to accommodate the component length
- **A0**: Dimension designed to accommodate the component thickness
- **W**: Overall width of the carrier tape
- **P1**: Pitch between successive cavity centers

#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

![Quadrant Assignments Diagram](image)

*All dimensions are nominal.*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75160BDWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>330.0</td>
<td>24.4</td>
<td>10.8</td>
<td>13.1</td>
<td>2.65</td>
<td>12.0</td>
<td>24.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SN75160BDWR</td>
<td>SOIC</td>
<td>DW</td>
<td>20</td>
<td>2000</td>
<td>346.0</td>
<td>346.0</td>
<td>41.0</td>
</tr>
</tbody>
</table>
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
D. Falls within JEDEC MS-013 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>VARIATION</th>
<th>AA</th>
<th>BB</th>
<th>AC</th>
<th>AD</th>
</tr>
</thead>
</table>

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

物流 JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

物流 The 20 pin end lead shoulder width is a vendor option, either half or full width.
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