

1.5-Gbps 2 × 2 LVDS CROSSPOINT SWITCH

FEATURES

- **Designed for Signaling Rates ⁽¹⁾ Up To 1.5 Gbps**
- **Total Jitter < 65 ps**
- **Pin-Compatible With SN65LVDS22 and SN65LVDM22**
- **25 mV of Receiver Input Threshold Hysteresis Over 0-V to 4-V Common-Mode Range**
- **Inputs Electrically Compatible With CML, LVPECL and LVDS Signal Levels**
- **Propagation Delay Times, 900 ps Maximum**
- **LVDT Integrates 110-Ω Terminating Resistor**
- **Offered in SOIC and TSSOP**

APPLICATIONS

- **10-G (OC-192) Optical Modules**
- **622-MHz Central Office Clock Distribution**
- **Wireless Basestations**
- **Low Jitter Clock Repeater/Multiplexer**
- **Protection Switching for Serial Backplanes**

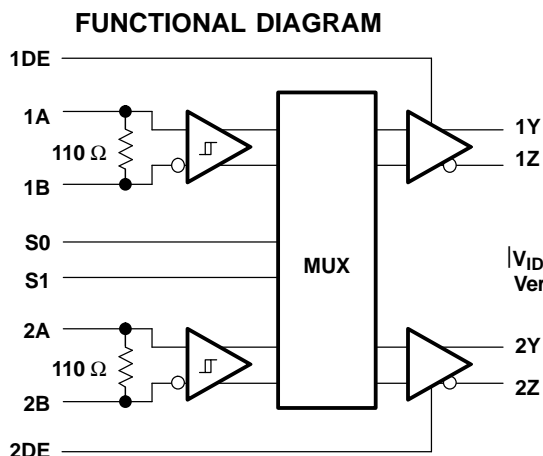
(1) The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

DESCRIPTION

The SN65LVDS122 and SN65LVDT122 are crosspoint switches that use low voltage differential signaling (LVDS) to achieve signaling rates as high as 1.5 Gbps. They are pin-compatible speed upgrades to the SN65LVDS22 and SN65LVDM22. The internal signal paths maintain differential signaling for high speeds and low signal skews. These devices have a 0-V to 4-V common-mode input range that accepts LVDS, LVPECL, or CML inputs. Two logic pins (S0 and S1) set the internal configuration between the differential inputs and outputs. This allows the flexibility to perform the following configurations: 2 × 2 crosspoint switch, 2:1 input multiplexer, 1:2 splitter or dual repeater/translator within a single device. Additionally, SN65LVDT122 incorporates a 110-Ω termination resistor for those applications where board space is a premium. Although these devices are designed for 1.5 Gbps, some applications at a 2-Gbps data rate can be supported depending on loading and signal quality.

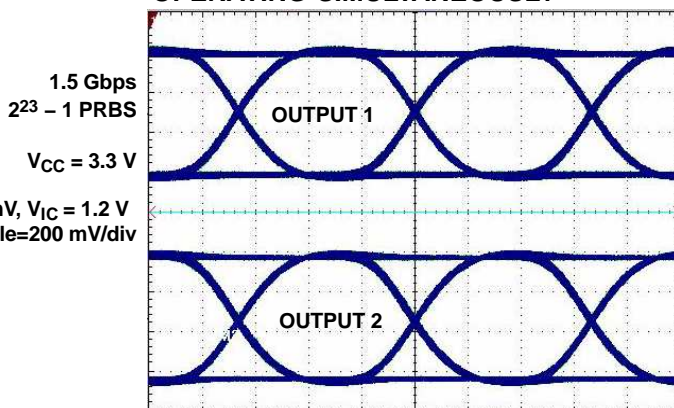
The intended application of this device is ideal for loopback switching for diagnostic routines, fanout buffering of clock/data distribution provide protection in fault-tolerant systems, clock multiplexing in optical modules, and for overall signal boosting over extended distances.

The SN65LVDS122 and SN65LVDT122 are characterized for operation from –40°C to 85°C.



Integrated Termination on SN65LVDT122 Only

EYE PATTERNS OF OUTPUTS OPERATING SIMULTANEOUSLY



Horizontal Scale = 200 ps/div



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

PACKAGE	TERMINATION RESISTOR	PART NUMBER ⁽¹⁾	SYMBOLIZATION
SOIC	No	SN65LVDS122D	LVDS122
SOIC	Yes	SN65LVDT122D	LVDT122
TSSOP	No	SN65LVDS122PW	LVDS122
TSSOP	Yes	SN65LVDT122PW	LVDT122

(1) Add the suffix R for taped and reeled carrier

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted⁽¹⁾

		SN65LVDS122, SN65LVDT122	
V_{CC}	Supply voltage range ⁽²⁾	–0.5 V to 4 V	
Voltage range	(A, B)	–0.7 V to 4.3 V	
	$ V_A - V_B $ (LVDT only)	1 V	
	(DE, S0, S1)	–0.5 V to 4 V	
	(Y, Z)	–0.5 V to 4 V	
ESD	Human Body Model ⁽³⁾	A, B, Y, Z, and GND	±4 kV
		All pins	±2 kV
	Charged-Device Model ⁽⁴⁾	All pins	±1500 V
Continuous power dissipation		See Dissipation Rating Table	
T_{stg}	Storage temperature range	–65°C to 150°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.7.
- (4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	S0, S1, 1DE, 2DE		4	V
V_{IL}	Low-level input voltage	S0, S1, 1DE, 2DE		0.8	V
$ V_{ID} $	Magnitude of differential input voltage	LVDS		1	V
		LVDT		0.8	
Input voltage (any combination of common-mode or input signals)		0	4		V
T_A	Operating free-air temperature	–40	85		°C

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ⁽¹⁾ ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ POWER RATING
PW	712 mW	6.2 mW/°C	340 mW
D	1002 mW	8.7 mW/°C	480 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT	
V _{IT+}	Positive-going differential input voltage threshold	See Figure 1 and Table 1			100	mV	
V _{IT-}	Negative-going differential input voltage threshold	See Figure 1 and Table 1	-100 ⁽²⁾			mV	
V _{ID(HYS)}	Differential input voltage hysteresis (V _{IT+} - V _{IT-})			25		mV	
I _{IH}	High-level input current	DE	V _{IH} = 2	-10	0	μA	
		S0, S1		0	20		
I _{IL}	Low-level input current	DE	V _{IL} = 0.8 V	-10	0	μA	
		S0, S1			20		
I _{CC}	Supply current	R _L = 100 Ω		80	100	mA	
		Disabled		35	45		
I _I	Input current (A or B inputs 'LVDS)	V _I = 0 V or 2.4 V, Other input at 1.2 V		-20	20	μA	
		V _I = 4 V, Other input at 1.2 V		0	33		
	Input current (A or B inputs 'LVDT)	V _I = 0 V or 2.4 V, Other input open		-40	40	μA	
		V _I = 4 V, Other input open		0	66		
I _{I(OFF)}	Input current (A or B inputs 'LVDS)	V _{CC} = 1.5 V, V _I = 0 V or 2.4 V, Other input at 1.2 V		-20	20	μA	
		V _{CC} = 1.5 V, V _I = 2.4 V or 4 V, Other input at 1.2 V		0	33		
	Input current (A or B inputs 'LVDT)	V _{CC} = 1.5 V, V _I = 0 V or 2.4 V, Other input open		-40	40	μA	
		V _{CC} = 1.5 V, V _I = 2.4 V or 4 V, Other input open		0	66		
I _{IO}	Input offset current (I _{IA} - I _{IB}) 'LVDS	V _{IA} = V _{IB} , 0 ≤ V _{IA} ≤ 4 V		-6	6	μA	
R _T	Termination resistance ('LVDT)	V _{ID} = 300 mV and 500 mV, V _{IC} = 0 V to 2.4 V		90	110	132	Ω
	Termination resistance ('LVDT with power-off)	V _{ID} = 300 mV and 500 mV, V _{CC} = 1.5 V, V _{IC} = 0 V to 2.4 V		90	110	132	
C _I	Differential input capacitance ('LVDT with power-off)	V _I = 0.4 sin(4E6πt) + 0.5 V			3	pF	
		Powered down (V _{CC} = 1.5 V)			3		

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) The algebraic convention in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OD}	Differential output voltage magnitude	See Figure 2	247	310	454	mV
Δ V _{OD}	Change in differential output voltage magnitude between logic states		-50		50	
V _{OC(SS)}	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
ΔV _{OC(SS)}	Change in steady-state common-mode output voltage between logic states		-50		50	mV
V _{OC(PP)}	Peak-to-peak common-mode output voltage			50	150	mV
I _{OS}	Short-circuit output current	V _{O(Y)} or V _{O(Z)} = 0 V	-24		24	mA
I _{OS(D)}	Differential short-circuit output current	V _{OD} = 0 V	-12		12	mA
I _{OZ}	High-impedance output current	V _{OD} = 600 mV		-1	1	μA
		V _O = 0 V or V _{CC}		-1	1	
C _O	Differential output capacitance	V _I = 0.4 sin(4E6πt) + 0.5 V			3	pF

(1) All typical values are at 25°C and with a 3.3-V supply.

TIMING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{SET}	Input to select setup time		0			ns
t_{HOLD}	Input to select hold time		0.5			ns
t_{SWITCH}	Select to switch output		1	2	2.6	ns

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM ⁽¹⁾	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	400	650	900	ps
t_{PHL}	Propagation delay time, high-to-low-level output		400	650	900	ps
t_r	Differential output signal rise time (20% - 80%)				280	ps
t_f	Differential output signal fall time (20% - 80%)				280	ps
$t_{sk(p)}$	Pulse skew ($ t_{PHL} - t_{PLH} $) ⁽²⁾			10	50	ps
$t_{sk(pp)}$	Part-to-part skew ⁽³⁾	$V_{ID} = 0.2\text{ V}$			100	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) ⁽⁴⁾	750 MHz clock input ⁽⁵⁾		1	2.2	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak) ⁽⁴⁾	750 MHz clock input ⁽⁶⁾		10	17	ps
$t_{jit(pp)}$	Peak-to-peak jitter ⁽⁴⁾	1.5 Gbps $2^{23}-1$ PRBS input ⁽⁷⁾		33	65	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak ⁽⁴⁾	1.5 Gbps 2^7-1 PRBS input ⁽⁸⁾		17	50	ps
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 5		6	8	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 5		6	8	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 5		4	6	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 5		4	6	ns
$t_{sk(o)}$	Output skew ⁽⁹⁾			15	40	ps

(1) All typical values are at 25°C and with a 3.3-V supply.

(2) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.

(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

(4) Jitter is specified by design and characterization. Stimulus jitter has been subtracted.

(5) Input voltage = $V_{ID} = 200\text{ mV}$, 50% duty cycle at 750 MHz, $t_r = t_f = 50\text{ ps}$ (20% to 80%), measured over 1000 samples.

(6) Input voltage = $V_{ID} = 200\text{ mV}$, 50% duty cycle at 750 MHz, $t_r = t_f = 50\text{ ps}$ (20% to 80%).

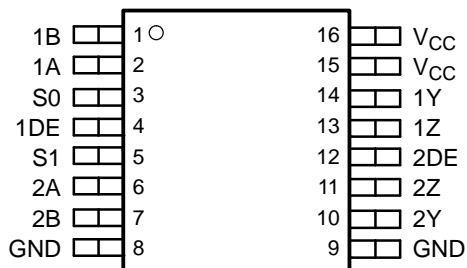
(7) Input voltage = $V_{ID} = 200\text{ mV}$, $2^{23}-1$ PRBS pattern at 1.5 Gbps, $t_r = t_f = 50\text{ ps}$ (20% to 80%), measured over 200 k samples.

(8) Input voltage = $V_{ID} = 200\text{ mV}$, 2^7-1 PRBS pattern at 1.5 Gbps, $t_r = t_f = 50\text{ ps}$ (20% to 80%).

(9) Output skew is the magnitude of the time delay difference between the outputs of a single device with all inputs tied together.

PIN ASSIGNMENT

D OR PW PACKAGE
(TOP VIEW)



Circuit Function Table

INPUTS ⁽¹⁾						OUTPUTS ⁽¹⁾		LOGIC DIAGRAM
1V _{ID}	2V _{ID}	S1	S0	1DE	2DE	1V _{OD}	2V _{OD}	
X	X	X	X	L	L	Z	Z	
> 100 mV	X	L	L	H	L	H	Z	
< -100 mV	X	L	L	H	L	L	Z	
< -100 mV	X	L	L	H	H	L	L	
> 100 mV	X	L	L	H	H	H	H	
> 100 mV	X	L	L	L	H	Z	H	
< -100 mV	X	L	L	L	H	Z	L	
> 100 mV	X	H	L	H	L	H	Z	
< -100 mV	X	H	L	H	L	L	Z	
< -100 mV	< -100 mV	H	L	H	H	L	L	
< -100 mV	> 100 mV	H	L	H	H	L	H	
> 100 mV	< -100 mV	H	L	H	H	H	L	
> 100 mV	> 100 mV	H	L	H	H	H	H	
X	> 100 mV	H	L	L	H	Z	H	
X	< -100 mV	H	L	L	H	Z	L	
X	> 100 mV	L	H	H	L	H	Z	
X	< -100 mV	L	H	H	L	L	Z	
X	> 100 mV	H	H	H	L	H	Z	
X	< -100 mV	H	H	H	L	L	Z	
< -100 mV	< -100 mV	H	H	H	H	L	L	
< -100 mV	> 100 mV	H	H	H	H	H	L	
> 100 mV	< -100 mV	H	H	H	H	L	H	
> 100 mV	> 100 mV	H	H	H	H	H	H	
> 100 mV	X	H	H	L	H	Z	H	
< -100 mV	X	H	H	L	H	Z	L	

(1) H = high level, L = low level, Z = high impedance, X = don't care

PARAMETER MEASUREMENT INFORMATION

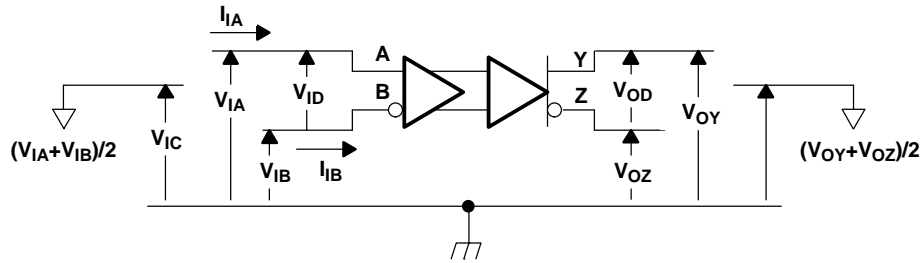


Figure 1. Voltage and Current Definitions

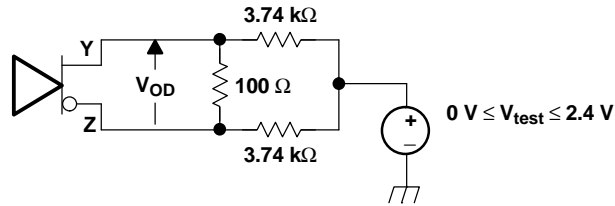
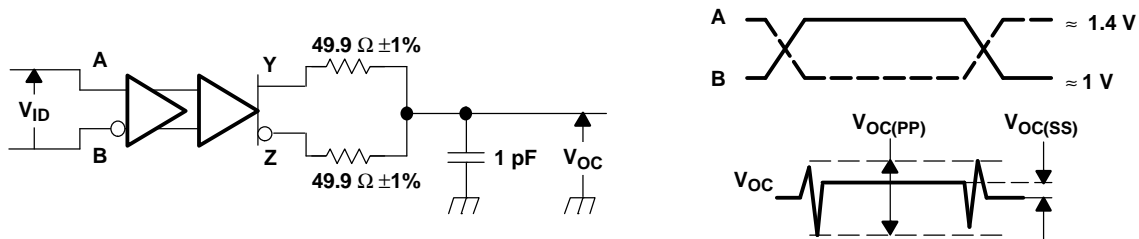
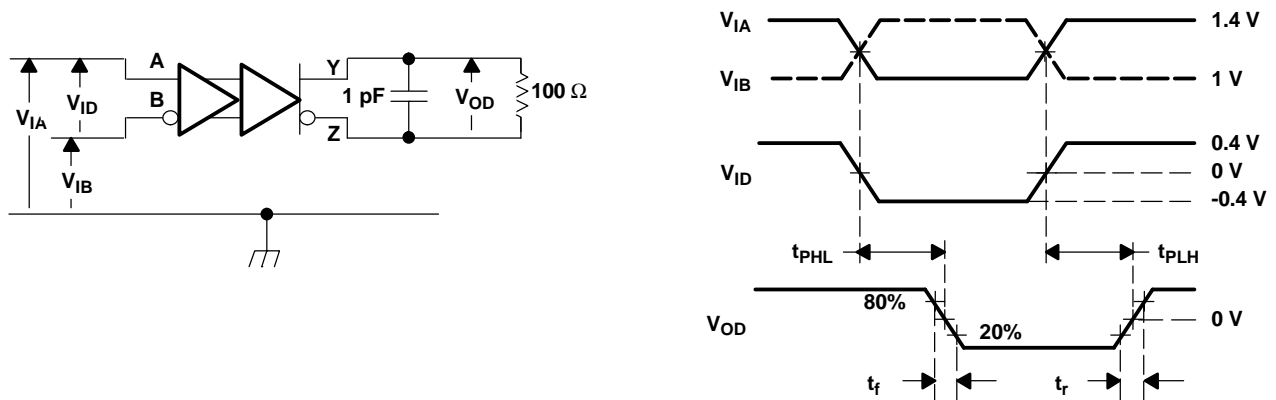


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns; $R_L = 100 \Omega$; C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 -dB bandwidth of at least 300 MHz.

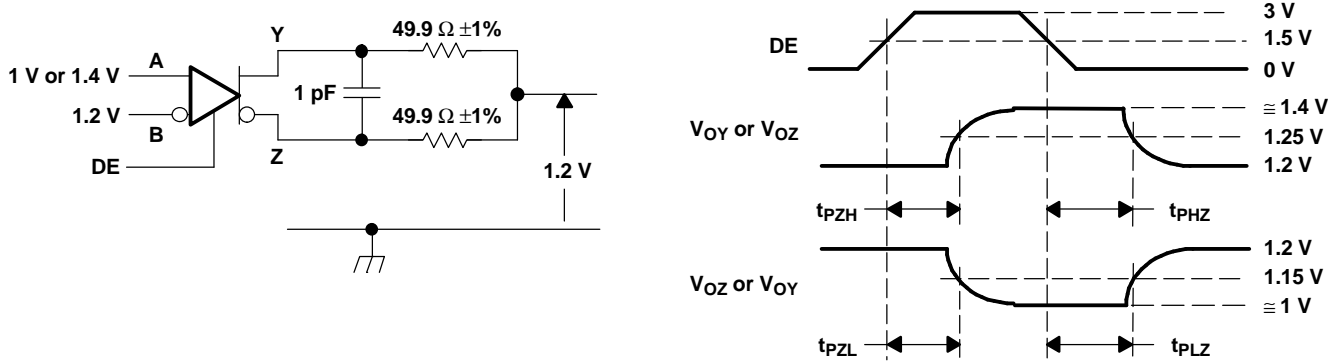
Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 0.25$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 4. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the D.U.T.

Figure 5. Enable and Disable Time Circuit and Definitions

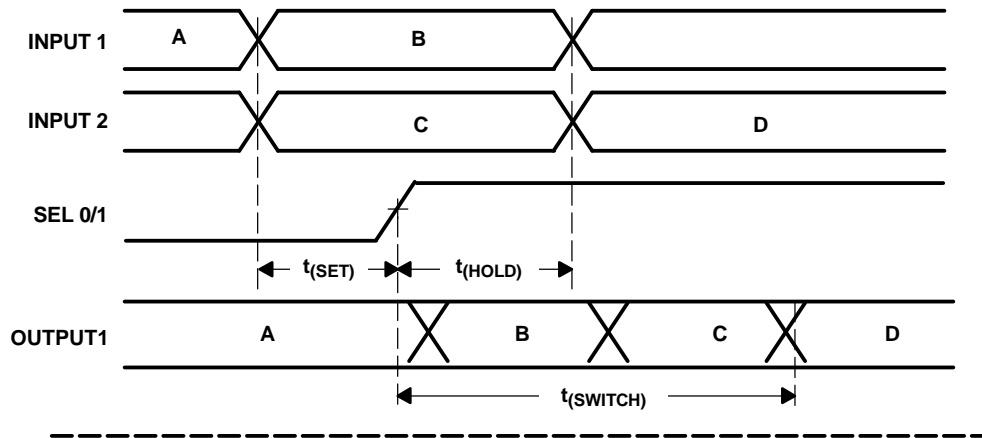


Figure 6. Example Switch, Setup, and Hold Times

PARAMETER MEASUREMENT INFORMATION (continued)

$t_{(SET)}$ and $t_{(HOLD)}$ times specify that data must be in a stable state before and after multiplex control switches.

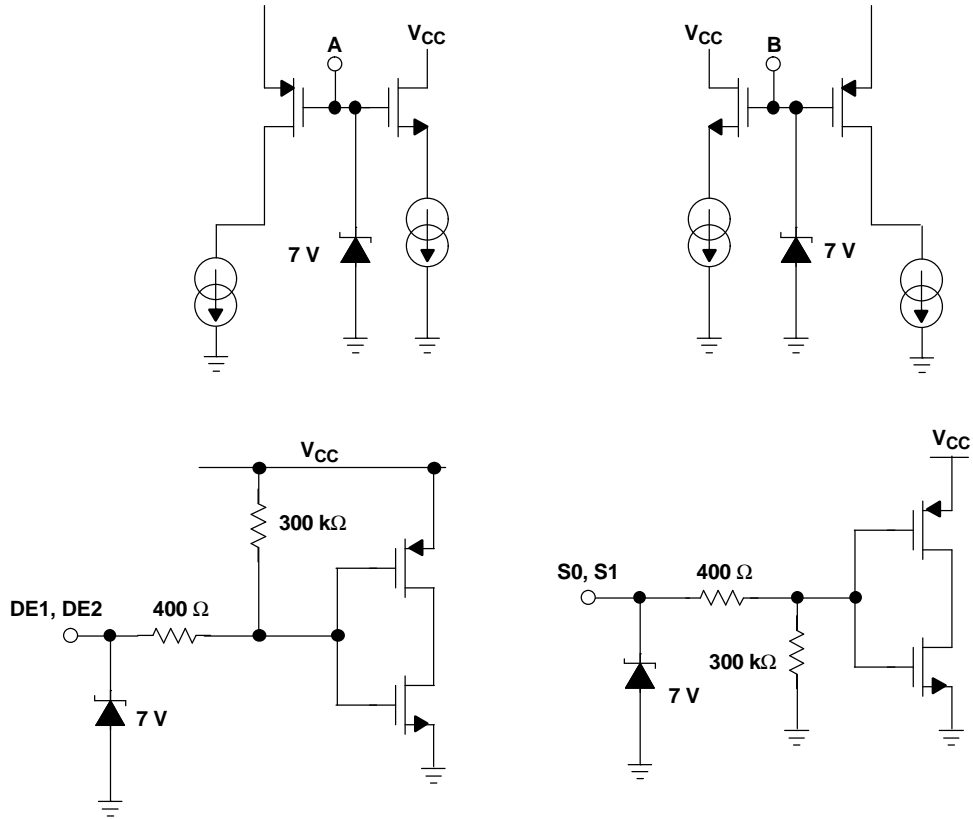
Table 1. Receiver Input Voltage Threshold Test

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	OUTPUT ⁽¹⁾
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
1.25 V	1.15 V	100 mV	1.2 V	H
1.15 V	1.25 V	-100 mV	1.2 V	L
4.0 V	3.9 V	100 mV	3.95 V	H
3.9 V	4.0 V	-100 mV	3.95 V	L
0.1 V	0.0 V	100 mV	0.05 V	H
0.0 V	0.1 V	-100 mV	0.05 V	L
1.7 V	0.7 V	1000 mV	1.2 V	H
0.7 V	1.7 V	-1000 mV	1.2 V	L
4.0 V	3.0 V	1000 mV	3.5 V	H
3.0 V	4.0 V	-1000 mV	3.5 V	L
1.0 V	0.0 V	1000 mV	0.5 V	H
0.0 V	1.0 V	-1000 mV	0.5 V	L

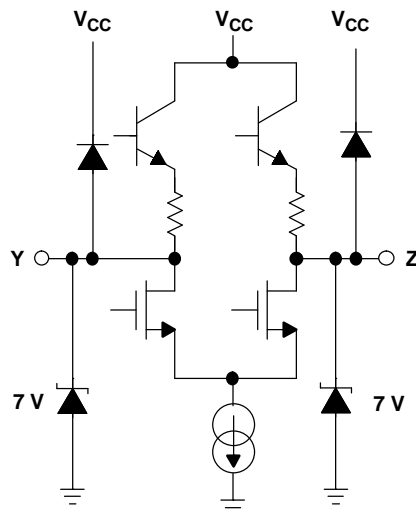
(1) H = high level, L = low level

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT LVDS122



OUTPUT LVDS122



TYPICAL CHARACTERISTICS

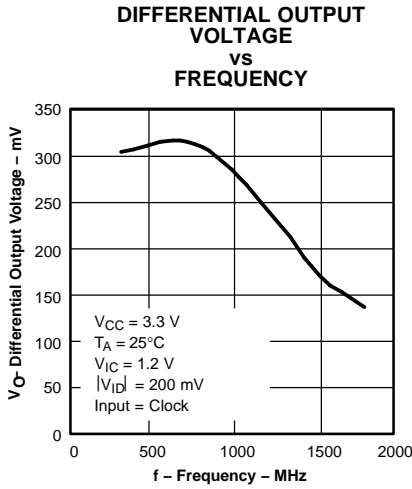


Figure 7.

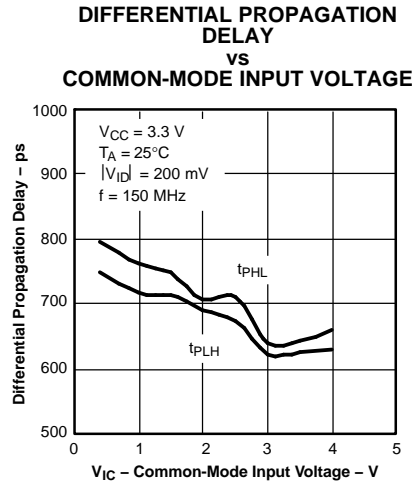


Figure 8.

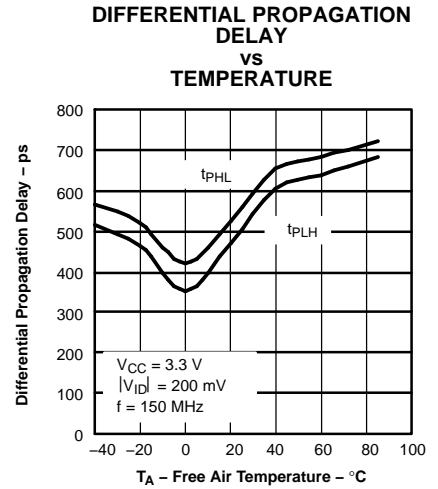


Figure 9.

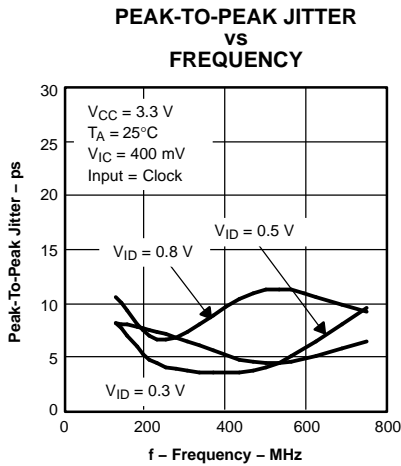


Figure 10.

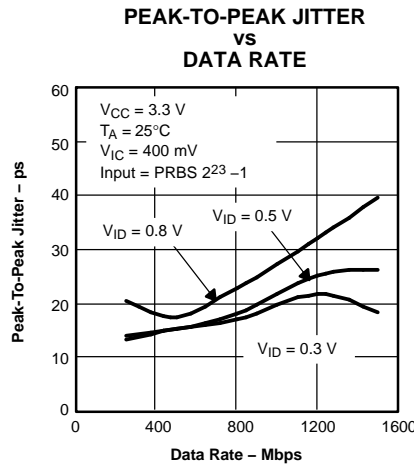


Figure 11.

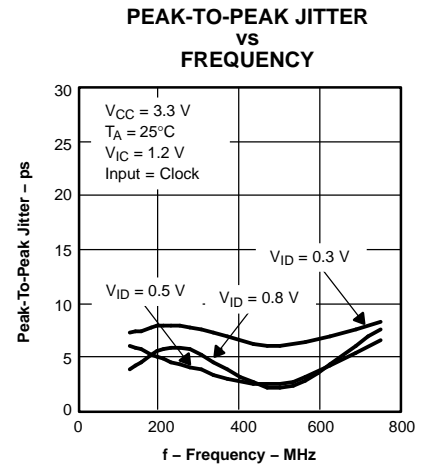


Figure 12.

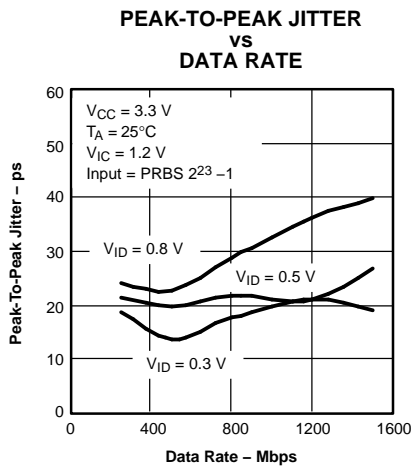


Figure 13.

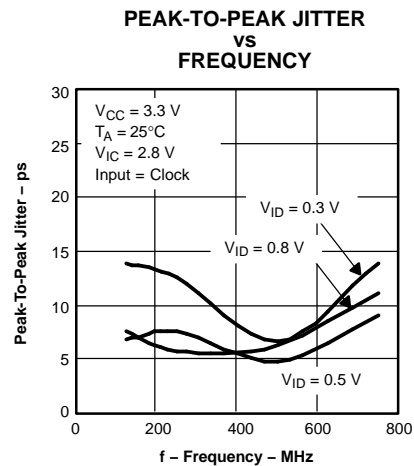


Figure 14.

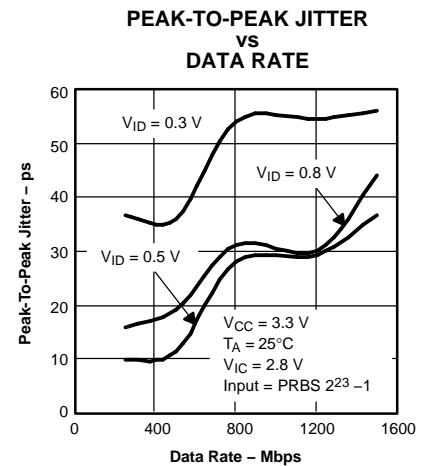


Figure 15.

TYPICAL CHARACTERISTICS (continued)

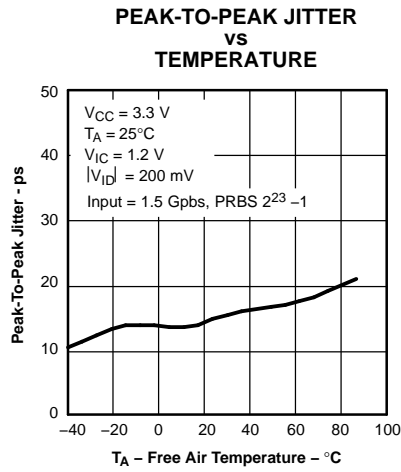


Figure 16.

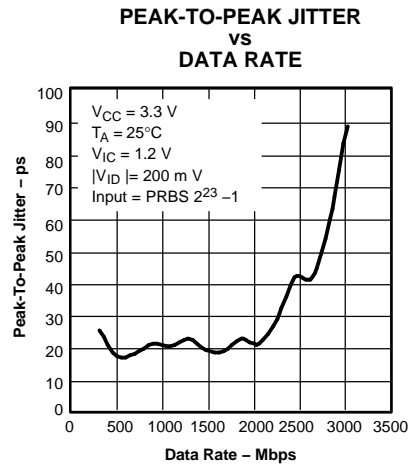
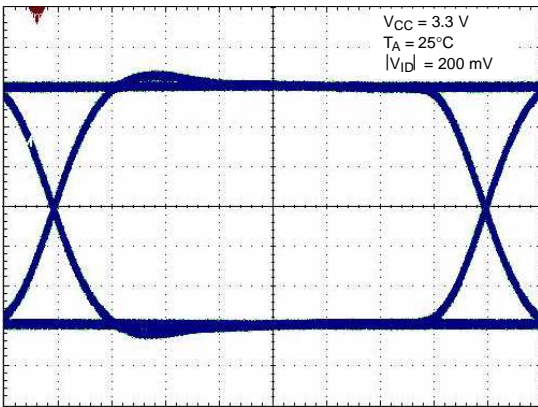


Figure 17.

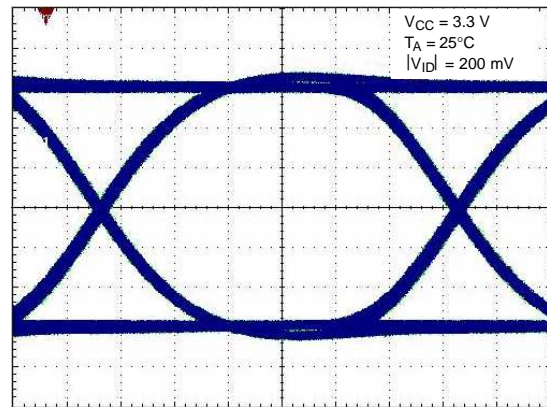
LVDS122
622 Mbps, 2²³-1 PRBS



Horizontal Scale= 200 ps/div
 LVPECL-to-LVDS

Figure 18.

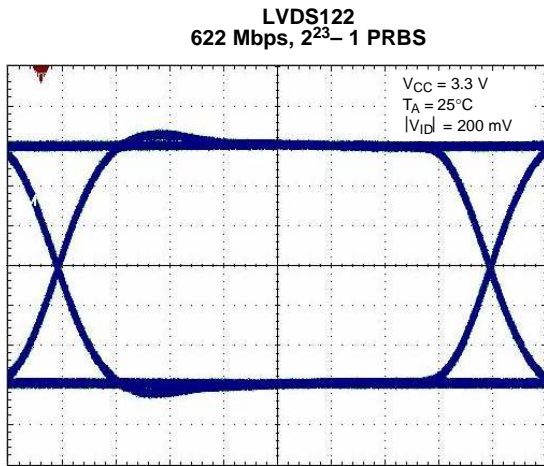
LVDS122
1.5 Gbps, 2²³-1 PRBS



Horizontal Scale= 100 ps/div
 LVPECL-to-LVDS

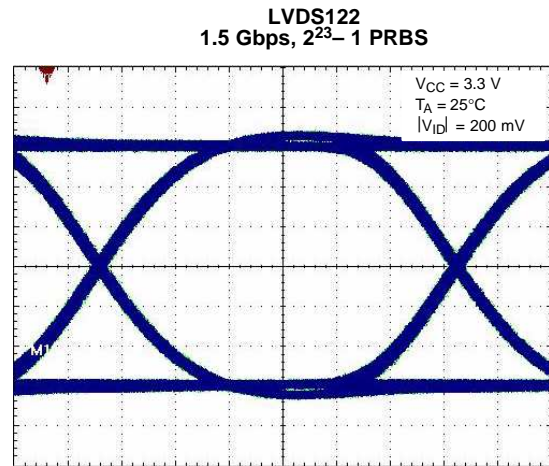
Figure 19.

TYPICAL CHARACTERISTICS (continued)



Horizontal Scale= 200 ps/div
LVDS-to-LVDS

Figure 20.



Horizontal Scale= 100 ps/div
LVDS-to-LVDS

Figure 21.

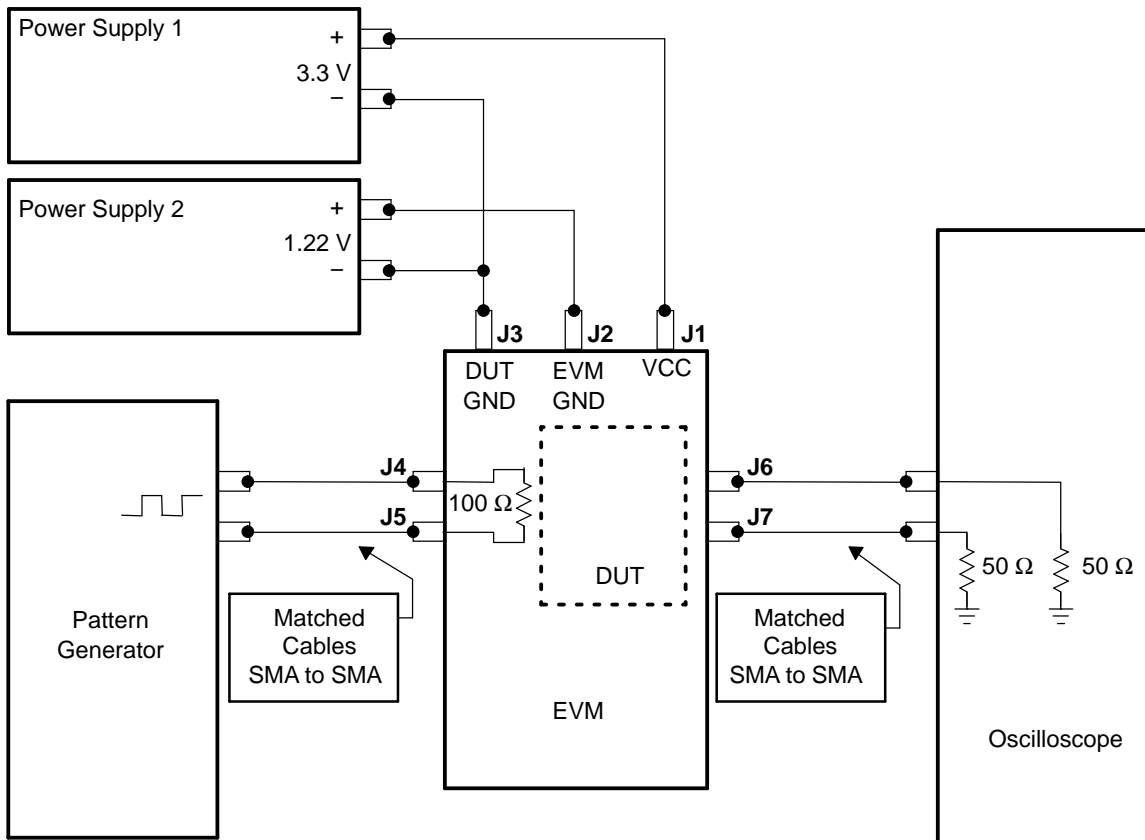


Figure 22. Jitter Setup Connections for SN65LVDS122

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

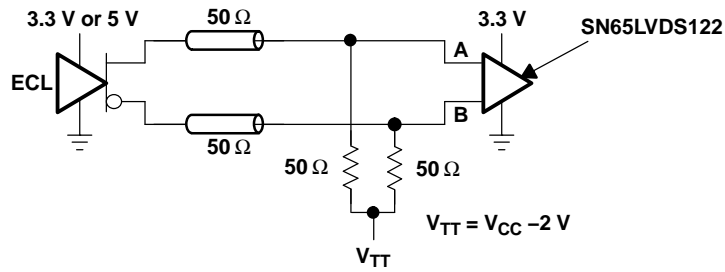


Figure 23. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

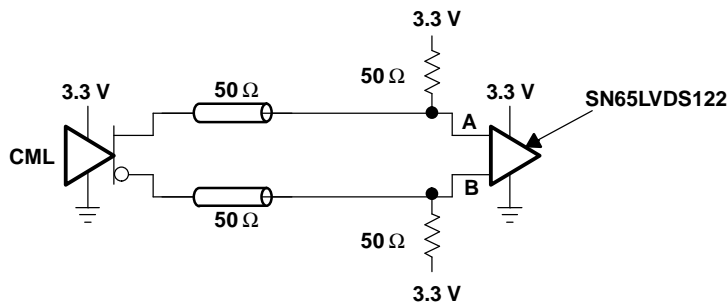


Figure 24. Current-Mode Logic (CML)

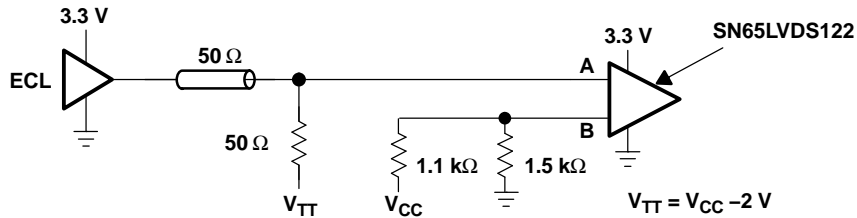


Figure 25. Single-Ended (LVPECL)

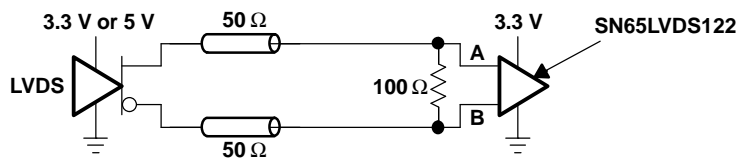


Figure 26. Low-Voltage Differential Signaling (LVDS)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS122D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS122	Samples
SN65LVDS122DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS122	Samples
SN65LVDS122DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS122	Samples
SN65LVDS122DRG4	ACTIVE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDS122PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS122	Samples
SN65LVDS122PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS122	Samples
SN65LVDS122PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS122	Samples
SN65LVDS122PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS122	Samples
SN65LVDT122D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT122	Samples
SN65LVDT122DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT122	Samples
SN65LVDT122PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT122	Samples
SN65LVDT122PWG4	ACTIVE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDT122PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT122	Samples
SN65LVDT122PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDT122	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS122DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS122PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDT122PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS122DR	SOIC	D	16	2500	367.0	367.0	38.0
SN65LVDS122PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDT122PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

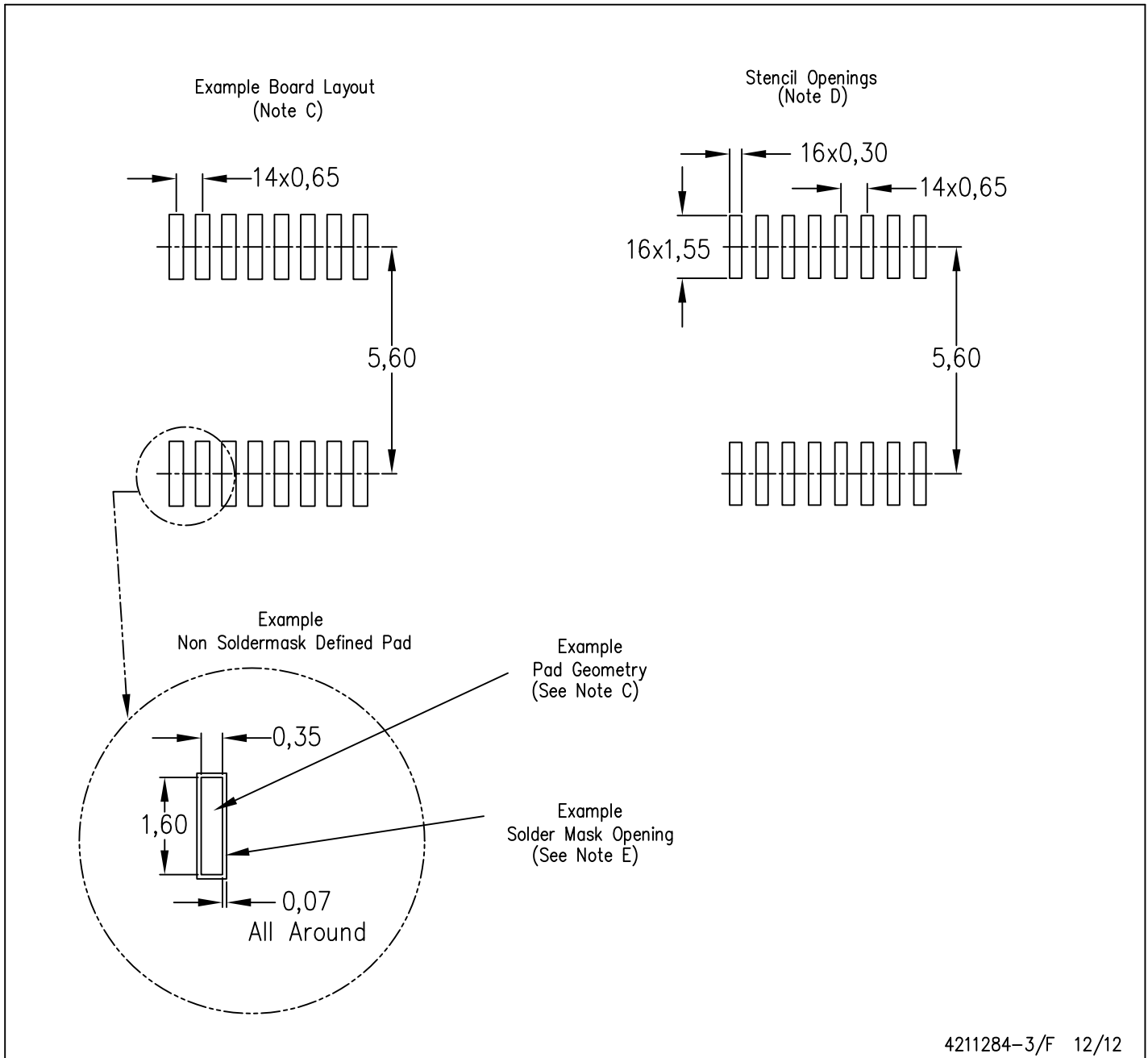


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com