

# PUSBMxX4-TL series

High-speed USB OTG ESD protection diode arrays

Rev. 3 — 14 June 2012

Product data sheet

## 1. Product profile

### 1.1 General description

PUSBMxX4-TL is a series of four 4-channel ElectroStatic Discharge (ESD) diode arrays for USB 2.0 (On-The-Go (OTG)) interfaces. The devices provide protection to downstream components from ESD voltages up to  $\pm 8$  kV contact discharge. They offer three low capacitance ESD protection pins and one  $V_{BUS}$  protection diode. They are encapsulated in an ultra thin DFN1616-6 (SOT1189-1/XSON6) plastic package with 0.5 mm pitch. These features make the devices ideal for use in applications requiring component miniaturization, such as mobile phone handsets.

### 1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) and Dark Green compliant
- ESD protection according to IEC 61000-4-2 level 4:  $\pm 8$  kV contact discharge
- Electrical Fast Transients (EFT) protection according to IEC 61000-4-4 40A (5/50 ns)
- Three pairs of ultra low capacitance (1.1 pF typ.) rail-to-rail ESD protection diodes
- Ultra thin DFN1616-6 (SOT1189-1/XSON6) plastic package; 0.5 mm pitch

### 1.3 Applications

High-speed USB 2.0 and USB OTG connector ESD protection in:

- Cellular phone and Personal Communication System (PCS) mobile handsets
- Mobile internet devices
- Digital still cameras
- Portable media players

## 2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	low capacitance ESD protection	<p>Transparent top view</p>	<p>018aaa140</p>
2	low capacitance ESD protection		
3	low capacitance ESD protection		
4	not connected		
5	not connected		
6	$V_{BUS}$ ESD protection		
7	ground (GND)		



### 3. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
PUSBM5V5X4-TL	DFN1616-6	plastic, thermal enhanced extremely thin small outline package; no leads; 6 terminals; body 1.6 × 1.6 × 0.5 mm	SOT1189-1
PUSBM12VX4-TL			
PUSBM15VX4-TL			
PUSBM30VX4-TL			

### 4. Marking

Table 3. Marking codes

Type number	Marking code
PUSBM5V5X4-TL	XE
PUSBM12VX4-TL	XL
PUSBM15VX4-TL	XO
PUSBM30VX4-TL	30

### 5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>RWM</sub>	reverse standoff voltage	pins 1, 2, 3	-0.5	+5.5	V
		PUSBM5V5X4-TL pin 6 (V <sub>BUS</sub> )	-0.5	+5.5	V
		PUSBM12VX4-TL pin 6 (V <sub>BUS</sub> )	-0.5	+12	V
		PUSBM15VX4-TL pin 6 (V <sub>BUS</sub> )	-0.5	+15	V
		PUSBM30VX4-TL pin 6 (V <sub>BUS</sub> )	-0.5	+30	V
V <sub>ESD</sub>	electrostatic discharge voltage	IEC 61000-4-2, level 4; pins 1, 2, 3, 6 to GND; <a href="#">[1]</a>	-	±8	kV
P <sub>PP</sub>	peak pulse power	t <sub>p</sub> = 8/20 μs			
		pins 1, 2, 3; V <sub>CL</sub> = 12 V	-	35	W
		PUSBM5V5X4-TL pin 6 (V <sub>BUS</sub> ); V <sub>CL</sub> = 9.2 V	-	100	W
		PUSBM12VX4-TL pin 6 (V <sub>BUS</sub> ); V <sub>CL</sub> = 16 V	-	100	W
		PUSBM15VX4-TL pin 6 (V <sub>BUS</sub> ); V <sub>CL</sub> = 22 V	-	100	W
	PUSBM30VX4-TL pin 6 (V <sub>BUS</sub> ); V <sub>CL</sub> = 43 V	-	100	W	
I <sub>PP</sub>	peak pulse current	t <sub>p</sub> = 8/20 μs			
		pins 1, 2, 3	-	3	A
		PUSBM5V5X4-TL pin 6 (V <sub>BUS</sub> )	-	12	A
		PUSBM12VX4-TL pin 6 (V <sub>BUS</sub> )	-	6	A
		PUSBM15VX4-TL pin 6 (V <sub>BUS</sub> )	-	3	A
	PUSBM30VX4-TL pin 6 (V <sub>BUS</sub> )	-	2	A	

**Table 4. Limiting values ...continued**  
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>reflow(peak)</sub>	peak reflow temperature	t <sub>p</sub> ≤ 10 s	-	+260	°C
T <sub>amb</sub>	ambient temperature		-30	+85	°C
T <sub>stg</sub>	storage temperature		-55	+150	°C

[1] Device is qualified with 1000 pulses of ±8 kV contact discharges each, according to IEC61000-4-2 far exceeding level 4 (±8 kV contact discharge).

## 6. Characteristics

**Table 5. Characteristics**  
T<sub>amb</sub> = 25 °C unless otherwise specified.

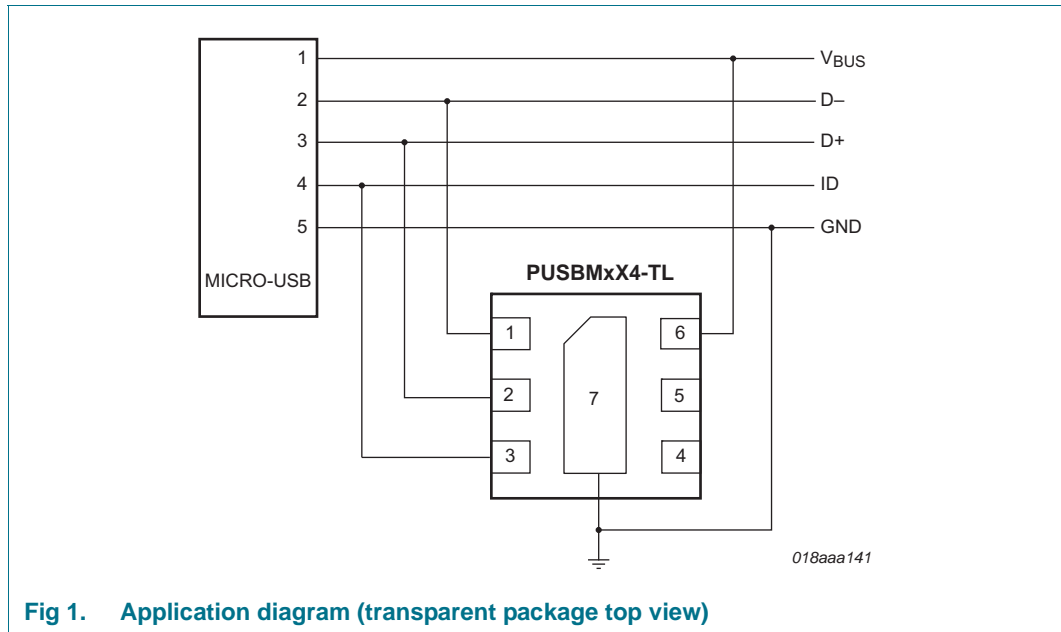
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>F</sub>	forward voltage		0.6	-	1.2	V
<b>Low capacitance ESD protection</b>						
V <sub>BRzd</sub>	Zener diode breakdown voltage	I <sub>test</sub> = 1 mA	6	-	10	V
C <sub>(I/O-GND)</sub>	input/output to ground capacitance	V <sub>bias(DC)</sub> = 0.5 V; f = 1 MHz; pins 1, 2, 3 to GND	[1]	-	1.1	1.3 pF
ΔC <sub>(I/O-GND)</sub>	input/output to ground capacitance variation	V <sub>bias(DC)</sub> = 0.5 V; f = 1 MHz	-	0.02	-	pF
C <sub>(I/O-I/O)</sub>	input/output to input/output capacitance	V <sub>bias(DC)</sub> = 0.5 V; f = 1 MHz; pins 1 to 2, 1 to 3, 2 to 3	-	0.5	-	pF
I <sub>RM</sub>	reverse leakage current	pins 1, 2, 3 to GND; V <sub>RWM</sub> = 5.5 V	-	100	1000	nA
<b>V<sub>BUS</sub> ESD protection</b>						
V <sub>BR</sub>	breakdown voltage	pin 6 (V <sub>BUS</sub> ) to GND; I <sub>test</sub> = 1 mA				
	PUSBM5V5X4-TL		6.4	6.8	7.2	V
	PUSBM12VX4-TL		12.5	14.5	16	V
	PUSBM15VX4-TL		17	18	19	V
	PUSBM30VX4-TL		32	36	40	V
C <sub>d</sub>	diode capacitance	V <sub>bias(DC)</sub> = 0.5 V; f = 1 MHz; pin 6 (V <sub>BUS</sub> ) to GND				
	PUSBM5V5X4-TL		-	165	220	pF
	PUSBM12VX4-TL		-	73	100	pF
	PUSBM15VX4-TL		-	60	90	pF
	PUSBM30VX4-TL		-	50	70	pF
I <sub>RM</sub>	reverse leakage current	pin 6 (V <sub>BUS</sub> ) to GND				
	PUSBM5V5X4-TL	V <sub>RWM</sub> = 5.5 V	-	200	500	nA
	PUSBM12VX4-TL	V <sub>RWM</sub> = 12 V	-	1	100	nA
	PUSBM15VX4-TL	V <sub>RWM</sub> = 15 V	-	1	100	nA
	PUSBM30VX4-TL	V <sub>RWM</sub> = 30 V	-	1	100	nA

[1] Guaranteed by design.

## 7. Application information

### 7.1 Typical application

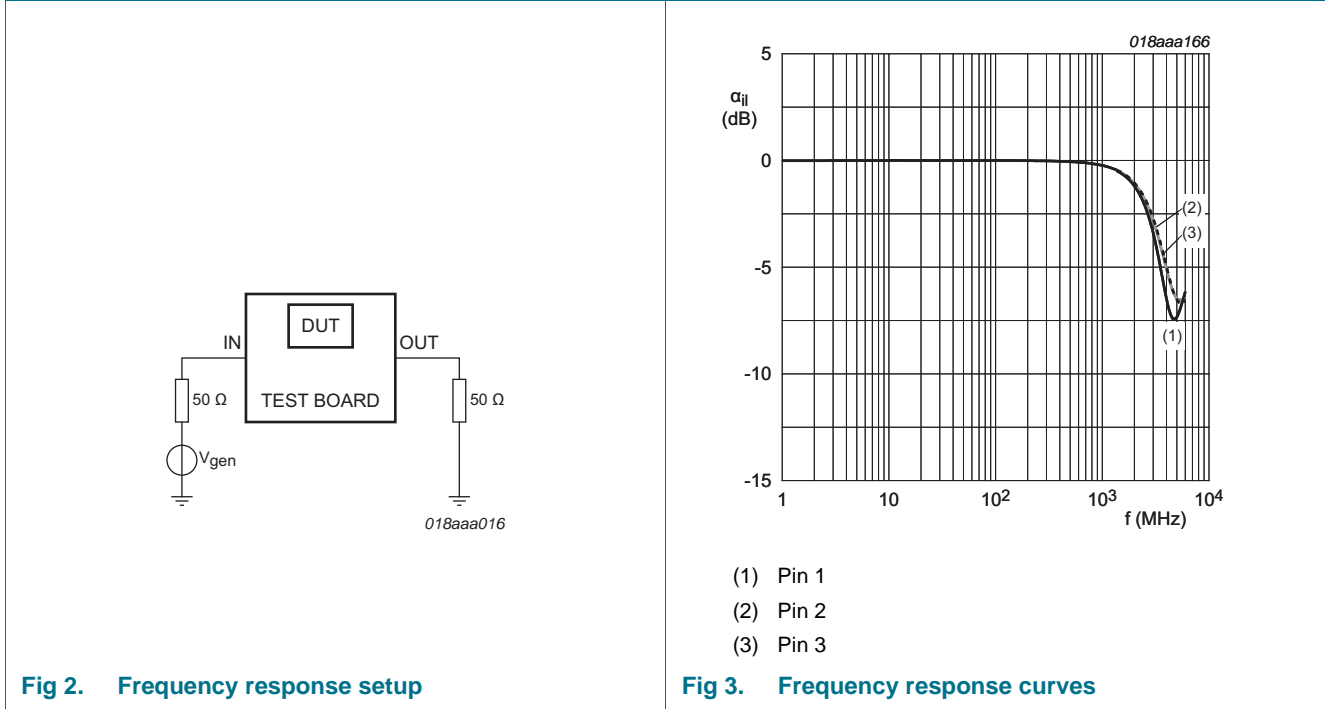
The devices are designed to protect USB interfaces from downstream ESD. They offer three low capacitance ESD protection channels for D-, D+ and ID and a high-voltage ESD protection channel for V<sub>BUS</sub>.



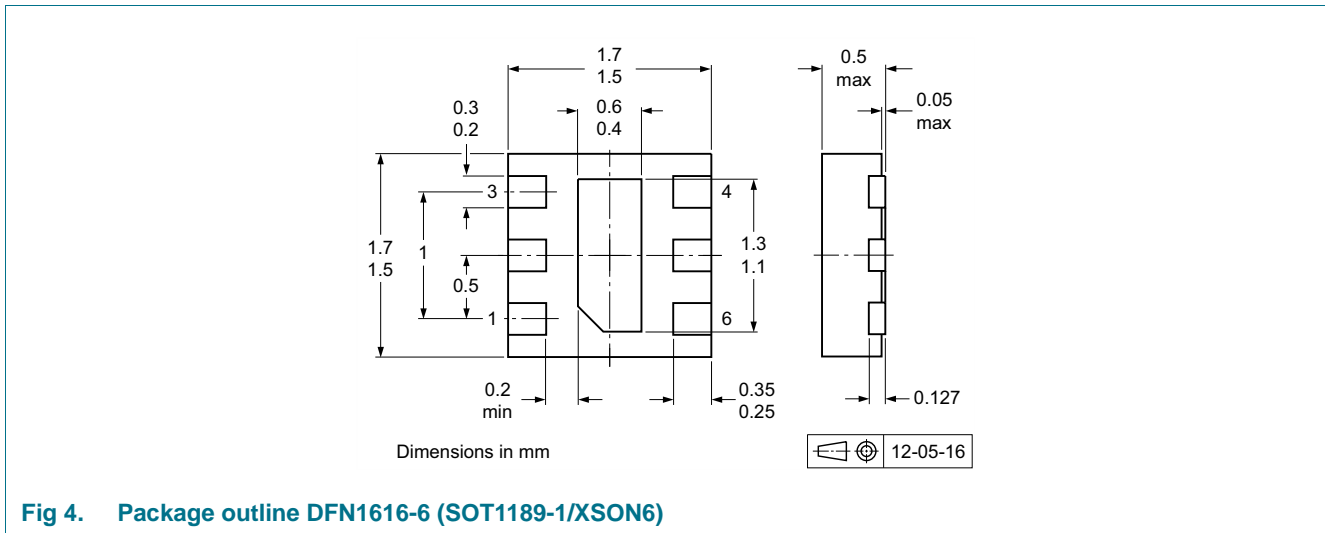
**Fig 1. Application diagram (transparent package top view)**

**7.2 Insertion loss**

The setup for measuring frequency response curves in a 50 Ω system is shown in [Figure 2](#). The frequency response curves for the low capacitance ESD protection channels (pins 1 to 3) are depicted in [Figure 3](#).



**8. Package outline**



## 9. Soldering

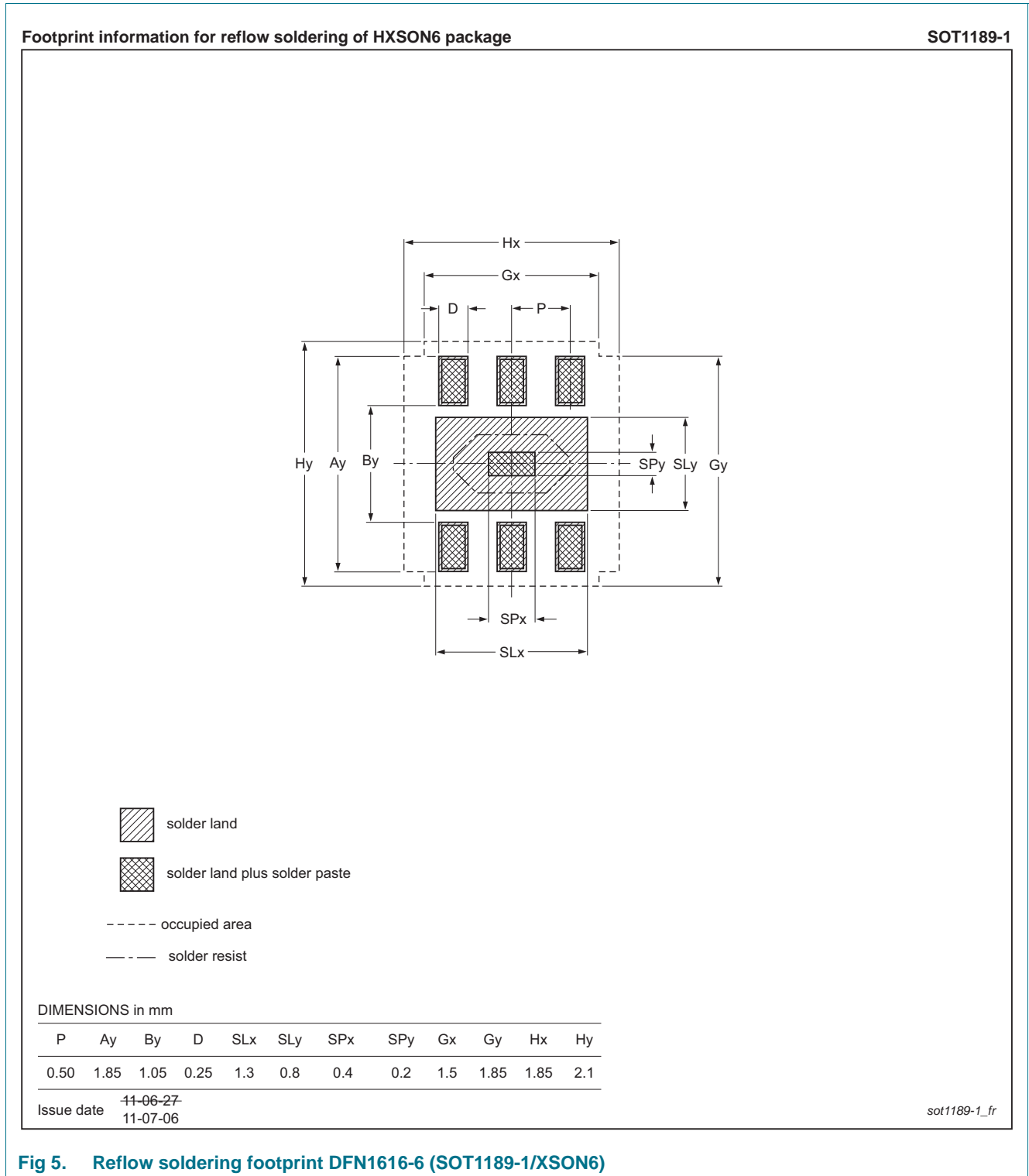


Fig 5. Reflow soldering footprint DFN1616-6 (SOT1189-1/XSON6)

## 10. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PUSBMXX4-TL_SER v.3	20120614	Product data sheet	-	PUSBMXX4-TL_SER v.2
Modifications:				
			<ul style="list-style-type: none"><li>• <a href="#">Section 2 "Pinning information"</a>: simplified outline graph updated</li><li>• <a href="#">Figure 1</a> updated</li><li>• <a href="#">Figure 4</a> replaced by minimized package outline</li></ul>	
PUSBMXX4-TL_SER v.2	20120416	Preliminary data sheet	-	PUSBMXX4-TL_SER v.1
PUSBMXX4-TL_SER v.1	20111209	Preliminary data sheet	-	-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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