PIC18F24/25/44/45K20 Device IDs Rev. 0x16 to 0x1B Silicon Errata and Data Sheet Clarification

The PIC18F24/25/44/45K20 family devices that you have received conform functionally to the current Device Data Sheet (DS41303**F**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F24/25/44/45K20 silicon.

Note:	This document summarizes all silicon errata issues for Device ID Revisions 0x16 to 0x19.

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F24/25/44/45K20 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1) (11-bit)	Revision ID for Silicon Revision(2) (5-bit)			
		A4	A7	A8	AE
PIC18F24K20	105h	0x16	0x18	0x19	0x1B
PIC18F25K20	103h	0x16	0x18	0x19	0x1B
PIC18F44K20	104h	0x16	0x18	0x19	0x1B
PIC18F45K20	102h	0x16	0x18	0x19	0x1B

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID:DEVREV".

2: Refer to the *"PIC18F2XK20/4XK20 Flash Memory Programming Specification"* (DS41297) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				0x16	0x18	0x19	0x1B
ECCP	Full-Bridge mode	1.	Wrong dead-band time.	X	X	X	X
ECCP	Full-Bridge mode	2.	Wrong signal start time.	X	X	X	X
MSSP SPI	SPI Clock	3.	Improper SCK output.	X	X	X	X
MSSP SPI	SPI Master	4.	Improper sampling of last bit.	X	X	X	X
MSSP SPI	SPI Master	5.	Improper handling of write collision.	X	X	X	X
MSSP I^2C™	I^2C™ Master	6.	Improper handling of Stop event.	X	X	X	X
EUSART	OERR Flag	7.	Clearing SPEN bit does not clear OERR flag.	X	X	X	X
EUSART	BAUDCTL	8.	RCIDL bit may stay low improperly.	X	X	X	X
Data EEPROM Memory	Endurance	9.	Endurance is limited to 10K cycles.	X	X	X	
Program Flash Memory	Endurance	10.	Endurance is limited to 1K cycles.	X	X	X	
PORTB Interrupt-on-change	Interrupt-on-Change	11.	False interrupt when setting interrupt enable.	X	X	X	X
ADC	ADC Conversion	12.	ADC conversion may be limited to half scale.	X	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current revision ID (**0x1B**).

1. Module: ECCP

Changing direction in Full-Bridge mode inserts a dead-band time of 4/FOSC * TMR2 Prescale instead of 1/FOSC * TMR2 Prescale as specified in the data sheet.

Work around

None.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

2. Module: ECCP

ECCP – In Full-Bridge mode when PR2 = CCPR1L and DC1B[1:0] <>'00' and the direction is changed then the dead time before the modulated output starts is compromised. The modulated signal improperly starts immediately with the direction change and stays on for TOSC * TMR2Presale * DC1B[1:0].

Work around

Avoid changing direction when the duty cycle is within three Least Significant steps of 100% duty cycle. Instead, clear the DC1B[1:0] bits before the direction change and then set them to the desired value after the direction change is complete.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

3. Module: MSSP SPI

When the SPI clock is configured for Timer2/2 (SSPCON1<3:0> = 0011) and the CKE bit of the SSPSTAT register is '1', then when SSPBUF is written, the SCK output is improperly immediately driven to the non-Idle state together with the MSb value of the SSPBUF. The duration at which SDO and SCK remain at these levels may be shorter than a full half-bit period. The remaining bits in the byte are output properly.

Work around

None.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

4. Module: MSSP SPI

In SPI Master mode, when the CKE bit of the SSPSTAT register is cleared and the SMP bit of the SSPSTAT register is set, then the last bit of the incoming data stream (bit 0) at the SDI pin will not be sampled properly.

Work around

None.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

5. Module: MSSP SPI

In SPI Master mode, if the SSPBUF register is written while a byte is actively being transmitted, an extra clock pulse will be improperly generated at the end of the transmission. Further writes to the SSPBUF register will be inhibited although 8 or 9 clock pulses will be generated for each attempted write. The WCON bit of the SSPCON register is properly set indicating that a write collision occurred. However, the write collision condition can only be cleared by resetting the MSSP module. Clear the MSSP by clearing the SSPEN bit of the SSPCON1 register.

Work around

Use the SSPIF bit of the PIR1 register or the BF bit of the SSPSTAT register to determine that the transmission is complete before writing the SSP-BUF register. In the event that a write collision does occur, use the slave select feature to resynchronize the slave clock.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

6. Module: MSSP I²C™

In Master I²C Receive mode if a Stop condition occurs in the middle of an address or data reception, then the SCL clock stream will continue endlessly and the RCEN bit of the SSPCON2 register will remain set improperly. If a Start condition occurs after the improper Stop condition then 9 additional clocks will be generated followed by the RCEN bit going low.

Work around

Use low-impedance pull-ups on the SDA line to reduce the possibility of noise glitches which may trigger an improper Stop event. Use a time-out event timer to detect the unexpected Stop condition and resulting stuck RCEN bit. Clear the stuck RCEN bit by clearing the SSPEN bit of SSPCON1.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

7. Module: EUSART

The OERR flag of the RCSTA register is reset only by clearing the CREN bit of the RCSTA register or by a device Reset. Clearing the SPEN bit of the RCSTA register does not clear the OERR flag.

Work around

Clear the OERR flag by clearing the CREN bit instead of clearing the SPEN bit.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

8. Module: EUSART

In Asynchronous Receive mode, the RCIDL bit of the BAUDCON register will properly go low when an invalid Start bit less than 1/16th of a bit time is received. The RCIDL bit will then properly go high 1/8th of a bit time later. However, if another invalid Start bit occurs less than 1 bit time after the leading edge of the first invalid Start bit, then the RCIDL bit will improperly stay high then improperly go low one bit time later. The RCIDL bit will then stay low improperly until a valid Start bit is received.

Work around

When monitoring the RCIDL bit, measure the length of time between the RCIDL going low and the RCIF flag going high. If this time is greater than one character time, then restore the RCIDL bit by resetting the EUSART module. The EUSART module is reset when the SPEN bit of the RCSTA register is cleared.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

9. Module: Data EEPROM Memory

The write/erase endurance of Data EE Memory is limited to 10K cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X				

10. Module: Program Flash Memory

The write/erase endurance of the PFM is limited to 1K cycles when VDD is above 3V. Endurance degrades when VDD is below 3V.

Work around

For data tables in program Flash memory use error correction method that stores data in multiple locations.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X				

11. Module: PORTB Interrupt-on-change

Setting a PORTB interrupt-on-change enable bit of the IOCB register while the corresponding PORTB input is high will cause an RBIF interrupt.

Work around

Set the IOCB bits to the desired configuration then read PORTB to clear the mismatch latches. Finally, clear the RBIF bit before setting the RBIE bit.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X	X			

12. Module: ADC

After extended stress the Most Significant bit (MSb) of the ADC conversion result can become stuck at '0'. Conversions resulting in code 511 or less are still accurate, but conversions that should result in codes greater than 511 are instead pinned at 511.

The potential for failures is a function of several factors:

- The potential for failures increases over the life of the part. No failures have ever been seen for accelerated stress estimated to be equivalent to 34 years at room temperature. The failure rate after accelerated stress estimated to be equivalent to 146 years at room temperature can be as high as 10% for VDD = 1.8V. The time to failure will decrease as the operating temperature increases.
- The potential for failures is highest at low VDD and decreases as VDD increases.
- The potential for failures depends on the settings of the ADCW<2:0> and ACQT<2:0> bits in ADCON2:

ADCS<2:0>	ACQT<2:0> = 000	ACQT<2:0> ≠ 000
011 or 111	No Failures	Low Probability
000	Very Low Probability	Low Probability
001, 010, 100, 101, or 110	Moderate Probability	Moderate Probability

Work around

1. Restrict the input voltage to less than 1/2 of the ADC voltage reference so that the expected result is always a code less than or equal to 511.
2. Use manual acquisition time (ACQT<2:0> = 000) and use the ADC's dedicated internal oscillator as the conversion clock source (ADCS<2:0>) = 011 or 111).
3. Use manual acquisition time (ACQT<2:0> = 000) and put the part to Sleep after each conversion.

Affected Silicon Revisions

0x16	0x18	0x19	0x1B			
X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41303**F**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (12/2008)

Initial release of this document.

Rev B Document (05/2009)

Updated Errata to new format; Added Module 11: PORTB and Module 12: ADC; minor edits.

Clarifications/Corrections to the Data Sheet: Added Module 1: MSSP; Module 2: Electrical Specifications; Module 3: Electrical Specifications.

Rev C Document (06/2009)

Clarifications/Corrections to the Data Sheet:

Deleted Module 1: MSSP: Figure 17-17 Baud Rate Generator Block Diagram, updating subsequent numbering. Added Module 3 MSSP: Register 17-3 SSPADD; Added Module 4 MSSP: Section 17.4.2 Operation; Added Module 5 MSSP: Figure 17-16 MSSP Block Diagram; Added Module 6 MSSP: Sections 17.4.7.1, 17.4.8, 17.4.9, 17.4.17.1, 17.4.17.2, 17.4.17.3: SSPADD, changing <6:0> to <7:0>.

Rev D Document (11/2009)

Updated to add revision 0x1B.

Data Sheet Clarifications: Deleted Modules 1, 2, 3, 4, 5, 6.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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