

PESD5V0L7BAS; PESD5V0L7BS

Low capacitance 7-fold bidirectional ESD protection diode arrays

Rev. 03 — 20 August 2009

Product data sheet

1. Product profile

1.1 General description

Low capacitance 7-fold bidirectional ESD protection diode arrays in small plastic packages designed for the protection of up to seven transmission or data lines from damage caused by ElectroStatic Discharge (ESD) and other transients.

Table 1. Product overview

Type number	Package	
	Name	NXP
PESD5V0L7BAS	TSSOP8	SOT505-1
PESD5V0L7BS	SO8	SOT96-1

1.2 Features

- ESD protection of up to seven lines
- Low diode capacitance
- Max. peak pulse power: $P_{pp} = 35 \text{ W}$
- Low clamping voltage: $V_{(CL)R} = 17 \text{ V}$
- Ultra low leakage current: $I_{RM} = 3 \text{ nA}$
- ESD protection of up to 10 kV
- IEC 61000-4-2, level 4 (ESD)
- IEC 61000-4-5 (surge); $I_{pp} = 2.5 \text{ A}$

1.3 Applications

- Computers and peripherals
- Communication systems
- Audio and video equipment
- High speed data lines
- Parallel ports

1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse stand-off voltage		-	-	5	V
C_d	diode capacitance	$V_R = 0 \text{ V};$ $f = 1 \text{ MHz}$	-	8	10	pF

2. Pinning information

Table 3. Discrete pinning

Pin	Description	Simplified outline	Symbol
TSSOP8			
1	cathode 1		
2	cathode 2		
3	cathode 3		
4	cathode 4		
5	cathode 5		
6	cathode 6		
7	cathode 7		
8	cathode 8		
SO8			
1	cathode 1		
2	cathode 2		
3	cathode 3		
4	cathode 4		
5	cathode 5		
6	cathode 6		
7	cathode 7		
8	cathode 8		

3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PESD5V0L7BAS	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1
PESD5V0L7BS	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Marking

Table 5. Marking codes

Type number	Marking code
PESD5V0L7BAS	5V0L7B
PESD5V0L7BS	5V0L7BS

5. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
Per diode					
P _{pp}	peak pulse power	8/20 μs pulse	[1] -	35	W
I _{pp}	peak pulse current	8/20 μs pulse	[1] -	2.5	A
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-65	+150	°C
T _{stg}	storage temperature		-65	+150	°C

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC61000-4-5; see [Figure 1](#).

Table 7. ESD maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
ESD	electrostatic discharge capability	IEC 61000-4-2 (contact discharge)	[1] -	10	kV
		HBM MIL-STD883	-	10	kV

[1] Device stressed with ten non-repetitive ElectroStatic Discharge (ESD) pulses; see [Figure 2](#).

Table 8. ESD standards compliance

Standard	Conditions
IEC 61000-4-2, level 4 (ESD); see Figure 2	> 8 kV (contact)
HBM MIL-STD883, class 3	> 4 kV

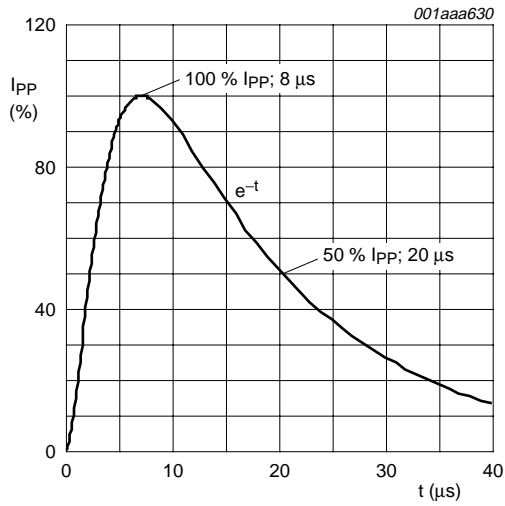


Fig 1. 8/20 μ s pulse waveform according to IEC 61000-4-5

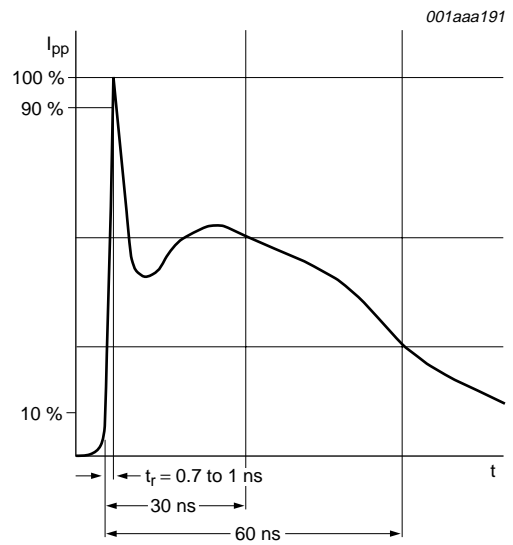


Fig 2. ElectroStatic Discharge (ESD) pulse waveform according to IEC 61000-4-2

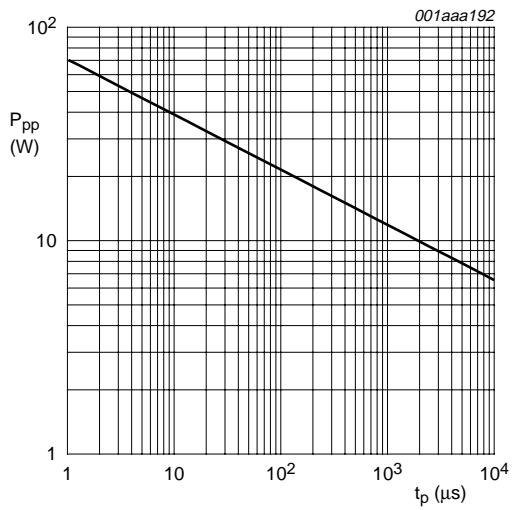
6. Characteristics

Table 9. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per diode						
V_{RWM}	reverse stand-off voltage		-	-	5	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}$; see Figure 6	-	3	25	nA
$V_{(CL)R}$	clamping voltage	$I_{pp} = 1\text{ A}$	[1]	-	11	V
		$I_{pp} = 2.5\text{ A}$	[1]	-	17	V
$V_{(BR)}$	breakdown voltage	$I_R = 1\text{ mA}$	7.2	7.6	7.9	V
r_{dif}	differential resistance	$I_R = 1\text{ mA}$	-	-	100	Ω
C_d	diode capacitance	$V_R = 0\text{ V}$; $f = 1\text{ MHz}$; see Figure 5	-	8	10	pF

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC61000-4-5; see [Figure 1](#).



$T_{amb} = 25\text{ }^\circ C$

Fig 3. Peak pulse power as a function of exponential pulse duration t_p ; typical values

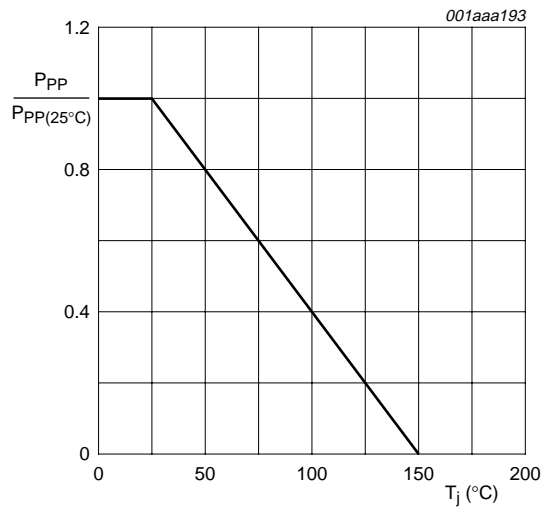
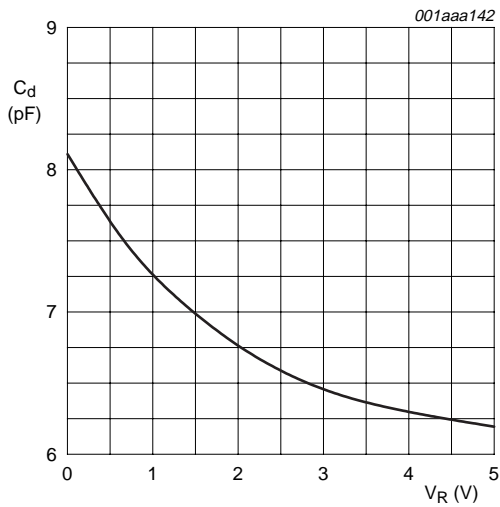


Fig 4. Relative variation of peak pulse power as a function of junction temperature; typical values



$T_{amb} = 25\text{ }^\circ C$; $f = 1\text{ MHz}$

Fig 5. Diode capacitance as a function of reverse voltage; typical values

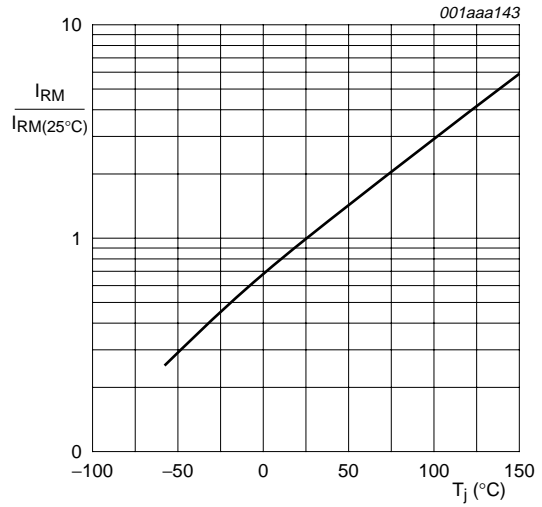


Fig 6. Relative variation of reverse leakage current as a function of junction temperature; typical values

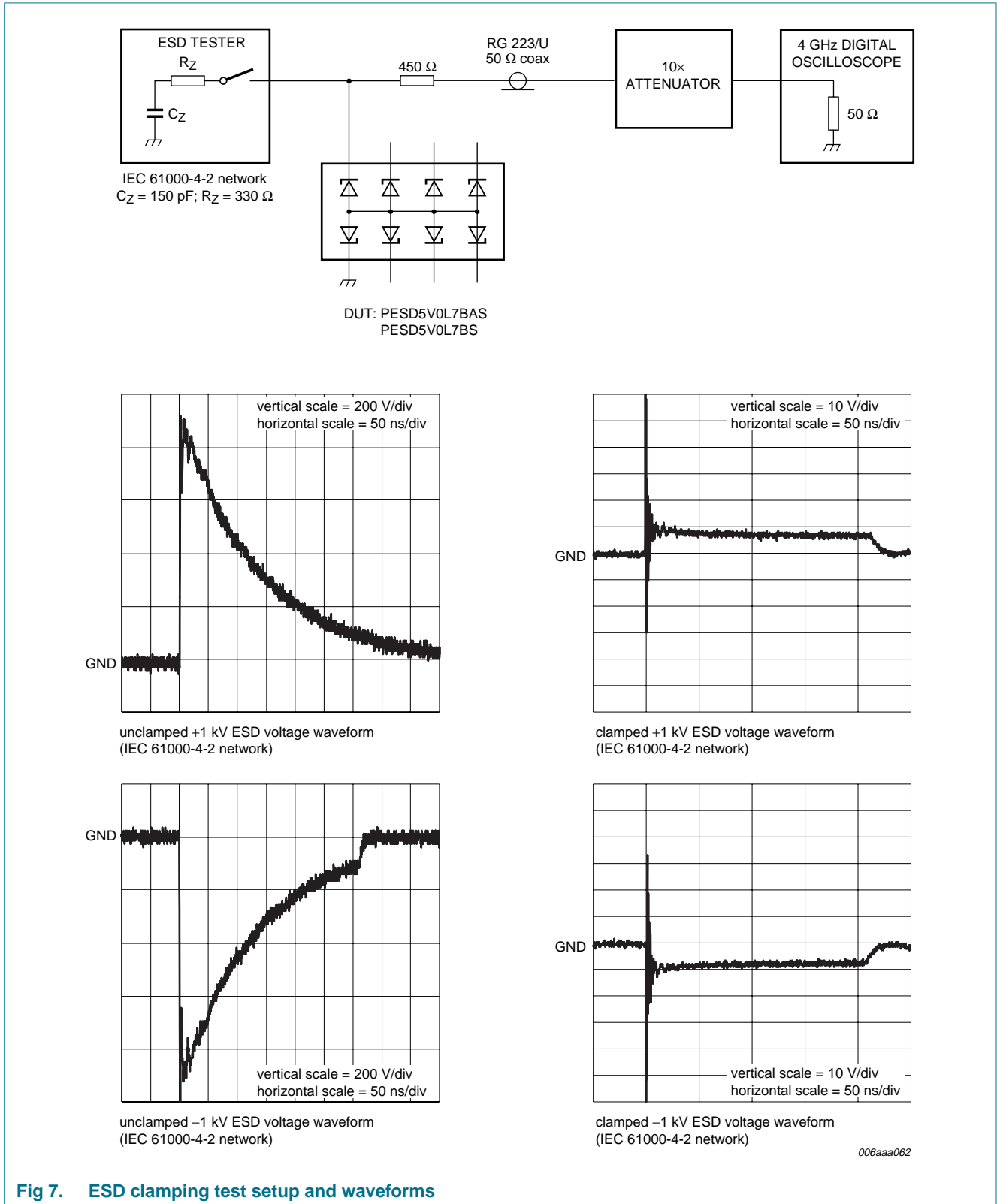


Fig 7. ESD clamping test setup and waveforms

7. Application information

The PESD5V0L7BAS and the PESD5V0L7BS are designed for protection of up to seven bidirectional data lines from the damage caused by ElectroStatic Discharge (ESD) and surge pulses. The PESD5V0L7BAS and the PESD5V0L7BS may be used on lines whose signal polarities are above and below ground.

The PESD5V0L7BAS and the PESD5V0L7BS provide a surge capability of 35 W per line for a 8/20 μ s waveform.

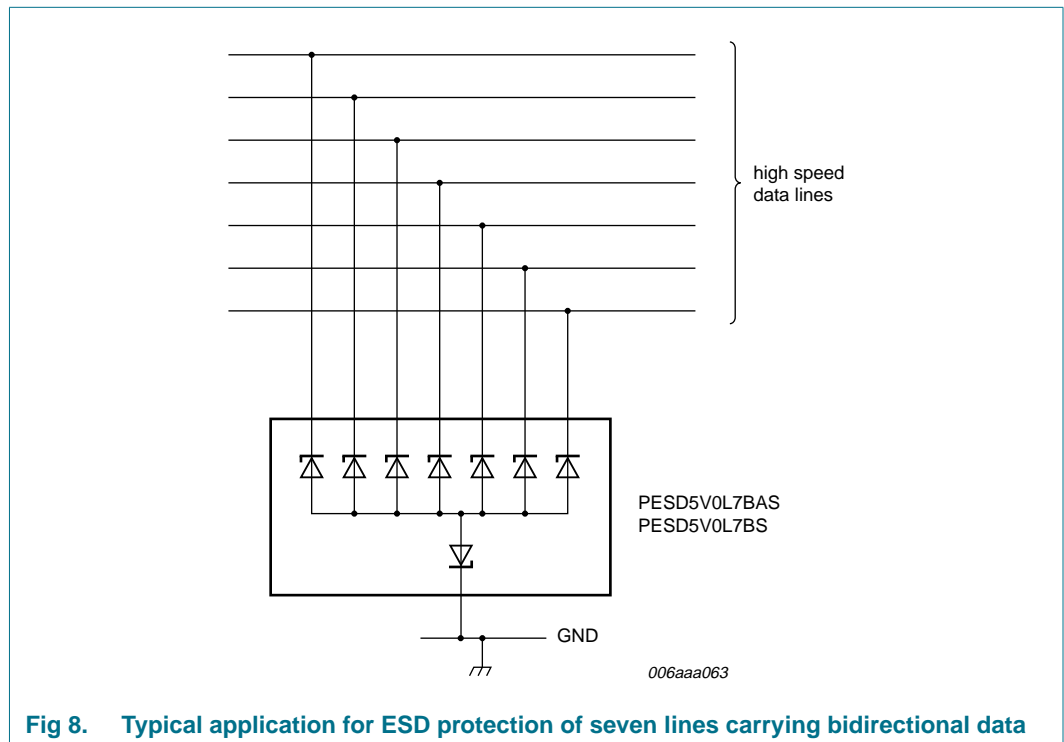


Fig 8. Typical application for ESD protection of seven lines carrying bidirectional data

Circuit board layout and protection device placement:

Circuit board layout is critical for the suppression of ESD, EFT and surge transients. The following guidelines are recommended:

1. Place the protection device as close as possible to the input terminal or connector.
2. Minimize the path length between the protection device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all printed-circuit board conductive loops including power and group loops.
6. Minimize the length of transient return paths to ground.
7. Avoid using shared return paths to a common ground point.
8. Ground planes should be used whenever possible.
9. Use vias for multilayer printed-circuit boards.

8. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1

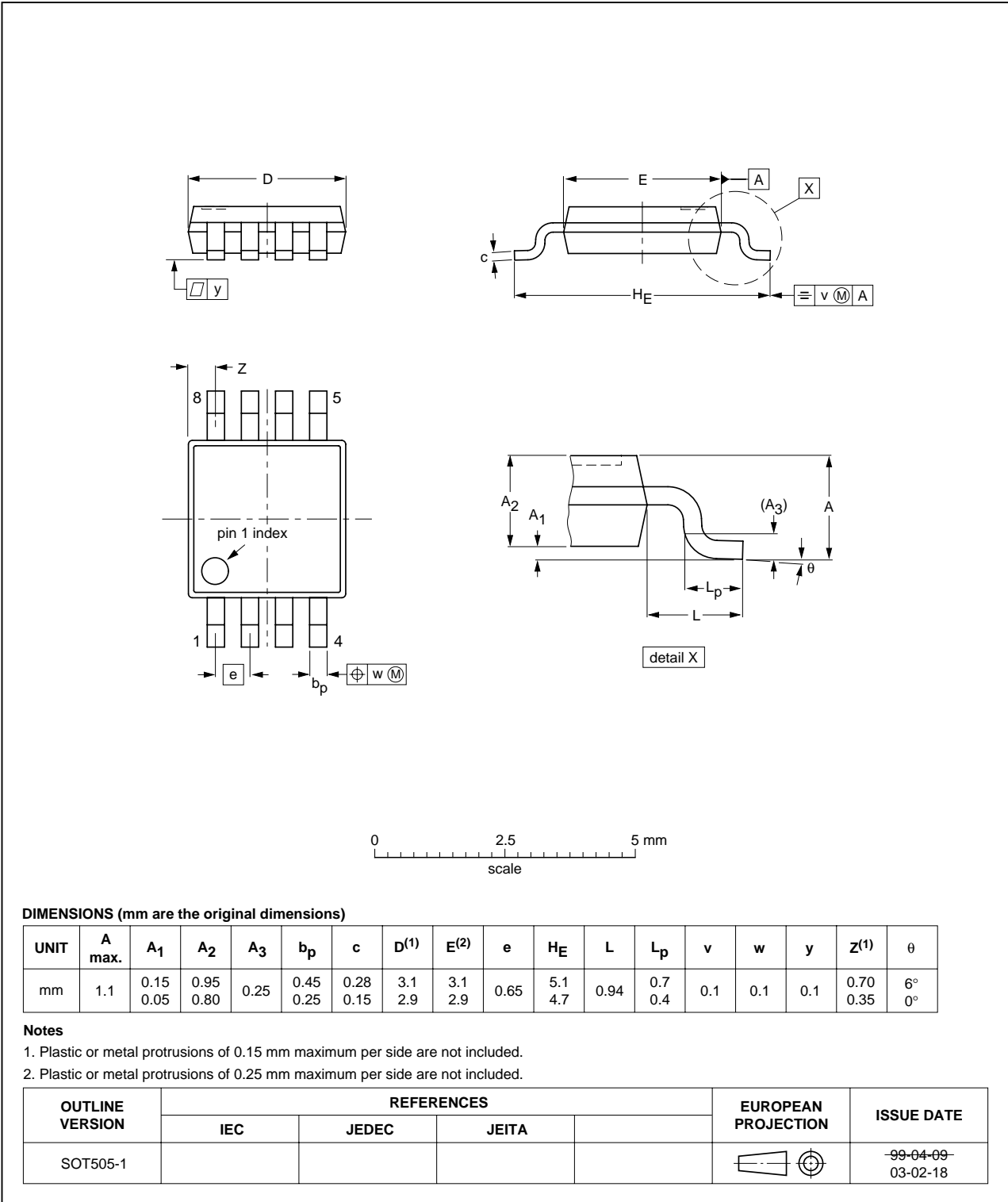


Fig 9. Package outline SOT505-1 (TSSOP8)

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

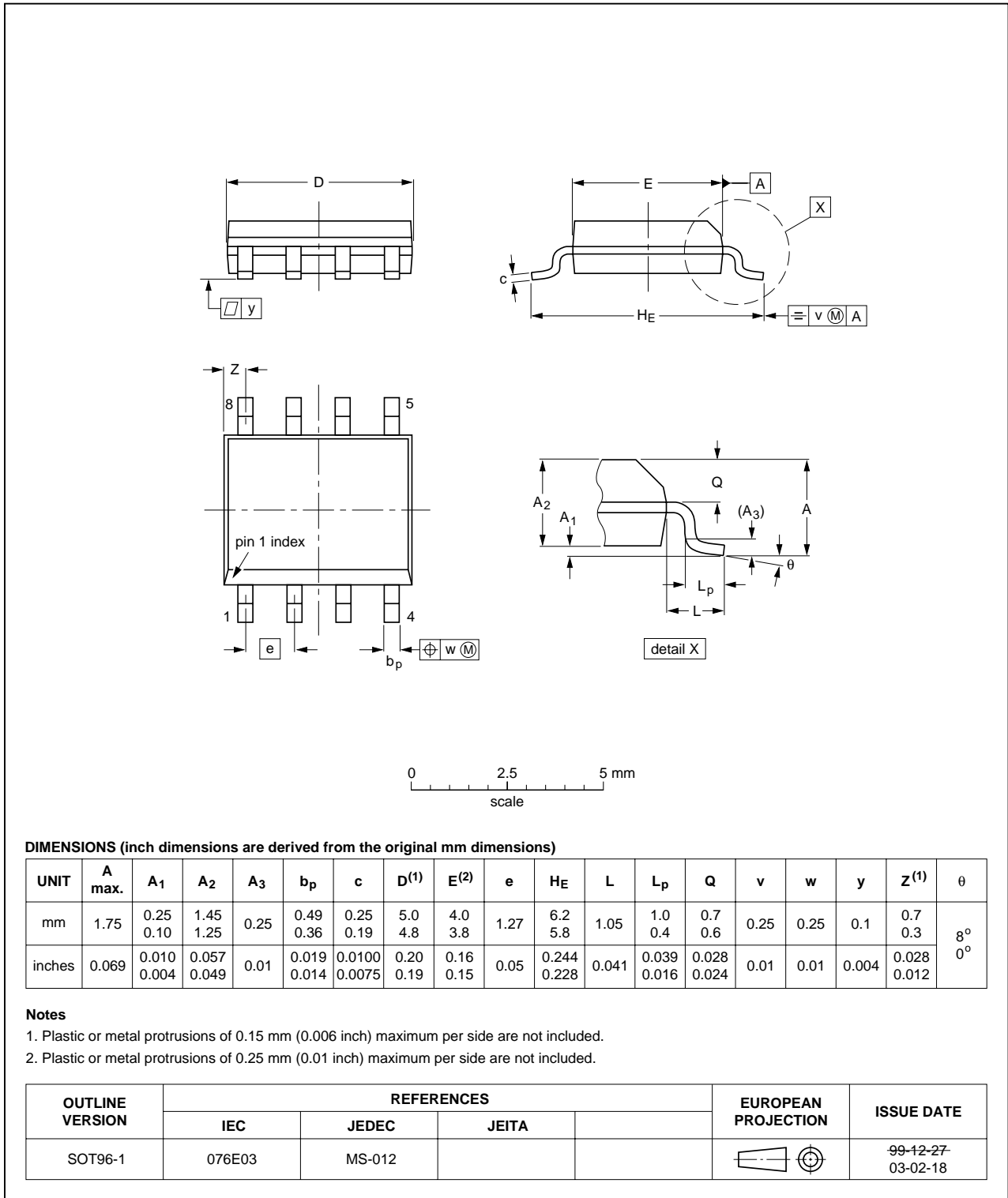


Fig 10. Package outline SOT96-1 (SO8/MS-012)

9. Packing information

Table 10. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity	
			1000	2500
PESD5V0L7BAS	SOT505-1	8 mm pitch, 12 mm tape and reel	-	-118
PESD5V0L7BS	SOT96-1	8 mm pitch, 12 mm tape and reel	-115	-118

[1] For further information and the availability of packing methods, see [Section 12](#).

10. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0L7BAS_BS_3	20090820	Product data sheet	-	PESD5V0L7BAS_BS_2
Modifications:		<ul style="list-style-type: none">This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.Table 3 "Discrete pinning": amended		
PESD5V0L7BAS_BS_2	20041125	Product data sheet	-	PESD5V0L7BS_1
PESD5V0L7BS_1	20040315	Product specification	-	-

11. Legal information

11.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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