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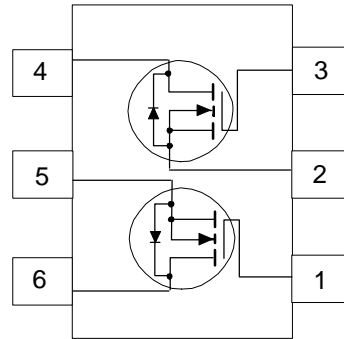
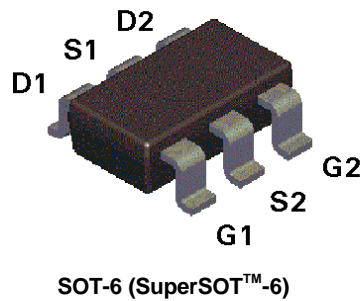
## NDC7002N Dual N-Channel Enhancement Mode Field Effect Transistor

### General Description

These dual N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. These devices is particularly suited for low voltage applications requiring a low current high side switch.

### Features

- 0.51A, 50V,  $R_{DS(ON)} = 2\Omega @ V_{GS}=10V$
- High density cell design for low  $R_{DS(ON)}$
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High saturation current.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	NDC7002N	Units	
$V_{DSS}$	Drain-Source Voltage	50	V	
$V_{GSS}$	Gate-Source Voltage - Continuous	20	V	
$I_D$	Drain Current - Continuous (Note 1a)	0.51	A	
	- Pulsed	1.5		
$P_D$	Maximum Power Dissipation (Note 1a)	0.96	W	
		(Note 1b)		0.9
		(Note 1c)		0.7
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$	
<b>THERMAL CHARACTERISTICS</b>				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	$^\circ\text{C}/\text{W}$	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	60	$^\circ\text{C}/\text{W}$	

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	50			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 125^\circ\text{C}$			1 500	$\mu\text{A}$
$I_{GSSF}$	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>ON CHARACTERISTICS</b> (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	1 0.8	1.9 1.5	2.5 2.2	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.51\text{ A}$ $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 0.35\text{ A}$		1 1.7 1.6	2 3.5 4	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 10\text{ V}$	1.5			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 0.51\text{ A}$		400		mS
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		20		pF
$C_{oss}$	Output Capacitance			13		pF
$C_{rss}$	Reverse Transfer Capacitance			5		pF
<b>SWITCHING CHARACTERISTICS</b> (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 25\text{ V}, I_D = 0.25\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 25\ \Omega$		6	20	nS
$t_r$	Turn - On Rise Time			6	20	
$t_{D(off)}$	Turn - Off Delay Time			11	20	
$t_f$	Turn - Off Fall Time			5	20	
$Q_g$	Total Gate Charge	$V_{DS} = 25\text{ V},$ $I_D = 0.51\text{ A}, V_{GS} = 10\text{ V}$		1		nC
$Q_{gs}$	Gate-Source Charge			0.19		nC
$Q_{gd}$	Gate-Drain Charge			0.33		nC

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRAIN-SOURCE DIODE CHARACTERISTICS</b>						
$I_S$	Maximum Continuous Source Current				0.51	A
$I_{SM}$	Maximum Pulse Source Current (Note 2)				1.5	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 0.51\text{ A}$ (Note 2)		0.8	1.2	V

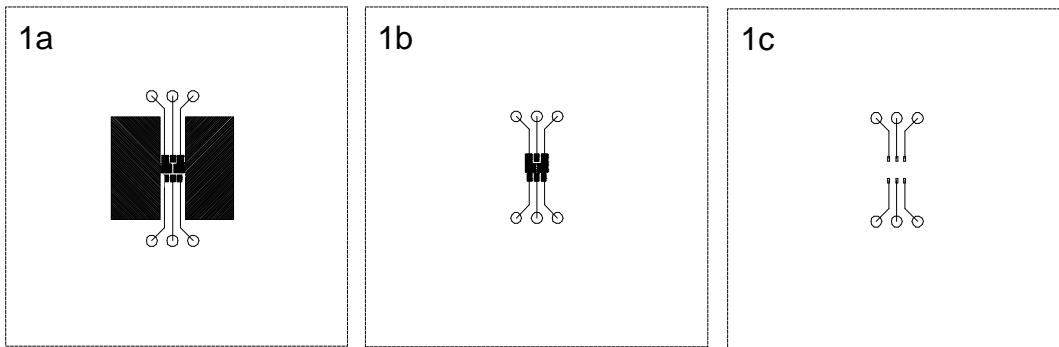
Notes:

- $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta J A(t)}} = \frac{T_J - T_A}{R_{\theta J C} + R_{\theta C A(t)}} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical  $R_{\theta JA}$  for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 130°C/W when mounted on a 0.125 in<sup>2</sup> pad of 2oz copper.
- 140°C/W when mounted on a 0.005 in<sup>2</sup> pad of 2oz copper.
- 180°C/W when mounted on a 0.0015 in<sup>2</sup> pad of 2oz copper.



Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## Typical Electrical Characteristics

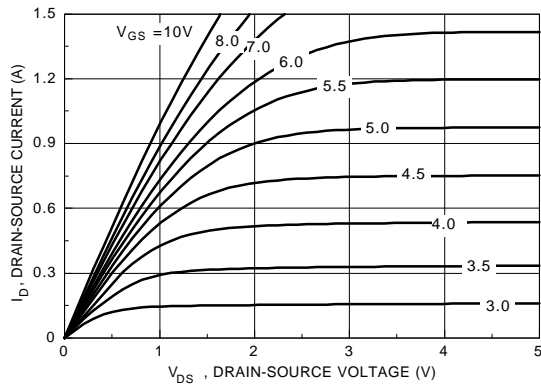


Figure 1. On-Region Characteristics.

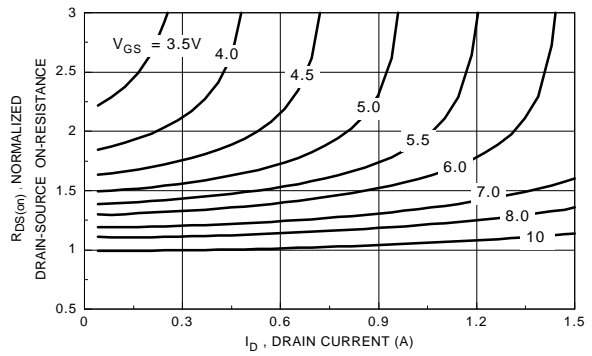


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

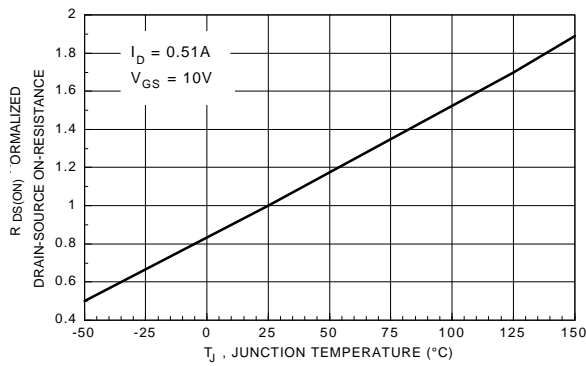


Figure 3. On-Resistance Variation with Temperature.

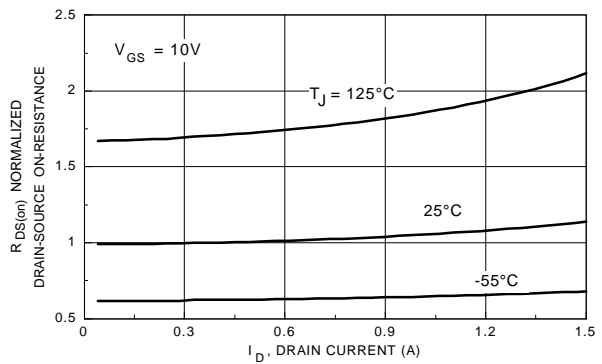


Figure 4. On-Resistance Variation with Drain Current and Temperature.

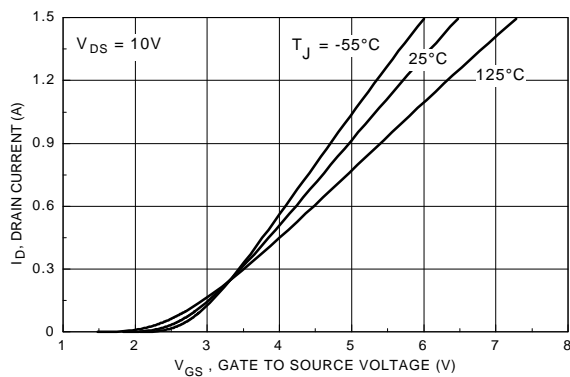


Figure 5. Transfer Characteristics.

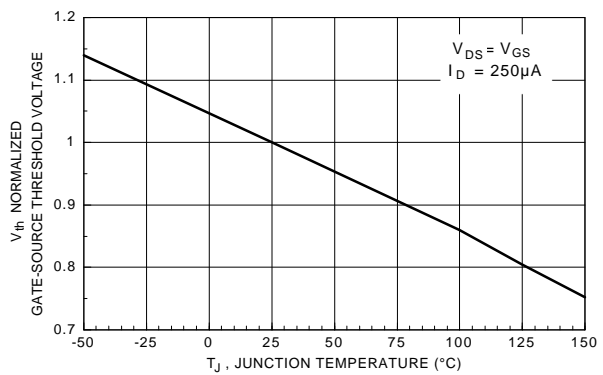
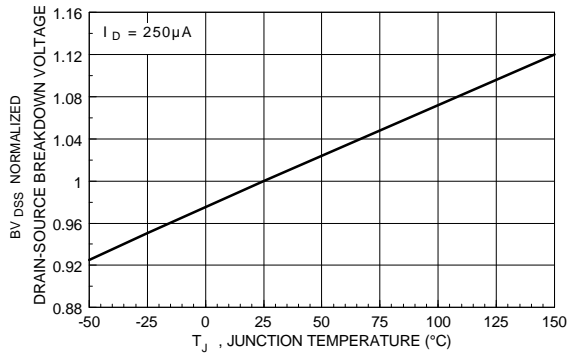
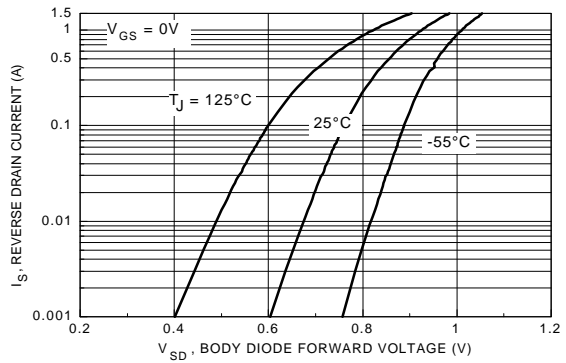


Figure 6. Gate Threshold Variation with Temperature.

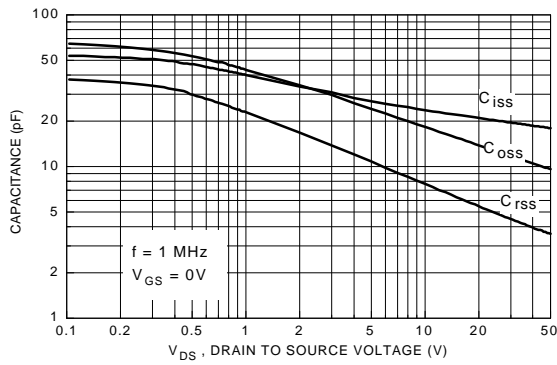
## Typical Electrical Characteristics (continued)



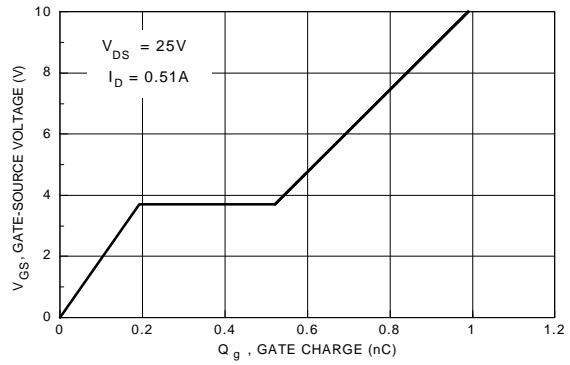
**Figure 7. Breakdown Voltage Variation with Temperature.**



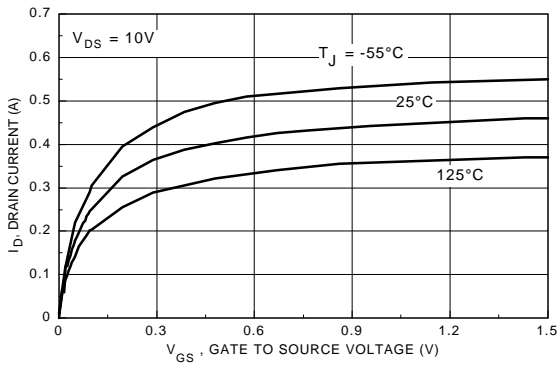
**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.**



**Figure 9. Capacitance Characteristics.**

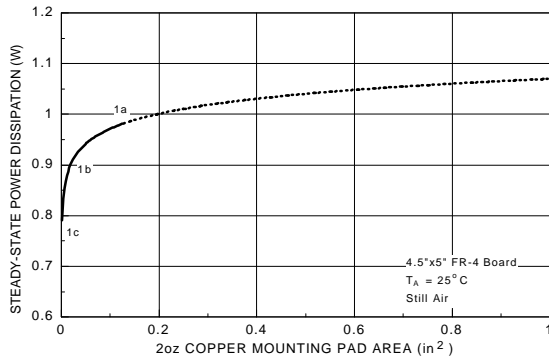


**Figure 10. Gate Charge Characteristics.**

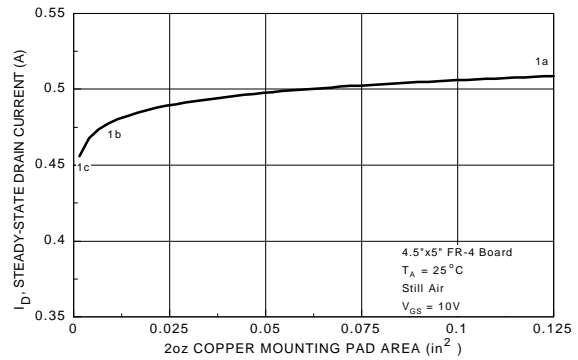


**Figure 11. Transconductance Variation with Drain Current and Temperature.**

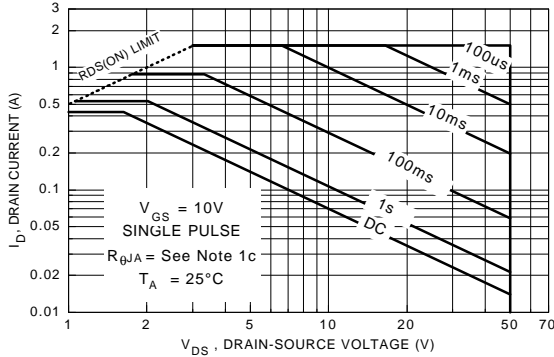
## Typical Thermal Characteristics



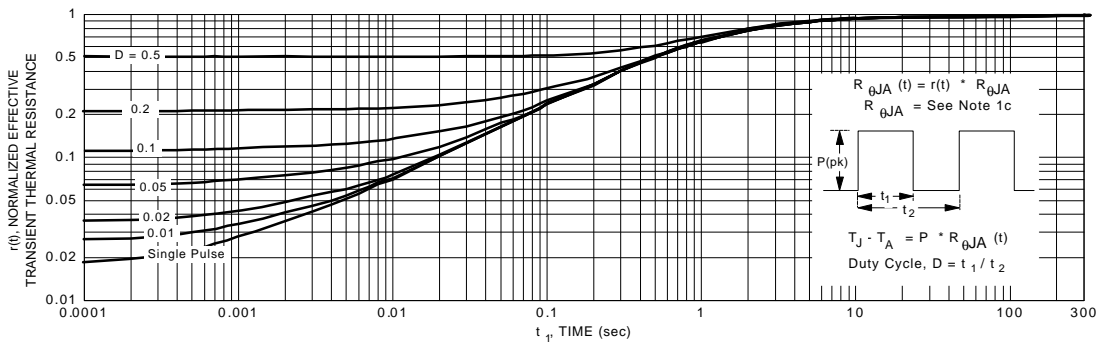
**Figure 12. SOT-6 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.**



**Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.**



**Figure 14. Maximum Safe Operating Area.**



**Figure 15. Transient Thermal Response Curve.**

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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