Freescale Semiconductor
Data Sheet: Advance Information

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RoHS

MCF5213 Microcontroller Family Hardware Specification

The MCF5213 is a member of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document provides an overview of the 32-bit MCF5213 microcontroller, focusing on its highly integrated and diverse feature set. Freescale reserves the right to change or discontinue this product without notice. Specifications and information herein are subject to change without notice.

This 32-bit device is based on the Version 2 ColdFire core operating at a frequency up to 80 MHz, offering high performance and low power consumption. On-chip memories connected tightly to the processor core include 256 Kbytes of Flash and 32 Kbytes of static random access memory (SRAM). On-chip modules include the following:

- V2 ColdFire core delivering 76 MIPS (Dhrystone 2.1) at 80 MHz running from internal Flash with Multiply Accumulate (MAC) Unit and hardware divider
- FlexCAN controller area network (CAN) module
- Three universal asynchronous/synchronous receiver/transmitters (UARTs)

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- Inter-integrated circuit (I^2C™) bus controller
- Queued serial peripheral interface (QSPI) module
- Eight-channel 12-bit fast analog-to-digital converter (ADC)
- Four-channel direct memory access (DMA) controller
- Four 32-bit input capture/output compare timers with DMA support (DTIM)
- Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation
- Eight-channel/Four-channel, 8-bit/16-bit pulse width modulation timer
- Two 16-bit periodic interrupt timers (PITs)
- Programmable software watchdog timer
- Interrupt controller capable of handling 57 sources
- Clock module with 8 MHz on-chip relaxation oscillator and integrated phase locked loop (PLL)
- Test access/debug port (JTAG, BDM)

1 MCF5213 Family Configurations

Table 1. MCF5213 Family Configurations

Module	5211	5212	5213
ColdFire Version 2 Core with MAC (Multiply-Accumulate Unit)	x	x	x
System Clock	66 MHz	66, 80 MHz	
Performance (Dhrystone 2.1 MIPS)	63	up to 76	
Flash / Static RAM (SRAM)	128/16 Kbytes	256/32 Kbytes	
Interrupt Controller (INTC)	x	x	x
Fast Analog-to-Digital Converter (ADC)	x	x	x
FlexCAN 2.0B Module	—	—	x
Four-channel Direct-Memory Access (DMA)	x	x	x
Software Watchdog Timer (WDT)	x	x	x
Programmable Interrupt Timer	2	2	2
Four-Channel General Purpose Timer	x	x	x
32-bit DMA Timers	4	4	4
QSPI	x	x	x
UART(s)	3	3	3
I^2C	x	x	x
Eight/Four-channel 8/16-bit PWM Timer	x	x	x
General Purpose I/O Module (GPIO)	x	x	x

Table 1. MCF5213 Family Configurations (continued)

Module	5211	5212	5213
Chip Configuration and Reset Controller Module	x	x	x
Background Debug Mode (BDM)	x	x	x
JTAG - IEEE 1149.1 Test Access Port[1]	x	x	x
Package	64 LQFP 64 QFN 81 MAPBGA	64 LQFP 81 MAPBGA	81 MAPBGA 100 LQFP

NOTES:
1 The full debug/trace interface is available only on the 100-pin packages. A reduced debug interface is bonded on smaller packages.

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the MCF5213. Package options for this family are described later in this document.

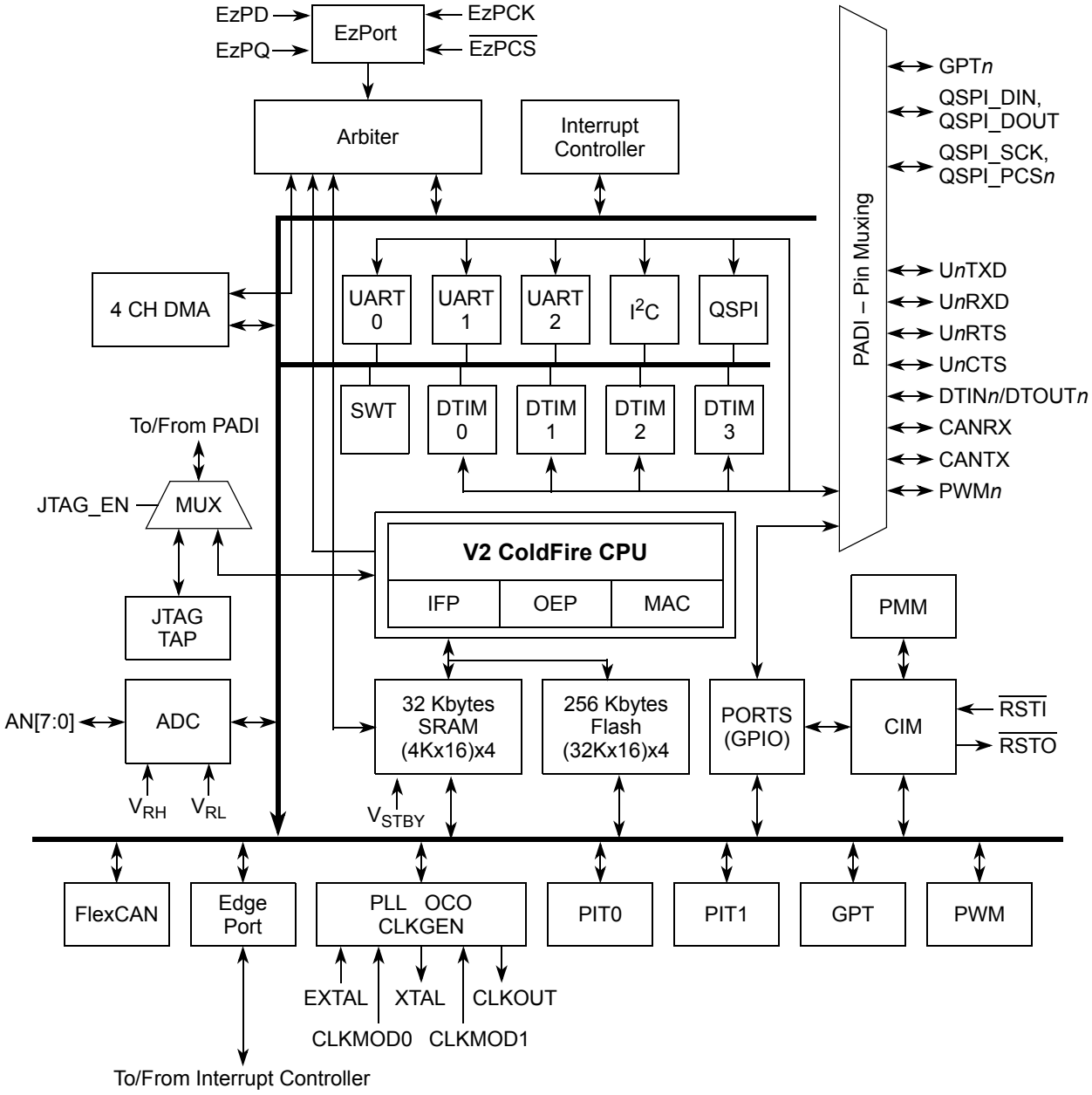


Figure 1. MCF5213 Block Diagram

1.2 Features

The MCF5213 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
  - — Static operation
  - — 32-bit address and data paths on-chip
  - — Up to 80 MHz processor core frequency

  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
  - Illegal instruction decode that allows for 68K emulation support
- System debug support
  - Real time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) that can be configured into a 1- or 2-level trigger
- On-chip memories
  - 32-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - 256 Kbytes of interleaved Flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used
- FlexCAN 2.0B module
  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard Data and Remote Frames (up to 109 bits long)
    - Extended Data and Remote Frames (up to 127 bits long)
    - 0–8 bytes data length
    - Programmable bit rate up to 1 Mbit/sec
  - Flexible Message Buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global for MBs 0-13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - “Time stamp” based on 16-bit free-running timer

  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- I^2C module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 μs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - Unused analog channels can be used as digital I/O
- Four 32-bit DMA timers
  - 12.5-ns resolution at 80 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler

  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low power mode support
- Clock generation features
  - 1 to 16 MHz crystal, 8 MHz on-chip relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator
  - 2 to 10 MHz reference frequency for normal PLL mode
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - 2^n ($n \leq 0 \leq 15$) low-power divider for extremely low frequency operation

- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4 x 32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)
  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number

- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.1 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF5213 core includes the multiply-accumulate (MAC) unit for improved signal processing capabilities. The MAC implements a three-stage arithmetic pipeline, optimized for 16 x 16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The MAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.2 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access debug information and real-time tracing capability is provided on 100-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. The MCF5213 implements revision B+ of the coldfire Debug Architecture.

The MCF5213's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event, thereby ensuring that the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand

data, and branch target addresses defining processor activity at the CPU's clock rate. The MCF5213 includes a new debug signal, ALLPST. This signal is the logical 'AND' of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.3 JTAG

The MCF5213 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5213 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF5213 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF5213 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.4 On-Chip Memories

1.2.4.1 SRAM

The SRAM module provides a general-purpose 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 32-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.4.2 Flash

The ColdFire Flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 32K x 16-bit Flash arrays to generate 256 Kbytes of 32-bit Flash memory. These arrays serve as electrically erasable and programmable, non-volatile program and data memory. The Flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high

voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller which supports interleaved accesses from the 2-cycle Flash arrays. A backdoor mapping of the Flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial Flash programming interface that allows the Flash to be read, erased and programmed by an external controller in a format compatible with most SPI bus Flash memory chips.

1.2.5 Power Management

The MCF5213 incorporates several low power modes of operation which are entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.2.6 FlexCAN

The FlexCAN module is a communication controller implementing version 2.0 of the CAN protocol parts A and B. The CAN protocol can be used as an industrial control serial data bus, meeting the specific requirements of reliable operation in a harsh EMI environment with high bandwidth. This instantiation of FlexCAN has 16 message buffers.

1.2.7 UARTs

The MCF5213 has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.8 I^2C Bus

The I^2C bus is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.9 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.10 Fast ADC

The Fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, perform a scan whenever triggered, or perform a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for either *sequential* or *simultaneous* conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.11 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the MCF5213. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTINx signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler which clocks the actual timer counter register (TCRn). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.12 General Purpose Timer (GPT)

The general purpose timer (GPT) is a 4-channel timer module consisting of a 16-bit programmable counter driven by a 7-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, one of the channels, channel 3, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.13 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can either count down from the value written in its PIT modulus register, or it can be a free-running down-counter.

1.2.14 Pulse Width Modulation Timers

The MCF5213 has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can thus be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.15 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.16 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. In order to improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.17 Interrupt Controller (INTC)

The MCF5213 has a single interrupt controller that supports up to 63 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining 7 sources are unassigned and may be used for software interrupt requests.

1.2.18 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a DCRn[START] bit or by the occurrence of certain UART or DMA timer events.

1.2.19 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer

- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software
- Low-voltage detector (LVD)

Control of the LVD and its associated reset and interrupt are handled by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

1.2.20 GPIO

Nearly all pins on the MCF5213 have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all 8 bits. Each port has registers that configure, monitor, and control the port pins.

1.3 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 2. Part Number Summary

Part Number	Flash / SRAM	Key Features	Package	Speed
MCF5211	128 Kbytes / 16 Kbytes	3 UARTs, I^2C, QSPI, A/D 16-/32-bit/PWM Timers	64 LQFP 81 MAPBGA 64 QFN	66 MHz 66, 80 MHz 66 MHz
MCF5212	256 Kbytes / 32 Kbytes	3 UARTs, I^2C, QSPI, A/D 16-/32-bit/PWM Timers	64 LQFP 81 MAPBGA	66 MHz 66, 80 MHz
MCF5213	256 Kbytes / 32 Kbytes	3 UARTs, I^2C, QSPI, A/D 16-/32-bit/PWM Timers, CAN	81 MAPBGA 100 LQFP	66, 80 MHz 66, 80 MHz

1.4 Package Pinouts

Figure 2 shows the pinout configuration for the 100 LQFP.

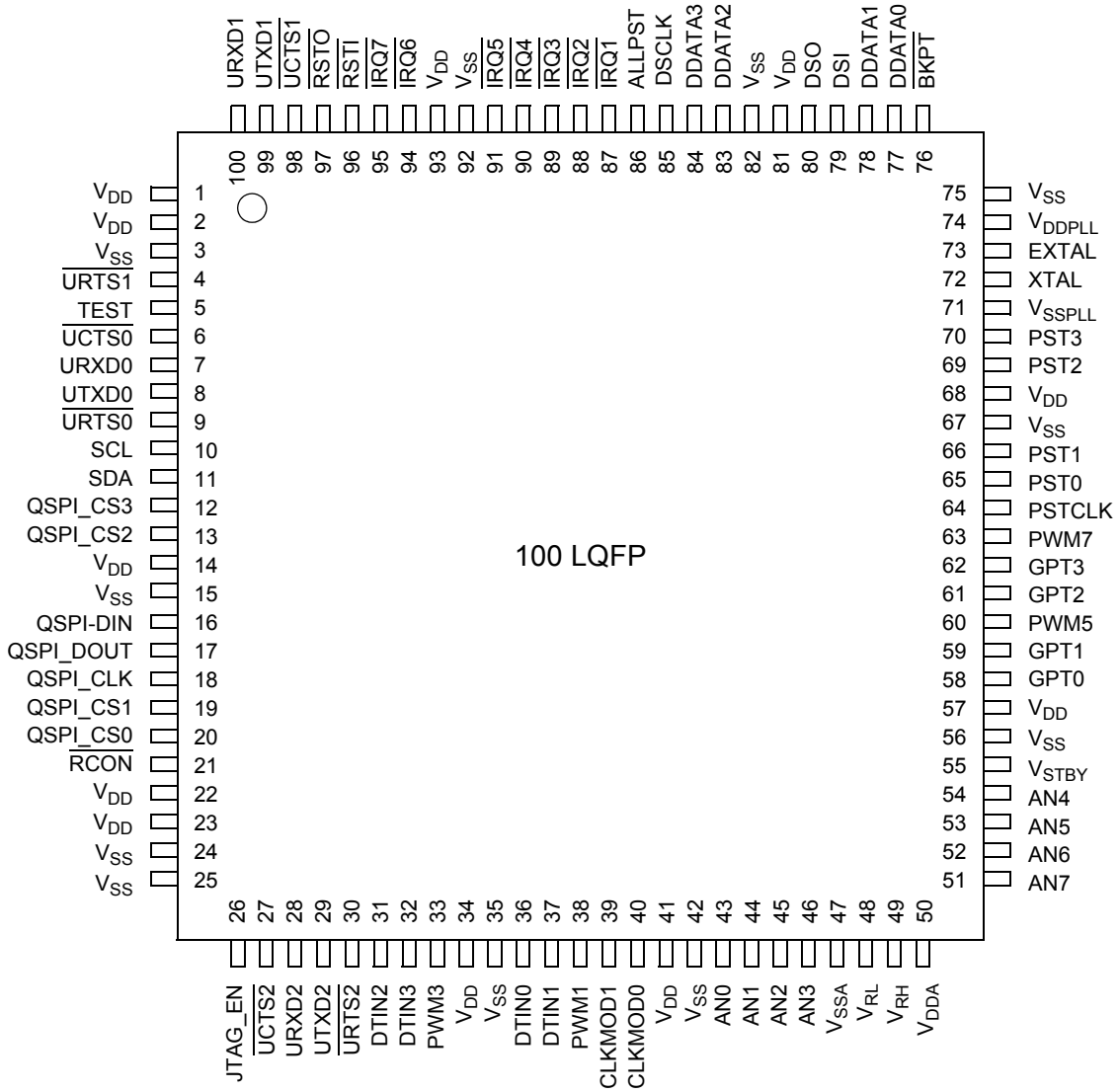


Figure 2. 100 LQFP Pin Assignments

Figure 3 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	VSS	UTXD1	$\overline{\text{RSTI}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ3}}$	ALLPST	TDO	TMS	VSS
B	$\overline{\text{URTS1}}$	URXD1	$\overline{\text{RSTO}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	$\overline{\text{TRST}}$	TDI	VDDPLL	EXTAL
C	$\overline{\text{UCTS0}}$	TEST	$\overline{\text{UCTS1}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ1}}$	TCLK	VSSPLL	XTAL
D	URXD0	UTXD0	$\overline{\text{URTS0}}$	VSS	VDD	VSS	PWM7	GPT3	GPT2
E	SCL	SDA	VDD	VDD	VDD	VDD	VDD	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	VSS	VDD	VSS	GPT0	VSTBY	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{\text{RCON}}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	VSSA	VDDA	AN7
J	VSS	JTAG_EN	DTIN2	PWM3	PWM1	AN0	VRL	VRH	VSSA

Figure 3. 81 MAPBGA Pin Assignments

Figure 4 shows the pinout configuration for the 64 LQFP and 64 QFN.

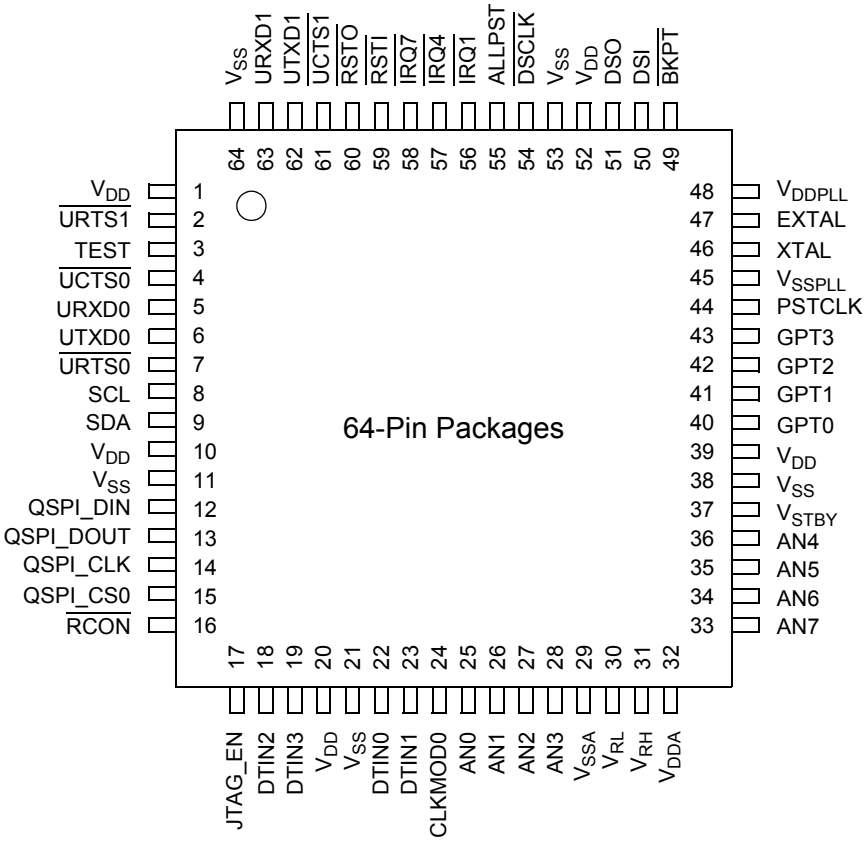


Figure 4. 64 LQFP and 64 QFN Pin Assignments

Table 3 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN	Notes
ADC	AN7	—	—	GPIO	Low	FAST	—	51	H9	33	
	AN6	—	—	GPIO	Low	FAST	—	52	G9	34	
	AN5	—	—	GPIO	Low	FAST	—	53	G8	35	
	AN4	—	—	GPIO	Low	FAST	—	54	F9	36	
	AN3	—	—	GPIO	Low	FAST	—	46	G7	28	
	AN2	—	—	GPIO	Low	FAST	—	45	G6	27	
	AN1	—	—	GPIO	Low	FAST	—	44	H6	26	
	AN0	—	—	GPIO	Low	FAST	—	43	J6	25	
	SYNCA	—	—	—	N/A	N/A	—	—	—	—	No Primary
	SYNCB	—	—	—	N/A	N/A	—	—	—	—	No Primary
	VDDA	—	—	—	N/A	N/A	—	50	H8	32	
	VSSA	—	—	—	N/A	N/A	—	47	H7	29	
	VRH	—	—	—	N/A	N/A	—	49	J8	31	
	VRL	—	—	—	N/A	N/A	—	48	J7	30	
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	73	B9	47	
	XTAL	—	—	—	N/A	N/A	—	72	C9	46	
	VDDPLL	—	—	—	N/A	N/A	—	74	B8	48	
	VSSPLL	—	—	—	N/A	N/A	—	71	C8	45	
Debug Data	ALLPST	—	—	—	High	FAST	—	86	A6	55	
	DDATA[3:0]	—	—	GPIO	High	FAST	—	84,83,78,77	—	—	
	PST[3:0]	—	—	GPIO	High	FAST	—	70,69,66,65	—	—	
I^2C	SCL	CANTX[3]	UTXD2	GPIO	PDSR[0]	PSRR[0]	pull-up[4]	10	E1	8	
	SDA	CANRX[3]	URXD2	GPIO	PDSR[0]	PSRR[0]	pull-up[4]	11	E2	9	

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN	Notes
Interrupts	IRQ7	—	—	GPIO	Low	FAST	—	95	C4	58	
	IRQ6	—	—	GPIO	Low	FAST	—	94	B4	—	
	IRQ5	—	—	GPIO	Low	FAST	—	91	A4	—	
	IRQ4	—	—	GPIO	Low	FAST	—	90	C5	57	
	IRQ3	—	—	GPIO	Low	FAST	—	89	A5	—	
	IRQ2	—	—	GPIO	Low	FAST	—	88	B5	—	
	IRQ1	SYNCA	PWM1	GPIO	High	FAST	pull-up[4]	87	C6	56	
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	26	J2	17	
	TCLK/ PSTCLK	CLKOUT	—	—	High	FAST	pull-up[5]	64	C7	44	
	TDI/DSI	—	—	—	N/A	N/A	pull-up[5]	79	B7	50	
	TDO/DSO	—	—	—	High	FAST	—	80	A7	51	
	TMS /$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	pull-up[5]	76	A8	49	
	TRST /DSCLK	—	—	—	N/A	N/A	pull-up[5]	85	B6	54	
Mode Selection[6]	CLKMOD0	—	—	—	N/A	N/A	pull-down[6]	40	G5	24	
	CLKMOD1	—	—	—	N/A	N/A	pull-down[6]	39	H5	—	
	RCON/ EZPCS	—	—	—	N/A	N/A	pull-up	21	G3	16	
PWM	PWM7	—	—	GPIO	PDSR[31]	PSRR[31]	—	63	D7	—	
	PWM5	—	—	GPIO	PDSR[30]	PSRR[30]	—	60	E8	—	
	PWM3	—	—	GPIO	PDSR[29]	PSRR[29]	—	33	J4	—	
	PWM1	—	—	GPIO	PDSR[28]	PSRR[28]	—	38	J5	—	

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN	Notes
QSPI	QSPI_DIN/ EZPD	CANRX[3]	RXD1	GPIO	PDSR[2]	PSRR[2]	—	16	F3	12	
	QSPI_DOUT /EZPQ	CANTX[3]	TXD1	GPIO	PDSR[1]	PSRR[1]	—	17	G1	13	
	QSPI_CLK/ EZPCK	SCL	RTS1	GPIO	PDSR[3]	PSRR[3]	pull-up[7]	18	G2	14	
	QSPI_CS3	SYNCA	SYNCB	GPIO	PDSR[7]	PSRR[7]	—	12	F1	—	
	QSPI_CS2	—	—	GPIO	PDSR[6]	PSRR[6]	—	13	F2	—	
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19	H2	—	
	QSPI_CS0	SDA	CTS1	GPIO	PDSR[4]	PSRR[4]	pull-up[7]	20	H1	15	
Reset[8]	RSTI	—	—	—	N/A	N/A	pull-up[8]	96	A3	59	
	RSTO	—	—	—	high	FAST	—	97	B3	60	
Test	TEST	—	—	—	N/A	N/A	pull-down	5	C2	3	
Timers, 16-bit	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up[9]	62	D8	43	
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up[9]	61	D9	42	
	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up[9]	59	E9	41	
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up[9]	58	F7	40	
Timers, 32-bit	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32	H3	19	
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31	J3	18	
	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37	G4	23	
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36	H4	22	
UART 0	UCTS0	CANRX	—	GPIO	PDSR[11]	PSRR[11]	—	6	C1	4	
	URTS0	CANTX	—	GPIO	PDSR[10]	PSRR[10]	—	9	D3	7	
	URXD0	—	—	GPIO	PDSR[9]	PSRR[9]	—	7	D1	5	
	UTXD0	—	—	GPIO	PDSR[8]	PSRR[8]	—	8	D2	6	

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN	Notes
UART 1	UCTS1	SYNCA	URXD2	GPIO	PDSR[15]	PSRR[15]	—	98	C3	61	
	URTS1	SYNCB	UTXD2	GPIO	PDSR[14]	PSRR[14]	—	4	B1	2	
	URXD1	—	—	GPIO	PDSR[13]	PSRR[13]	—	100	B2	63	
	UTXD1	—	—	GPIO	PDSR[12]	PSRR[12]	—	99	A2	62	
UART 2	UCTS2	—	—	GPIO	PDSR[27]	PSRR[27]	—	27	—	—	
	URTS2	—	—	GPIO	PDSR[26]	PSRR[26]	—	30	—	—	
	URXD2	—	—	GPIO	PDSR[25]	PSRR[25]	—	28	—	—	
	UTXD2	—	—	GPIO	PDSR[24]	PSRR[24]	—	29	—	—	
FlexCAN	CANRX				N/A	N/A	—	—	—	—	See Note[3,10]
	CANTX				N/A	N/A	—	—	—	—	See Note[3,10]
VSTBY	VSTBY	—	—	—	N/A	N/A	—	55	F8	37	
VDD	VDD	—	—	—	N/A	N/A	—	1,2,14,22, 23,34,41, 57,68,81,93	D5,E3–E7, F5	1,10,20,39, 52	
VSS	VSS	—	—	—	N/A	N/A	—	3,15,24,25, 35,42,56, 67,75,82,92	A1,A9,D4, D6,F4,F6, J1	11,21,38, 53,64	

NOTES:
1 The PDSR and PSSR registers are described in the Ports/GPIO chapter of the MCF5213 Reference Manual. All programmable signals default to 2mA drive and FAST slew rate in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 The multiplexed CANTX and CANRX signals are not available on the MCF5211 or MCF5212
4 For primary and GPIO functions only.
5 Only when JTAG mode is enabled.
6 CLKMOD0 and CLKMOD1 have internal pull-down resistors, however the use of external resistors is very strongly recommended
7 For secondary and GPIO functions only.
8 RSTI has an internal pull-up resistor, however the use of an external resistor is very strongly recommended
9 For GPIO function. Primary Function has pull-up control within the GPT module
10 CANTX and CANRX are secondary functions only.

1.5 Reset Signals

Table 4 describes signals that are used to either reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 512 CPU clocks after the reset source has deasserted.	O

1.6 PLL and Clock Signals

Table 5 describes signals that are used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used.	I
Crystal	XTAL	Crystal oscillator output except when CLKMOD1=1, then sampled as part of the clockmode selection mechanism.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.7 Mode Selection

Table 6 describes signals used in mode selection, Table 7 describes particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Selects the clock boot mode.	I
Reset Configuration	$\overline{\text{RCON}}$	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the Flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

Table 7. Clocking Modes

CLKMOD[1:0]	XTAL	Configure the clock mode.
00	0	PLL disabled, clock driven by external oscillator
00	1	PLL disabled, clock driven by on-chip oscillator
01	N/A	PLL disabled, clock driven by crystal
10	0	PLL in normal mode, clock driven by external oscillator
10	1	PLL in normal mode, clock driven by on-chip oscillator
11	N/A	PLL in normal mode, clock driven by crystal

1.8 External Interrupt Signals

Table 8 describes the external interrupt signals.

Table 8. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[7:1]	External interrupt sources.	I

1.9 Queued Serial Peripheral Interface (QSPI)

Table 9 describes QSPI signals.

Table 9. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip selects that can be programmed to be active high or low.	O

1.10 I²C I/O Signals

Table 10 describes the I²C serial interface module signals.

Table 10. I²C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I²C interface. Either it is driven by the I²C module when the bus is in master mode or it becomes the clock input when the I²C is in slave mode.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I²C interface.	I/O

1.11 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I
Clear-to-Send	$\overline{\text{UCTS}}n$	Indicate to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}}n$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.12 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT	Programmable output from the DMA timer modules.	O

1.13 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the A-to-D converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise	—
	V_{SSA}		—

1.14 General Purpose Timer Signals

Table 14 describes the General Purpose Timer Signals.

Table 14. GPT Signals

Signal Name	Abbreviation	Function	I/O
General Purpose Timer Input/Output	GPT[3:0]	Inputs to or outputs from the general purpose timer module	I/O

1.15 Pulse Width Modulator Signals

Table 15 describes the PWM signals.

Table 15. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channels	PWM[7:0]	Pulse width modulated output for PWM channels	O

1.16 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and also to interface to the BDM logic.

Table 16. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
JTAG Enable	JTAG_EN	Select between debug module and JTAG signals at reset	I
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock-Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint - Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status/debug data signals (PST[3:0]PSTDDATA[7:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I
Development Serial Input	DSI	Development Serial Input -Internally synchronized input that provides data input for the serial communication port to the debug module, once the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output -Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical “AND” of PST[3.0]	O

1.17 EzPort Signal Descriptions

Table 17 contains a list of EzPort external signals

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers	I
EzPort Chip Select	$\overline{\text{EZPCS}}$	Chip select for signalling the start and end of serial transfers	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK	O

1.18 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function	I/O
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.	I
Positive Supply	VDD	These pins supply positive power to the core logic.	I
Ground	VSS	This pin is the negative supply (ground) to the chip.	

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF5213 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5213.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 19. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	– 0.3 to +4.0	V
Clock Synthesizer Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
RAM Memory Standby Supply Voltage	V_{STBY}	– 0.3 to + 4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous Maximum Current Single pin limit (applies to all pins) [4, 5]	I_{DD}	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

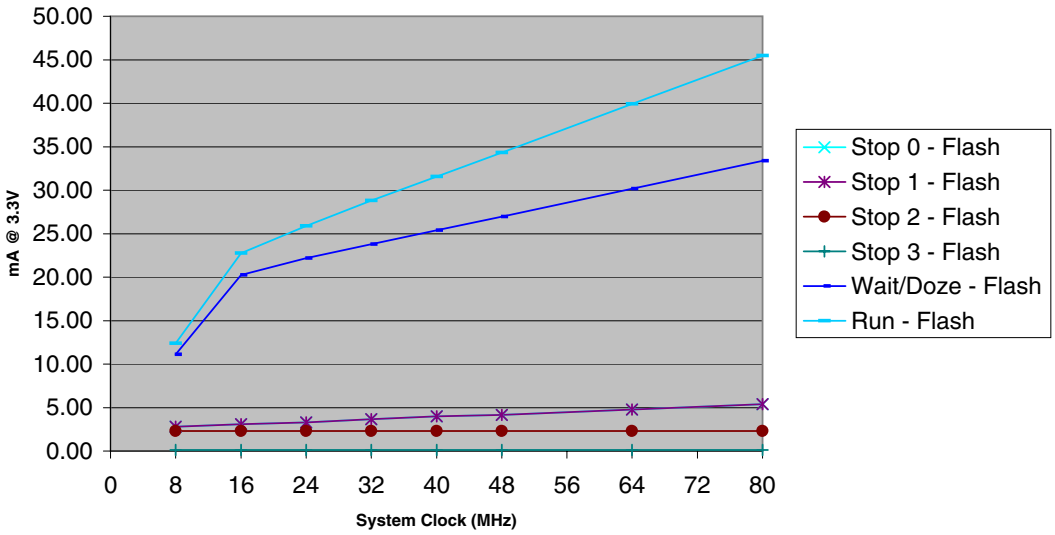
NOTES:
1. Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).
3. Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
5. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock).Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

2.2 Current Consumption

Table 20. Current Consumption in Low-Power Mode[1,2]

Mode	8MHz (Typ)[3]	16MHz (Typ)[2]	64MHz (Typ)[2]	80MHz (Typ)[2]	80MHz (Peak)[4]	Units
Stop Mode 3 (Stop 11)[5]	0.13				TBD	mA
Stop Mode 2 (Stop 10)[5]	2.29				TBD	
Stop Mode 1 (Stop 01)[5,6]	2.80	3.08	4.76	5.38	TBD	
Stop Mode 0 (Stop 00)[5]	2.80	3.08	4.76	5.39	TBD	
Wait / Doze	11.12	20.23	30.17	33.36	TBD	
Run	12.40	22.74	39.92	45.47	TBD	

NOTES:
1. All values are measured with a 3.30V power supply
2. Refer to the Power Management chapter in the MCF5213 Reference Manual for more information on low-power modes.
3. CLKOUT and all peripheral clocks except UART0 and CFM off before entering low power mode. CLKOUT is disabled. All code executed from FLASH. Code run from SRAM reduces power consumption further. Tests performed at room temperature.
4. CLKOUT and all peripheral clocks on before entering low power mode. All code is executed from FLASH. All code is executed at 80MHz clock.
5. See the description of the Low-Power Control Register (LCPR) in the MCF5213 Reference Manual for more information on Stop modes 0–3.
6. Results are identical to STOP 00 for typical values since they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low power mode.



Typical Current Consumption in Low-Power Modes

Table 21. Typical Active Current Consumption Specifications

Characteristic	Symbol	Typical[1] Active (SRAM)	Typical[1] Active (Flash)	Peak[2]	Unit
• 1 MHz core & I/O	I_{DD}	TBD	3.48	TBD	mA
• 8 MHz core & I/O		7.28	13.37	19.02	
• 16 MHz core & I/O		12.08	25.08	35.66	
• 64 MHz core & I/O		40.14	54.62	85.01	
• 80 MHz core & I/O		49.2	64.09	100.03	
RAM Memory Standby Supply Current Normal Operation: $V_{DD} > V_{STBY}$ - 0.3 V Transient Condition: V_{STBY} - 0.3 V > $V_{DD} > V_{SS}$ + 0.5 V Standby Operation: $V_{DD} < V_{SS}$ + 0.5 V	I_{STBY}	0 TBD TBD		TBD TBD TBD	µA mA µA
Analog Supply Current Normal Operation Low-Power Stop	I_{DDA}	— —	— —	TBD TBD	mA µA

NOTES:
1 Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from Flash).
2 Peak current measured with all modules active, and default drive strength with matching load.

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single Layer board (1s)	θ_{JA}	53[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single Layer board (1s)	θ_{JMA}	42[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33[1,3]	°C/W
	Junction to board		θ_{JB}	25[4]	°C/W
	Junction to case		θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature		T_j	105	°C
81 MAPBGA	Junction to ambient, natural convection	Single Layer board (1s)	θ_{JA}	61[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35[2,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single Layer board (1s)	θ_{JMA}	50[2,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31[2,3]	°C/W
	Junction to board		θ_{JB}	20[4]	°C/W
	Junction to case		θ_{JC}	12[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature		T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36[1,3]	°C/W
	Junction to board		θ_{JB}	26[4]	°C/W
	Junction to case		θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature		T_j	105	°C

Table 22. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
64 QFN	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	68[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	24[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	55[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	19[1,3]	°C/W
	Junction to board		θ_{JB}	8[4]	°C/W
	Junction to case (bottom)		θ_{JC}	0.6[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	3[6]	°C/W
	Maximum operating junction temperature		T_j	105	°C

NOTES:
1. θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.
3. Per JEDEC JESD51-6 with the board JESD51-7) horizontal.
4. Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The Flash memory characteristics are shown in Table 23 and Table 24.

Table 23. SGFM Flash Program and Erase Characteristics

(V_{DDF} = 2.7 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	80	MHz
System clock (program/erase)[1]	$f_{sys(P/E)}$	0.15	—	80	MHz

NOTES:
1 Refer to the Flash section for more information

Table 24. SGFM Flash Module Life Characteristics

(V_{DDF} = 2.7 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

NOTES:
1 A program/erase cycle is defined as switching the bits from 1 → 0 → 1.
2 Reprogramming of a Flash array block prior to erase is not required.

2.5 ESD Protection

Table 25. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	ohms
	C	100	pF
MM Circuit Description	R_{series}	0	ohms
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

NOTES:
1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.6 DC Electrical Specifications

Table 26. DC Electrical Specifications [1]

Characteristic	Symbol	Min	Max	Unit
Supply Voltage	V_{DD}	3.0	3.6	V
Input High Voltage	V_{IH}	0.7 x V_{DD}	4.0	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x V_{DD}	V
Input Hysteresis	V_{HYS}	0.06 x V_{DD}	—	mV
Input Leakage Current V_{in} = V_{DD} or V_{SS}, digital pins	I_{in}	–1.0	1.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	OV_{DD} - 0.5	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 2.0mA	V_{OL}	—	0.5	V
Output High Voltage (High Drive) I_{OH} = TBD	V_{OH}	OV_{DD} - 0.5	—	V
Output Low Voltage (High Drive) I_{OL} = TBD	V_{OL}	—	0.5	V
Output High Voltage (Low Drive) I_{OH} = TBD	V_{OH}	OV_{DD} - 0.5	—	V
Output Low Voltage (Low Drive) I_{OL} = TBD	V_{OL}	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	-10	- 130	µA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

NOTES:
1 Refer to Table 27 for additional PLL specifications.
2 Refer to the MCF5213 signals chapter for pins having weak internal pull-up devices.
3 This parameter is characterized before qualification rather than 100% tested.

2.7 Clock Source Electrical Specifications

Table 27. PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
PLL Reference Frequency Range Crystal reference External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 2 2	 10.0 10.0	MHz
System Frequency [1] External Clock Mode On-Chip PLL Frequency	f_{sys}	 0 f_{ref} / 32	 80 80	MHz
Loss of Reference Frequency [2, 4]	f_{LOR}	100	1000	kHz
Self Clocked Mode Frequency [3, 4]	f_{SCM}	1	5	MHz
Crystal Start-up Time [4, 5]	t_{cst}	—	10	ms

Table 27. PLL Electrical Specifications (continued)

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
EXTAL Input High Voltage External reference	V_{IHEXT}	 2.0	 V_{DD}	V
EXTAL Input Low Voltage External reference	V_{ILEXT}	 V_{SS}	 0.8	V
PLL Lock Time[4,6]	t_{lpll}	—	500	µs
Duty Cycle of reference [4]	t_{dc}	40	60	% f_{ref}
Frequency un-LOCK Range	f_{UL}	- 1.5	1.5	% f_{ref}
Frequency LOCK Range	f_{LCK}	- 0.75	0.75	% f_{ref}
CLKOUT Period Jitter [4, 5, 7, 7,8], Measured at f_{SYS} Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

NOTES:
1 All internal registers retain data at 0 Hz.
2 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
3 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
4 This parameter is characterized before qualification rather than 100% tested.
5 Proper PC board layout procedures must be followed to achieve specifications.
6 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
7 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the Cjitter percentage for a given interval
8 Based on slow system clock of 40 MHz measured at f_{sys} max.

2.8 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, TIMERS, UARTS, FEC0, FEC1, Interrupts and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 28 and Figure 5.

Table 28. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	-	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	-	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	-	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	-	ns

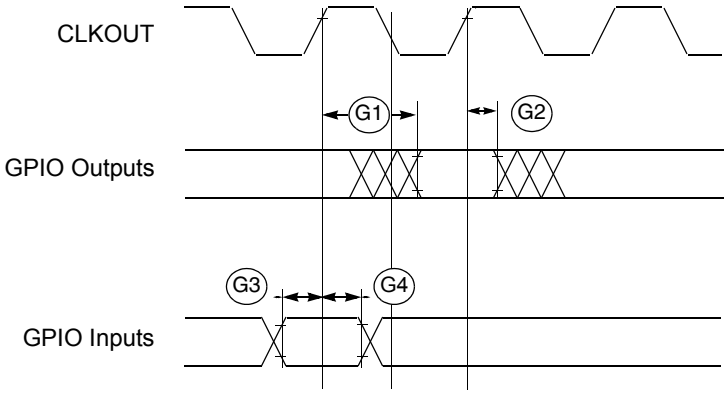


Figure 5. GPIO Timing

2.9 Reset Timing

Table 29. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ Input valid to CLKOUT High	t_{RVCH}	9	-	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	-	ns
R3	$\overline{RSTI}$ Input valid Time [2]	t_{RIVT}	5	-	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	-	10	ns

NOTES:
1 All AC timing is shown with respect to 50% O V_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.

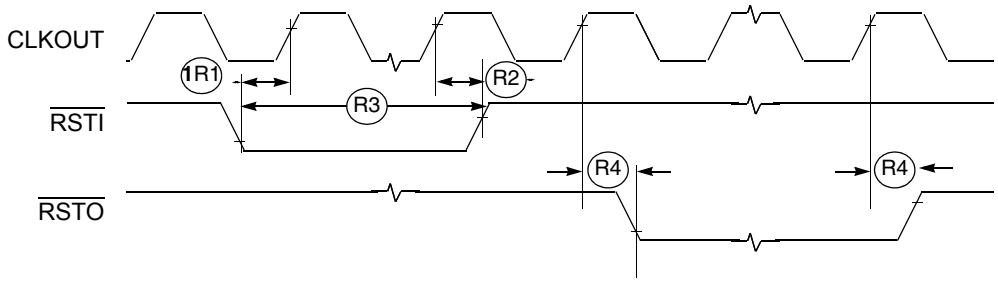


Figure 6. $\overline{RSTI}$ and Configuration Override Timing

2.10 I²C Input/Output Timing Specifications

Table 30 lists specifications for the I²C input timing parameters shown in Figure 7.

Table 30. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	2 x t_{CYC}	—	ns
I2	Clock low period	8 x t_{CYC}	—	ns
I3	SCL/SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	mS
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	mS
I6	Clock high time	4 x t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 x t_{CYC}	—	ns
I9	Stop condition setup time	2 x t_{CYC}	—	ns

Table 31 lists specifications for the I²C output timing parameters shown in Figure 7.

Table 31. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11[1]	Start condition hold time	6 x t_{CYC}	—	ns
I2[1]	Clock low period	10 x t_{CYC}	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µS
I4[1]	Data hold time	7 x t_{CYC}	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6[1]	Clock high time	10 x t_{CYC}	—	ns
I7[1]	Data setup time	2 x t_{CYC}	—	ns
I8[1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9[1]	Stop condition setup time	10 x t_{CYC}	—	ns

NOTES:
1. Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 31. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 31 are minimum values.
2. Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
3. Specified at a nominal 50-pF load.

Figure 7 shows timing for the values in Table 30 and Table 31.

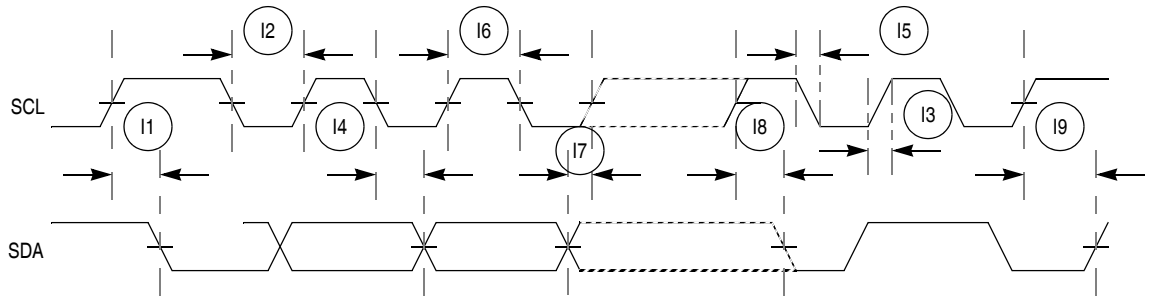


Figure 7. I²C Input/Output Timings

2.11 Analog-to-Digital Converter (ADC) Parameters

Table 32 lists specifications for the analog-to-digital converter.

Table 32. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
R_{ES}	Resolution	12	—	12	Bits
INL	Integral Non-Linearity (Full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral Non-Linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential Non-Linearity	—	-1 < DNL < +1	<+1	LSB
	Monotonicity	GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion Range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 8	—	pF
X_{IN}	Input impedance		See Figure 8		Ω
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	μ
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain Error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	TBD	mV
SNR	Signal-to-Noise ratio	TBD	62 to 66		dB

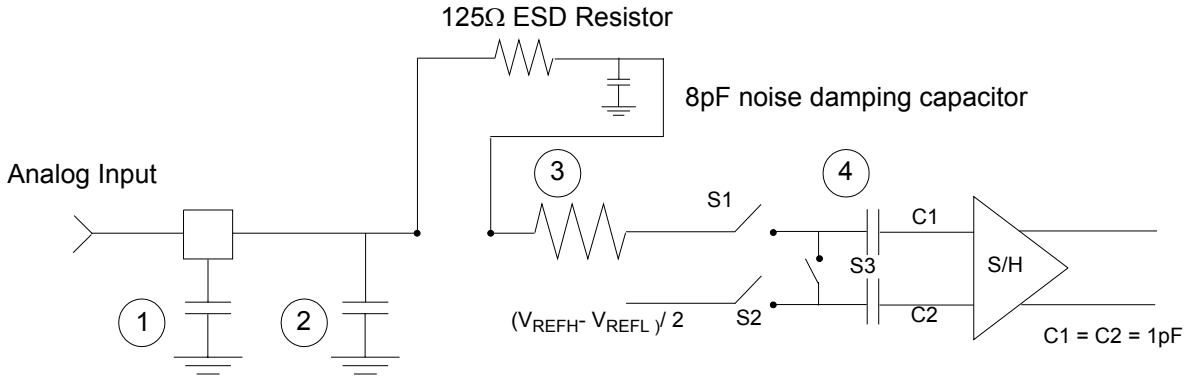
Table 32. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
THD	Total Harmonic Distortion	TBD	-75		dB
SFDR	Spurious Free Dynamic Range	TBD	67 to 70.3		dB
SINAD	Signal-to-Noise plus Distortion	TBD	61 to 63.9		dB
ENOB	Effective Number OF Bits	9.1	10.6		Bits

NOTES:
1 All measurements are preliminary pending full characterization, and were made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
3 LSB = Least Significant Bit
4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
5 Includes power-up of ADC and V_{REF}
6 ADC clock cycles
7 The current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.11.1 Equivalent Circuit for ADC Inputs

Figure 10-17 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). Note that there are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. Equivalent resistance for the channel select mux; 100 ohms
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF

5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times 1.4 \times 10^{-12}}$

Figure 8. Equivalent Circuit for A/D Loading

2.12 DMA Timers Timing Specifications

Table 33 lists timer module AC timings.

Table 33. Timer Module AC Timing Specifications

Name	Characteristic[1]	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	3 x t_{CYC}	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	1 x t_{CYC}	—	ns

NOTES:
1 All timing references to CLKOUT are given to its rising edge.

2.13 QSPI Electrical Specifications

Table 34 lists QSPI timings.

Table 34. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 34 correspond to Figure 9.

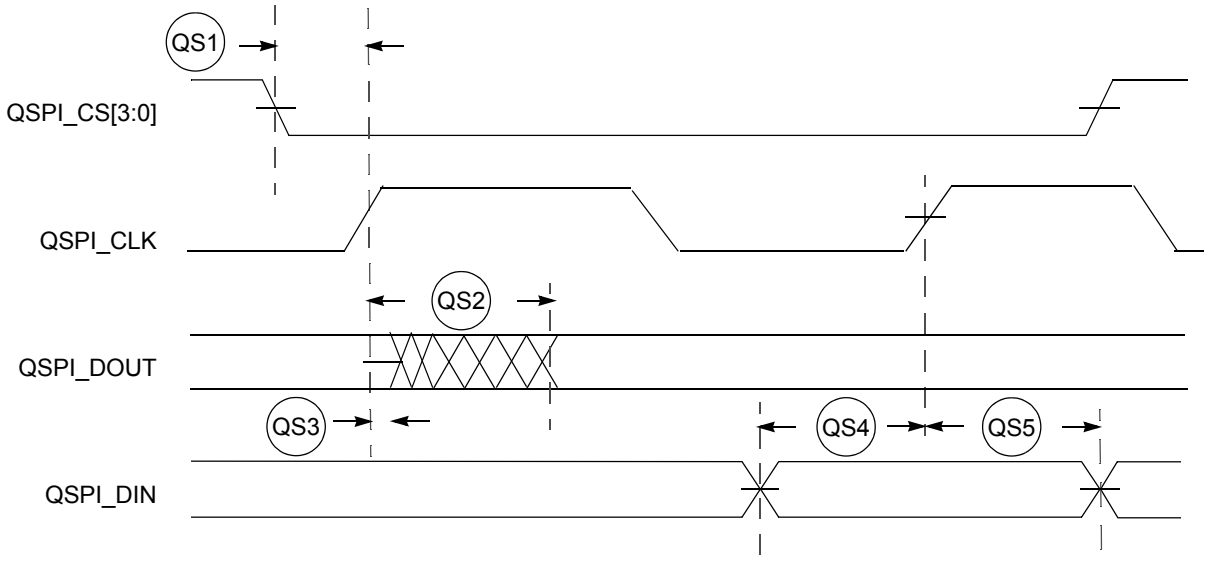


Figure 9. QSPI Timing

2.14 JTAG and Boundary Scan Timing

Table 35. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4 x t_{CYC}	-	ns
J3	TCLK Clock Pulse Width	t_{JCW}	26	-	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	-	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	-	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	-	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	-	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ Assert Time	t_{TRSTAT}	100	-	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	-	ns

NOTES:
1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

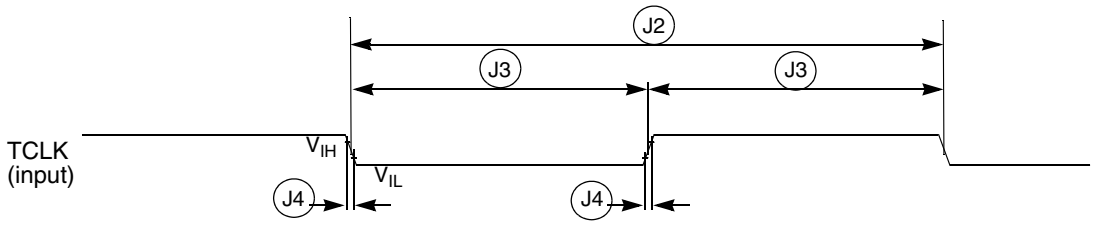


Figure 10. Test Clock Input Timing

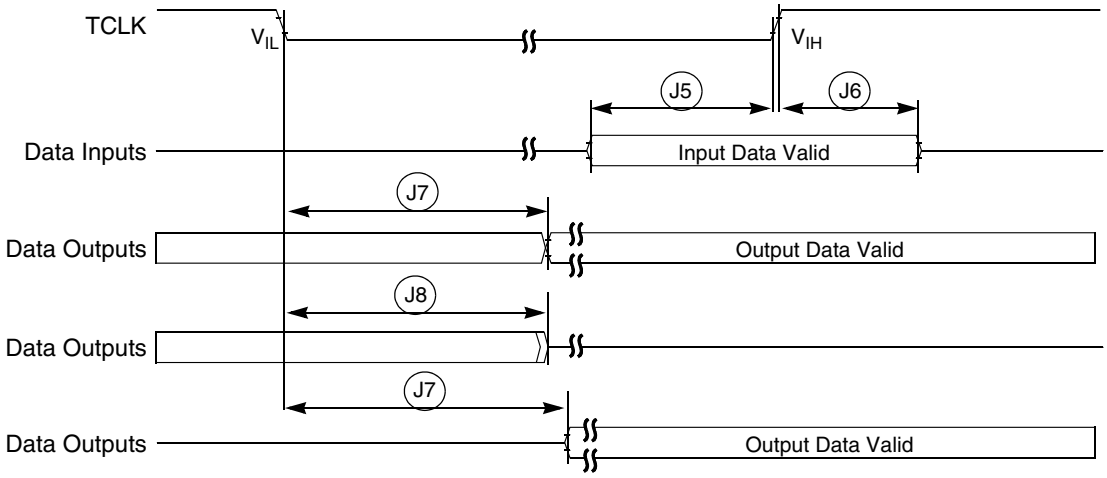


Figure 11. Boundary Scan (JTAG) Timing

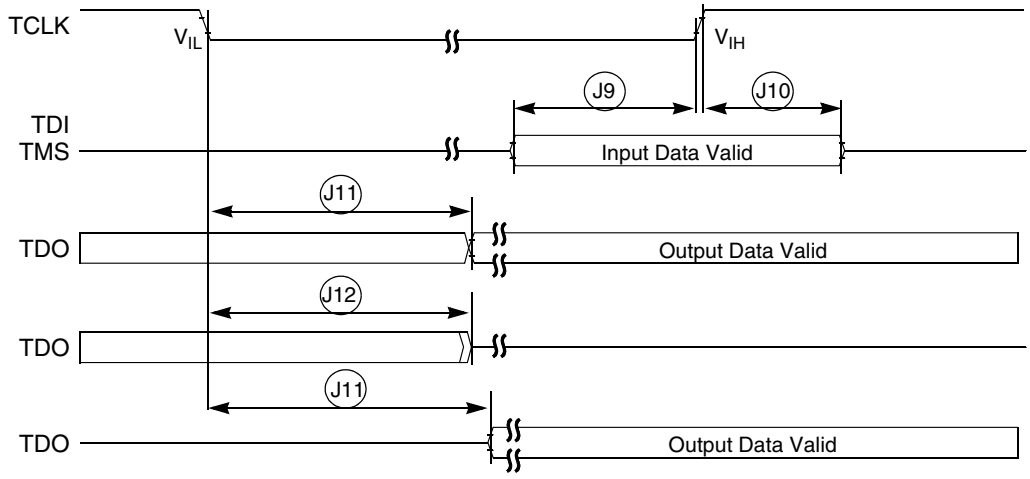


Figure 12. Test Access Port Timing

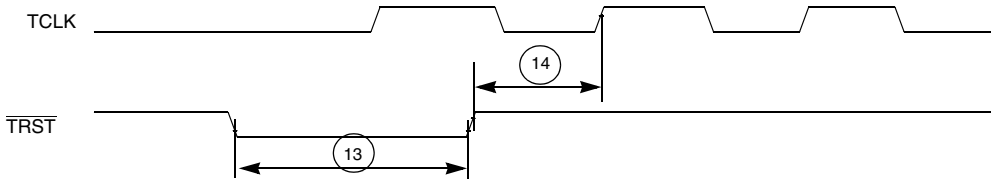


Figure 13. $\overline{\text{TRST}}$ Timing

2.15 Debug AC Timing Specifications

Table 36 lists specifications for the debug AC timing parameters shown in Figure 15.

Table 36. Debug AC Timing Specification

Num	Characteristic	166 MHz		Units
		Min	Max	
D0	PSTCLK cycle time		0.5	t_{CYC}
D1	PST, DDATA to CLKOUT setup	4		ns
D2	CLKOUT to PST, DDATA hold	1.5		ns
D3	DSI-to-DSCLK setup	1 x t_{CYC}		ns
D4[1]	DSCLK-to-DSO hold	4 x t_{CYC}		ns
D5	DSCLK cycle time	5 x t_{CYC}		ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT Rise	4		ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT Rise	1.5		ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

NOTES:
1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 14 shows real-time trace timing for the values in Table 36.

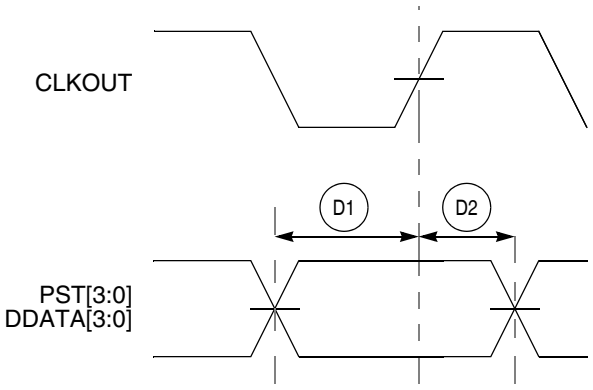


Figure 14. Real-Time Trace AC Timing

Figure 15 shows BDM serial port AC timing for the values in Table 36.

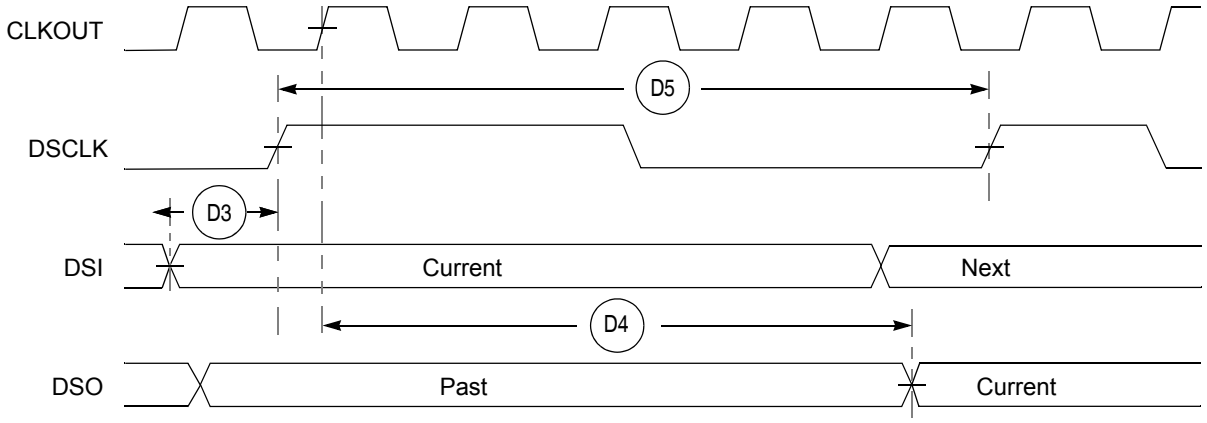
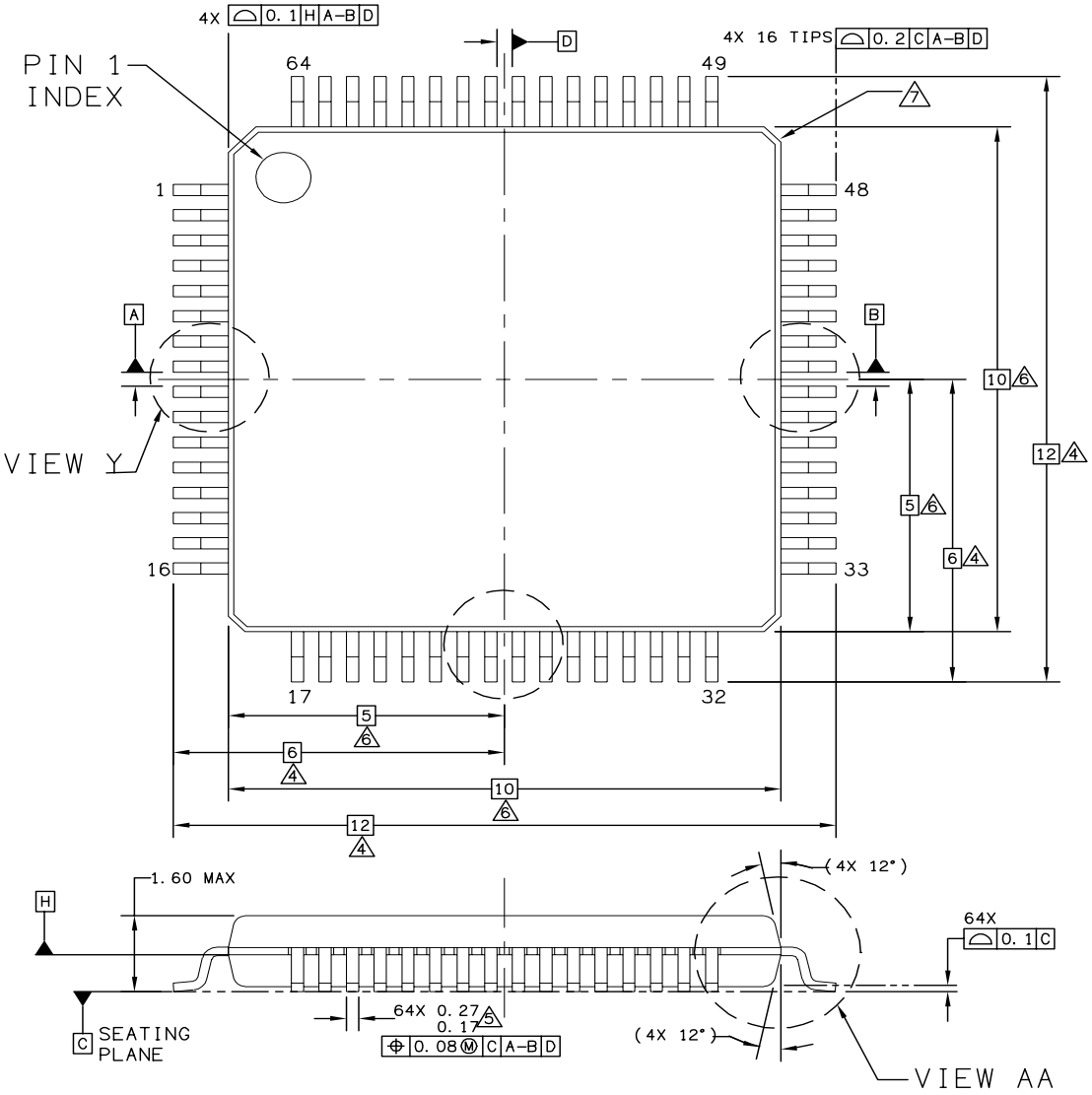


Figure 15. BDM Serial Port AC Timing

3 Mechanical Outline Drawings

This section describes the physical properties of the MCF5213 and its derivatives.



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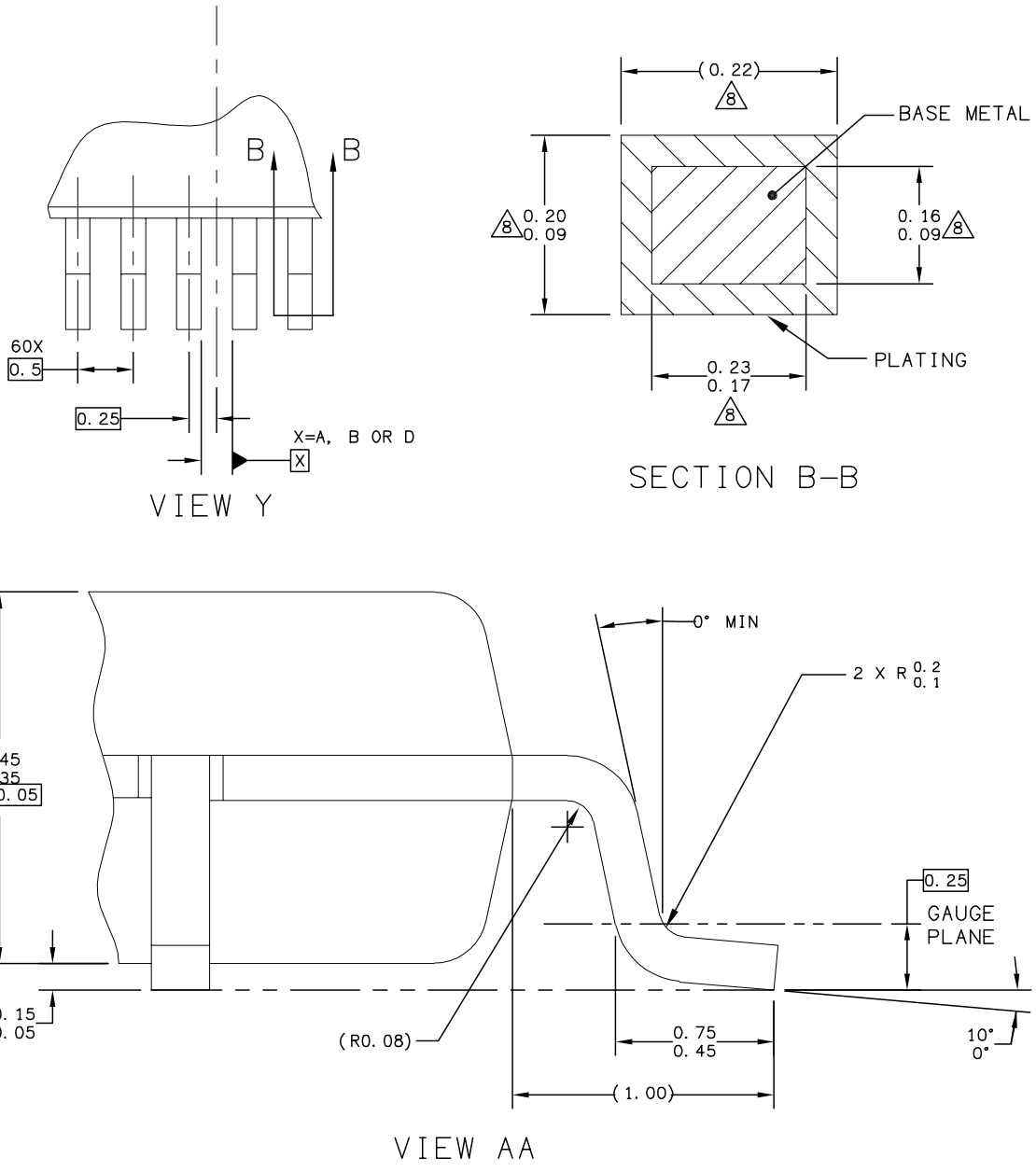
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	



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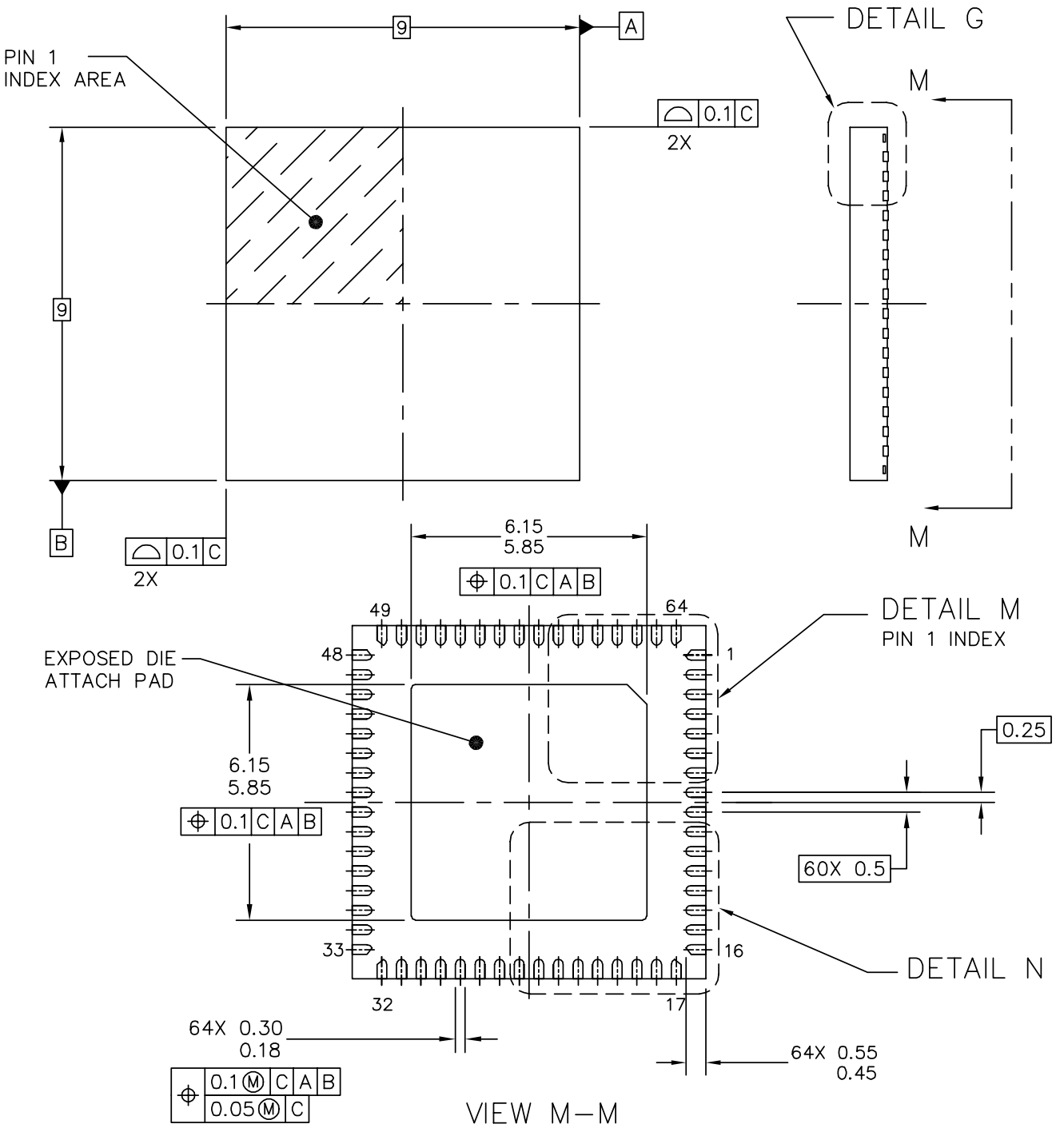
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

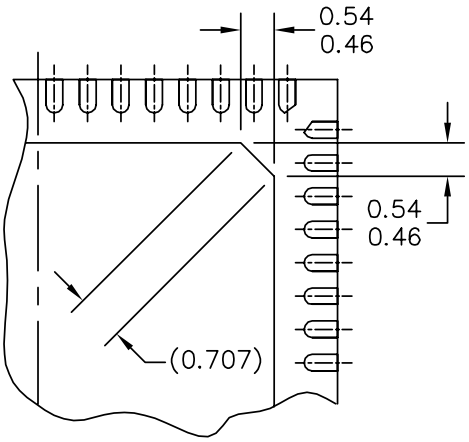
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

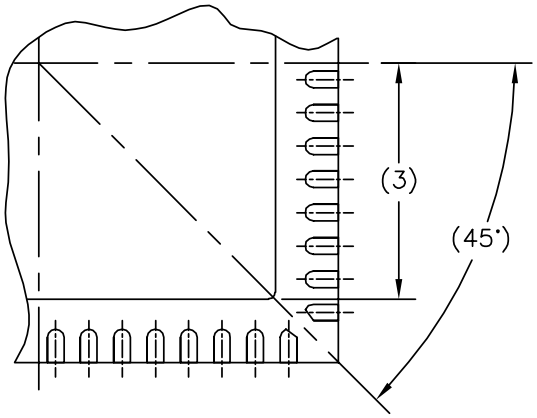
	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	



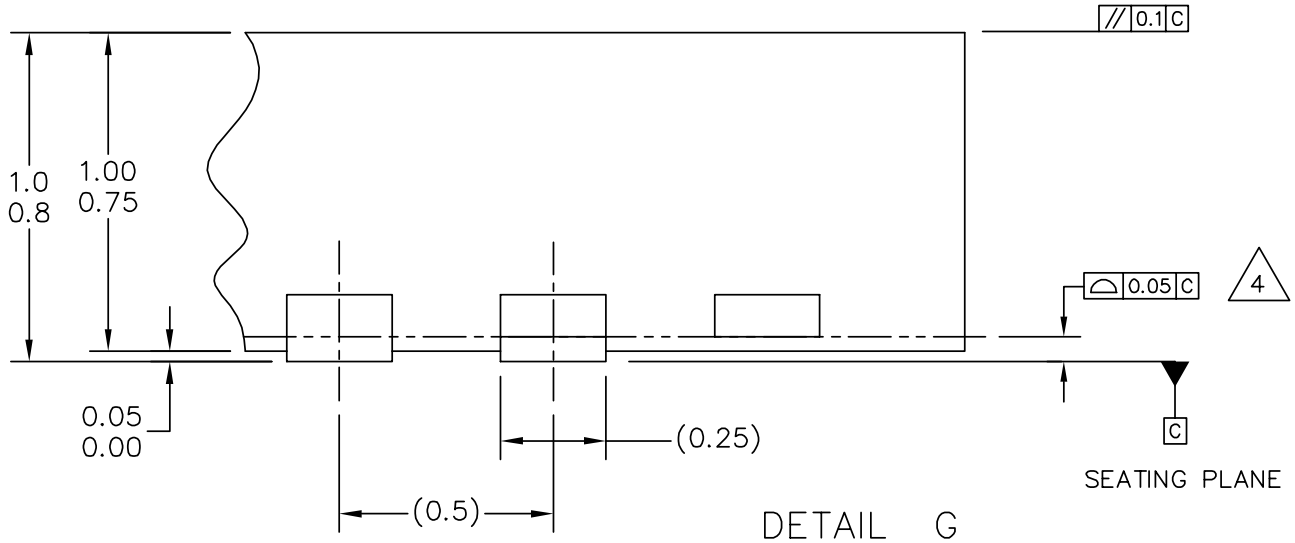
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740–01	
	STANDARD: JEDEC MO–220 VMMD–3	
	PACKAGE CODE: 6200	SHEET: 1 OF 4



DETAIL M
PREFERRED PIN1 BACKSIDE IDENTIFIER



DETAIL N
PREFERRED CORNER CONFIGURATION



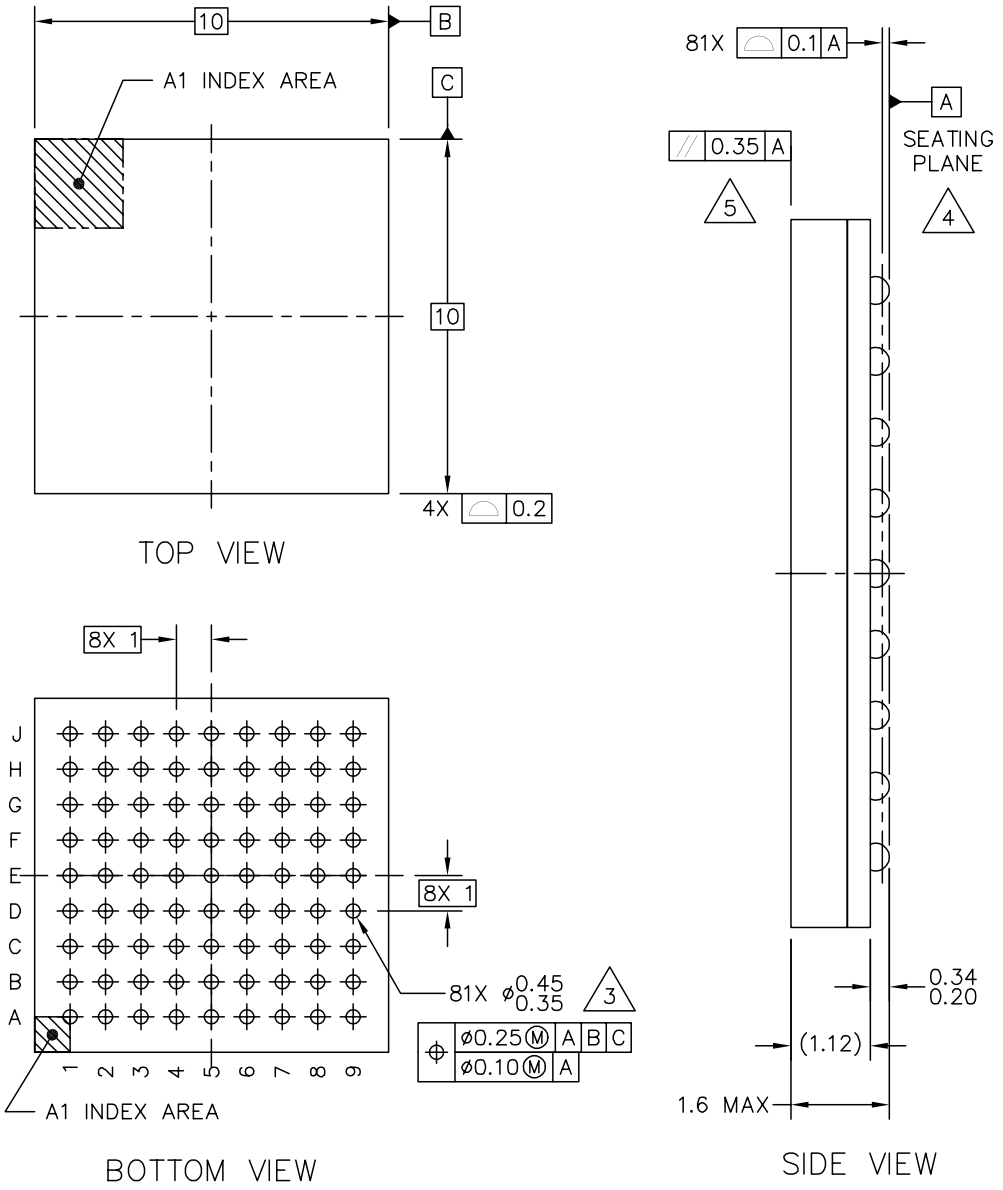
DETAIL G
VIEW ROTATED 90° CW

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740-01	
	STANDARD: JEDEC MO-220 VMMD-3	
	PACKAGE CODE: 6200	SHEET: 2 OF 4

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740–01	
	STANDARD: JEDEC MO–220 VMMD–3	
	PACKAGE CODE: 6200	SHEET: 3 OF 4



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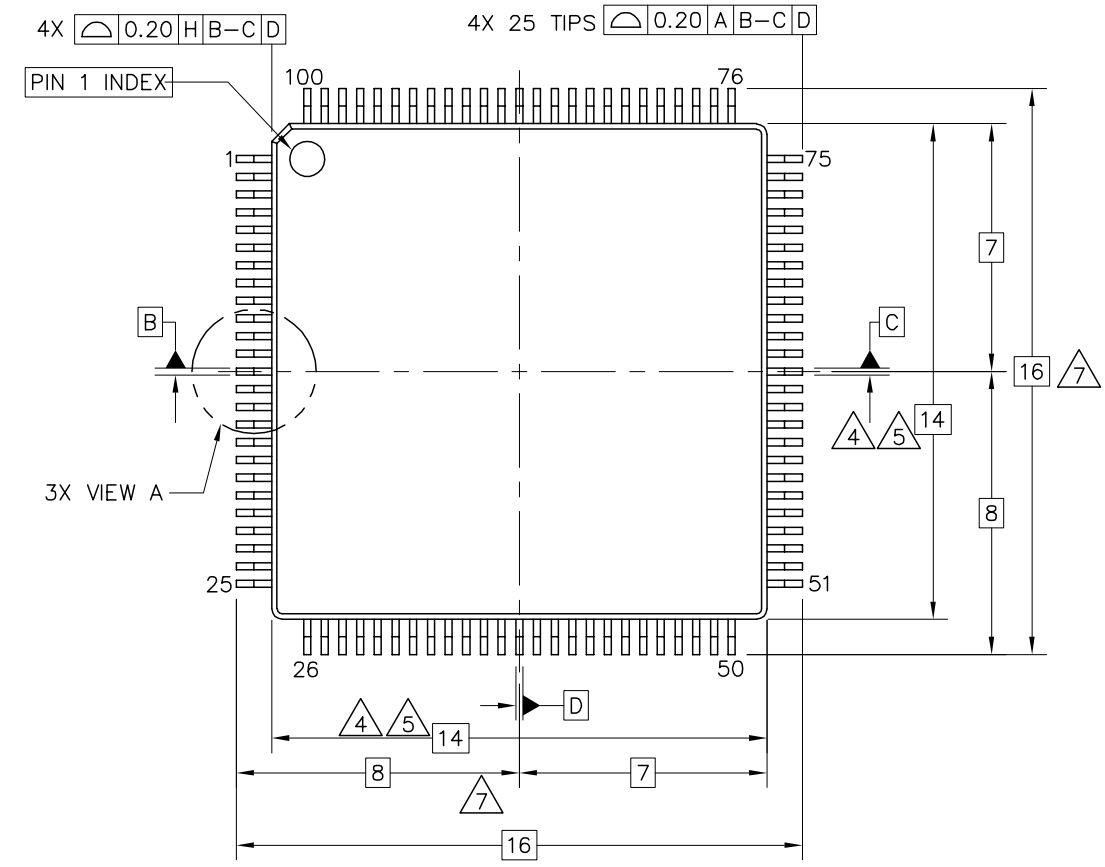
TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D	REV: O
	CASE NUMBER: 1662–01	04 FEB 2005
	STANDARD: NON–JEDEC	

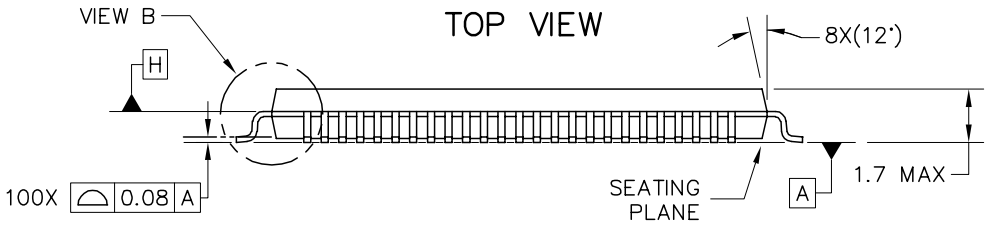
NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D	REV: O
	CASE NUMBER: 1662–01	04 FEB 2005
	STANDARD: NON–JEDEC	





SIDE VIEW

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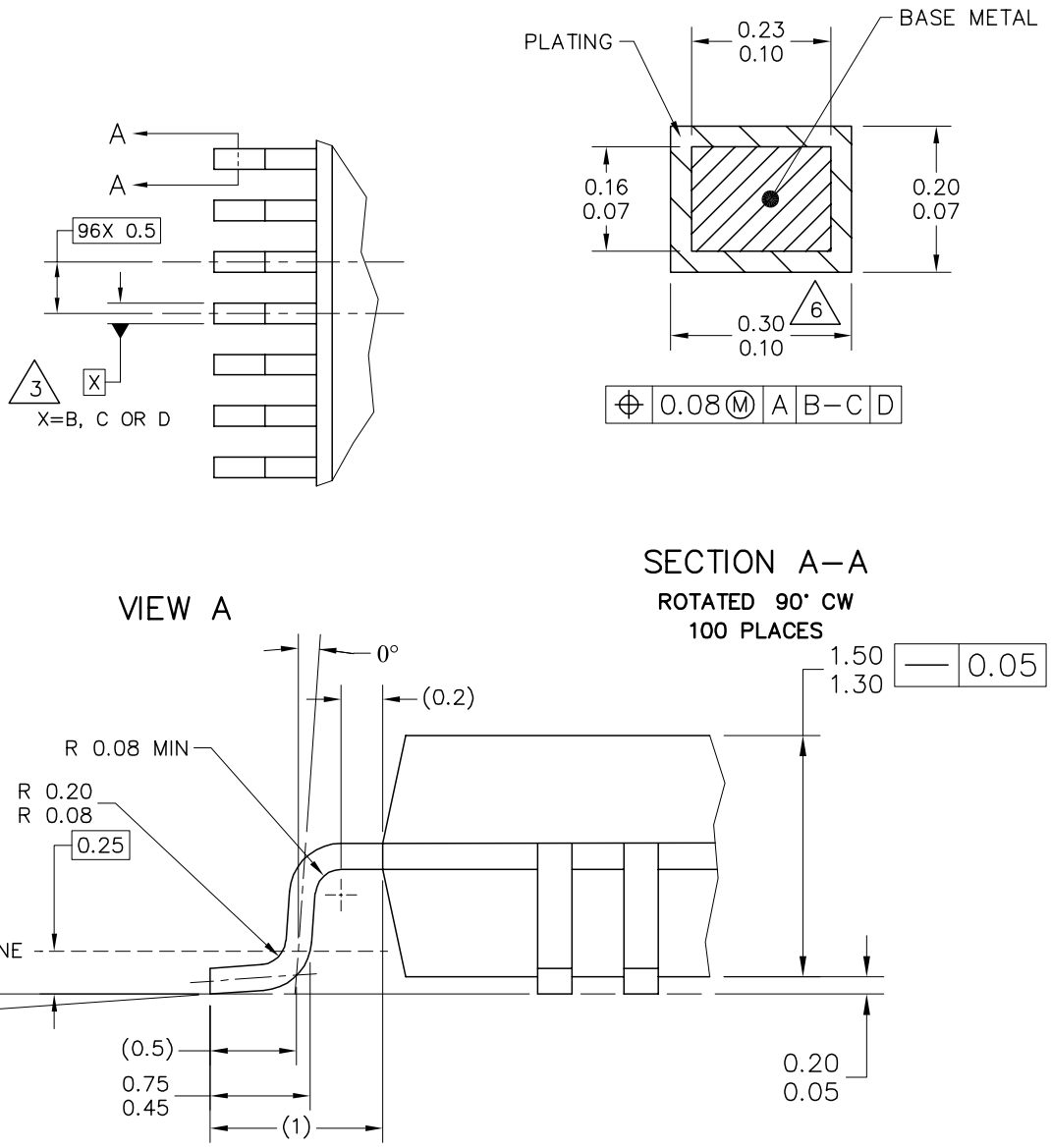
TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	



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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.

4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 mm.

5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

6. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.

7. DIMENSIONS D AND E ARE DETERMINED AT THE SEATING PLANE, DATUM A.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	

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