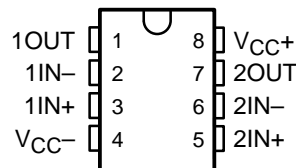


MC1458, MC1558 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

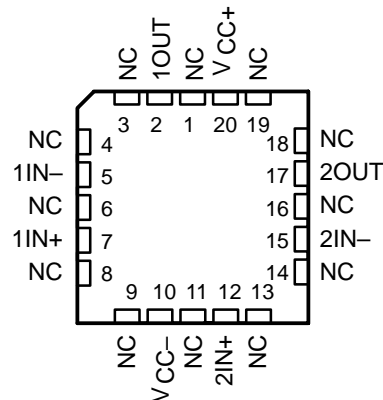
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- Short-Circuit Protection
- Wide Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- Low Power Consumption
- No Latch-Up
- Designed to Be Interchangeable With Motorola MC1558/MC1458 and Signetics S5558/N5558

MC1458 . . . D, P, OR PS PACKAGE
MC1558 . . . JG PACKAGE
(TOP VIEW)



MC1558 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The MC1458 and MC1558 are dual general-purpose operational amplifiers, with each half electrically similar to the μ A741, except that offset null capability is not provided.

The high-common-mode input voltage range and the absence of latch-up make these amplifiers ideal for voltage-follower applications. The devices are short-circuit protected and the internal frequency compensation ensures stability without external components.

ORDERING INFORMATION

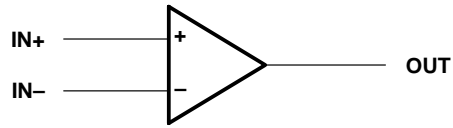
T_A	V_{IOmax} AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (P)	Tube	MC1458P	MC1458P
		SOIC (D)	Tube	MC1458D	MC1458
			Tape and reel	MC1458DR	
		SOP (PS)	Tape and reel	MC1458PSR	M1458
–55°C to 125°C	5 mV	CDIP (JG)	Tube	MC1558JG	MC1558JG
		CDIP (JGB)	Tube	MC1558JGB	MC1558JGB
		LCCC (FK)	Tube	MC1558FK	MC1558FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

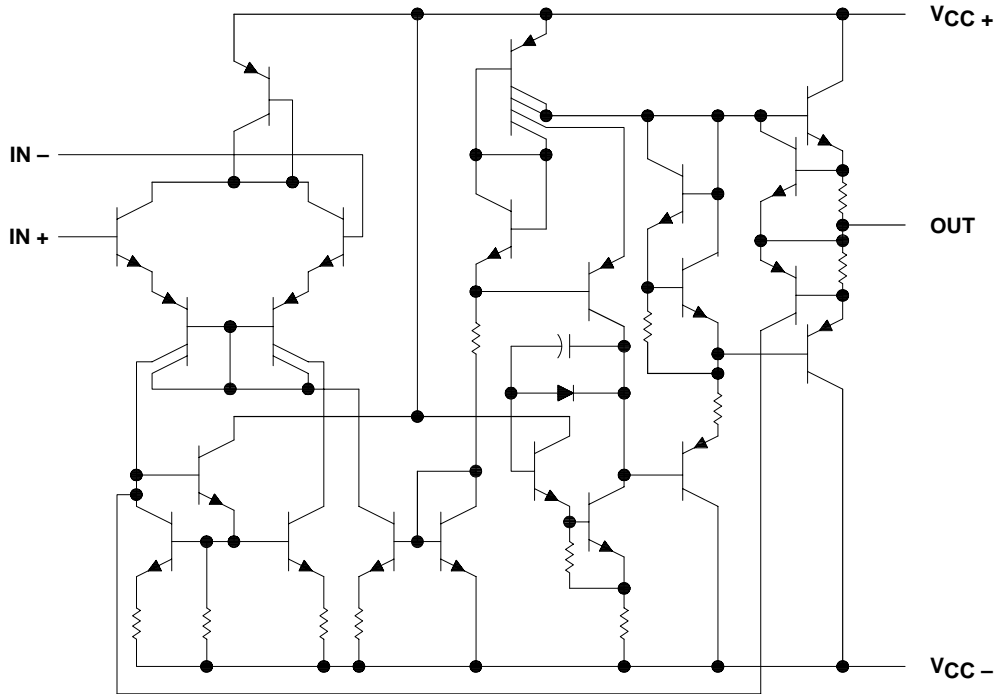
MC1458, MC1558 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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symbol (each amplifier)



schematic (each amplifier)



MC1458, MC1558 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC+} (see Note 1):	MC1458	18 V
	MC1558	22 V
Supply voltage, V_{CC-} (see Note 1):	MC1458	-18 V
	MC1558	-22 V
Differential input voltage, V_{ID} (see Note 2)	± 30 V
Input voltage, V_I (either input, see Notes 1 and 3)	± 15 V
Duration of output short circuit (see Note 4)	Unlimited
Operating virtual junction temperature, T_J	150°C
Package thermal impedance, θ_{JA} (see Notes 5 and 6):	D package	97°C/W
	P package	85°C/W
	PS package	95°C/W
Package thermal impedance, θ_{JC} (see Notes 7 and 8):	FK package	5.61°C/W
	JG package	14.5°C/W
Case temperature for 60 seconds: FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: JG package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, P, or PS package	260°C
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$.
 3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
 4. The output can be shorted to ground or either power supply. For the MC1558 only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 70°C free-air temperature.
 5. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 6. The package thermal impedance is calculated in accordance with JESD 51-7.
 7. Maximum power dissipation is a function of $T_J(max)$, θ_{JC} , and T_C . The maximum allowable power dissipation at any allowable case temperature is $P_D = (T_J(max) - T_C)/\theta_{JC}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 8. The package thermal impedance is calculated in accordance with MIL-STD-883.

recommended operating conditions

		MIN	MAX	UNIT
$V_{CC\pm}$	Supply voltage	± 5	± 15	V
T_A	Operating free-air temperature range	MC1458	0 70	°C
		MC1558	-55 125	



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electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15\text{ V}$

PARAMETER	TEST CONDITIONS†	MC1458			MC1558			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0$	25°C	1	6	1	5	mV	
		Full range		7.5		6		
I_{IO} Input offset current	$V_O = 0$	25°C	20	200	20	200	nA	
		Full range		300		500		
I_{IB} Input bias current	$V_O = 0$	25°C	80	500	80	500	nA	
		Full range		800		1500		
V_{ICR} Common-mode input voltage range		25°C	±12	±13	±12	±13	V	
		Full range	±12		±12			
V_{OM} Maximum peak output voltage swing	$R_L = 10\text{ k}\Omega$	25°C	±12	±14	±12	±14	V	
	$R_L \geq 10\text{ k}\Omega$	Full range	±12		±12			
	$R_L = 2\text{ k}\Omega$	25°C	±10	±13	±10	±13		
	$R_L \geq 2\text{ k}\Omega$	Full range	±10		±10			
A_{VD} Large-signal differential voltage amplification	$R_L \geq 2\text{ k}\Omega, V_O = \pm 10\text{ V}$	25°C	20	200	50	200	V/mV	
		Full range	15		25			
B_{OM} Maximum-output-swing bandwidth (closed loop)	$R_L = 2\text{ k}\Omega, A_{VD} = 1, THD \geq 5\%$	25°C	14		14		kHz	
B_1 Unity-gain bandwidth		25°C	1		1		MHz	
ϕ_m Phase margin	$A_{VD} = 1$	25°C	65		65		deg	
		Gain margin	11		11			
r_i Input resistance		25°C	0.3	2	0.3*	2	MΩ	
r_o Output resistance	$V_O = 0, \text{ See Note 9}$	25°C	75		75		Ω	
C_i Input capacitance		25°C	1.4		1.4		pF	
z_{ic} Common-mode input impedance	$f = 20\text{ Hz}$	25°C	200		200		MΩ	
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICR}\text{ min}, V_O = 0$	25°C	70	90	70	90	dB	
		Full range	70		70			
k_{SVS} Supply-voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9\text{ V to } \pm 15\text{ V}, V_O = 0$	25°C	30	150	30	150	μV/V	
		Full range		150		150		
V_n Equivalent input noise voltage (closed loop)	$A_{VD} = 100, f = 1\text{ kHz}, R_S = 0, BW = 1\text{ Hz}$	25°C	45		45		nV/√Hz	
I_{OS} Short-circuit output current		25°C	±25	±40	±25	±40	mA	
I_{CC} Supply current (both amplifiers)	$V_O = 0, \text{ No load}$	25°C	3.4	5.6	3.4	5	mA	
		Full range		6.6		6.6		
P_D Total power dissipation (both amplifiers)	$V_O = 0, \text{ No load}$	25°C	100	170	100	150	mW	
		Full range		200		200		
V_{O1}/V_{O2} Crosstalk attenuation		25°C	120		120		dB	

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All characteristics are specified under open-loop operating conditions with zero common-mode input voltage, unless otherwise specified. Full range for MC1458 is 0°C to 70°C and for MC1558 is -55°C to 125°C.

NOTE 9: This typical value applies only at frequencies above a few hundred hertz because of the effect of drift and thermal feedback.



MC1458, MC1558 DUAL GENERAL-PURPOSE OPERATIONAL AMPLIFIERS

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operating characteristics, $V_{CC\pm} = \pm 15\text{ V}$, $C_L = 100\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Figure 1)

PARAMETER		TEST CONDITIONS		MC1458			MC1558			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20\text{ mV}$,	$R_L = 2\text{ k}\Omega$,	0.3			0.3			μs
	Overshoot factor	$V_I = 20\text{ mV}$,	$R_L = 2\text{ k}\Omega$	5			5			%
SR	Slew rate at unity gain	$V_I = 10\text{ V}$,	$R_L = 2\text{ k}\Omega$	0.5			0.5			$\text{V}/\mu\text{s}$

PARAMETER MEASUREMENT INFORMATION

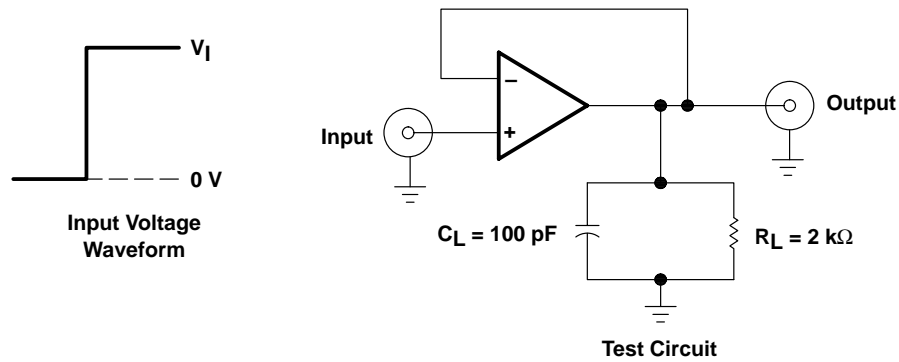


Figure 1. Rise-Time, Overshoot, and Slew-Rate Waveform and Test Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-9760301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-9760301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
MC1458D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC1458DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC1458DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC1458DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC1458P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC1458PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
MC1458PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC1458PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MC1558FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
MC1558JG	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
MC1558JGB	ACTIVE	CDIP	JG	8	1	TBD	A42 SNPB	N / A for Pkg Type
MC1558P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
SN98212P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

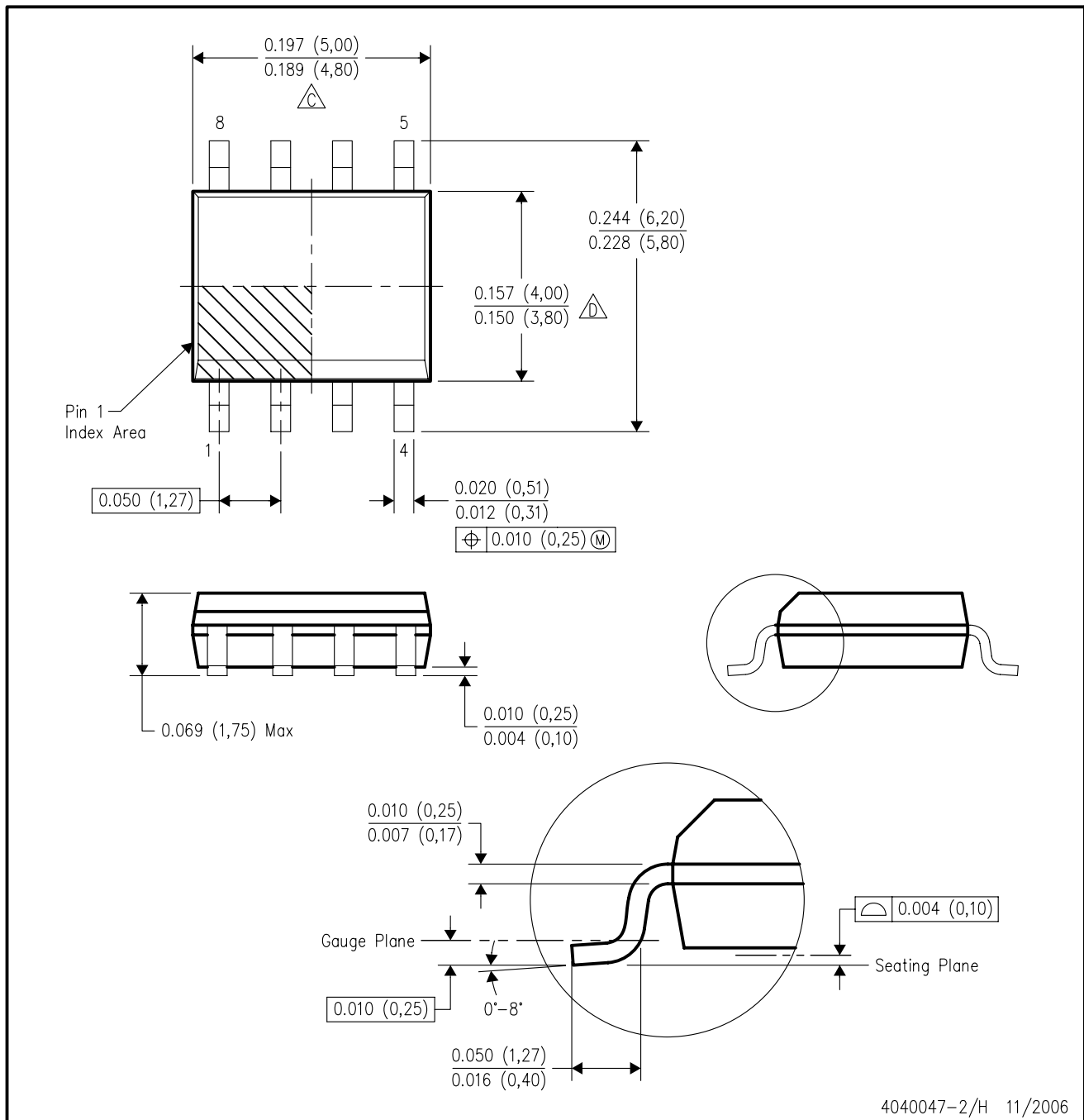


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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