

## FEATURES

- Low Quiescent Current: 8 $\mu$ A Operating, 6 $\mu$ A Shutdown
- Withstands Surge Voltage Up to the MOSFET Limit
- Wide Operating Voltage Range: 4V to 72V
- Overcurrent Protection
- Selectable Internal 31.5V/50V or Adjustable Gate Clamp Voltage (Table 1)
- Reverse Input Protection to -60V
- Adjustable Turn-On Threshold
- Adjustable Fault Timer with MOSFET Stress Acceleration
- Controls N-Channel MOSFET
- Latchoff and Retry Options (Table 1)
- Low Retry Duty Cycle During Faults (Table 1)
- 10-Pin DFN (3mm  $\times$  3mm) and MSOP Packages

## APPLICATIONS

- Automotive/Avionic/Industrial Surge Protection
- Hot Swap/ Live Insertion
- High Side Switch for Battery Powered Systems
- Intrinsic Safety Applications

## DESCRIPTION

The **LTC<sup>®</sup>4380** low quiescent current surge stopper protects loads from high voltage transients. Overvoltage protection is provided by clamping the gate voltage of an external N-channel MOSFET to limit the output voltage to a safe value during overvoltage events such as load dump in automobiles. Fixed gate clamp voltages are selectable for 12V and 24V/28V systems. For systems of any voltage up to 72V, use the adjustable gate clamp versions. Overcurrent protection is also provided.

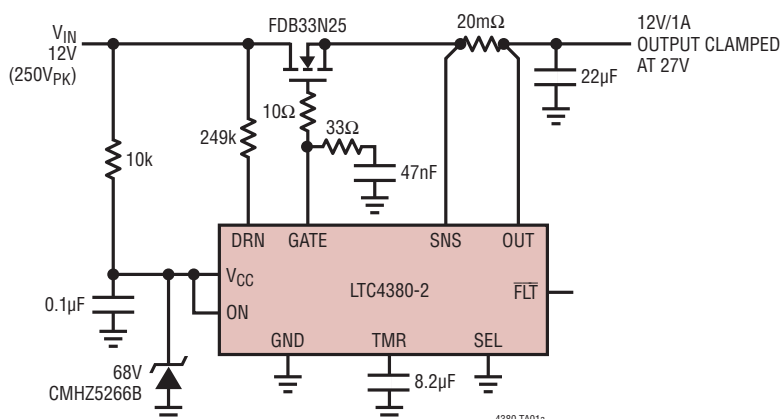
An internal multiplier generates a TMR pin current proportional to  $V_{DS}$  and  $I_D$ , so that operating time in both overcurrent and overvoltage conditions is limited in accordance with MOSFET stress.

The GATE pin can drive back-to-back MOSFETs for reverse input protection, eliminating the voltage drop and dissipation of a Schottky diode solution. A low 8 $\mu$ A operating current permits use in always-on and battery powered applications. An accurate ON pin comparator monitors the input supply for undervoltage (UV) conditions and also serves as a shutdown input, reducing the quiescent current to 6 $\mu$ A.

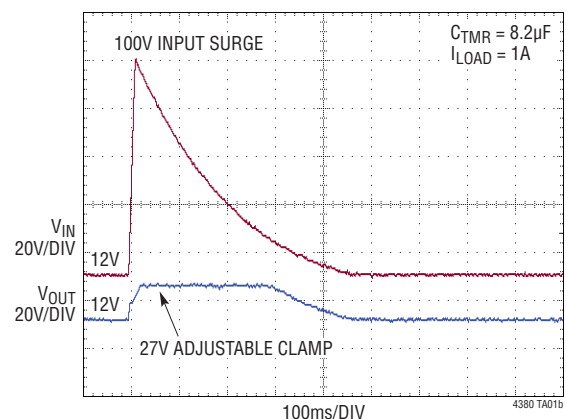
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## TYPICAL APPLICATION

12V, 1A with 250V Overvoltage Protection



Surge Stopper Limits Output to 27V During Input Surge

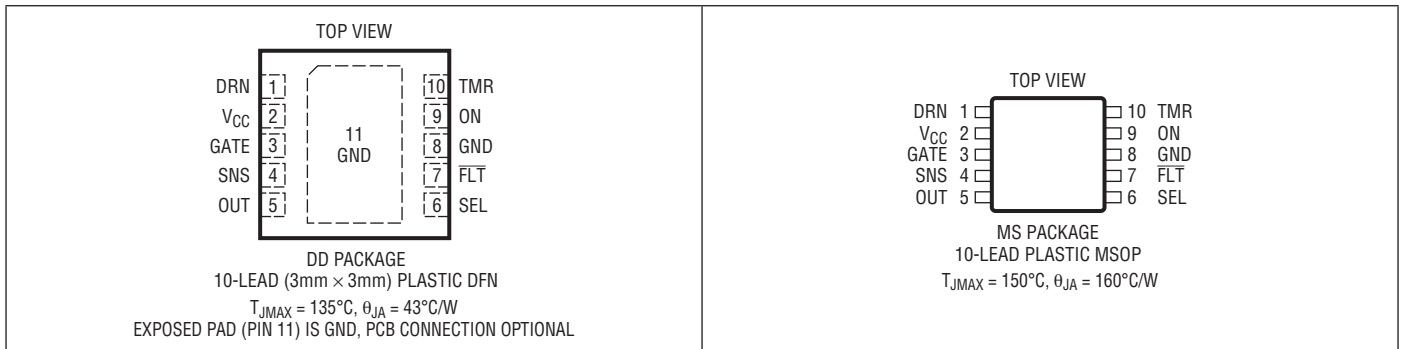


# LTC4380

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

$V_{CC}$ , ON, SEL.....	-60V to 80V	$\overline{FLT}$ .....	-0.3V to 80V
DRN (Note 3), SNS, OUT		$I_{DRN}$ .....	2.5mA
LTC4380-1/LTC4380-2.....	-0.3V to 53V	Operating Ambient Temperature Range	
LTC4380-3/LTC4380-4.....	-0.3V to 80V	LTC4380C.....	0°C to 70°C
SNS to OUT.....	-5V to 5V	LTC4380I.....	-40°C to 85°C
GATE (Note 4)		LTC4380H.....	-40°C to 125°C
LTC4380-1/LTC4380-2.....	-0.3V to 53V	Storage Temperature Range .....	-65°C to 150°C
LTC4380-3/LTC4380-4.....	-0.3V to 86V	Lead Temperature (Soldering, 10 sec)	
GATE to OUT, $V_{CC}$ (Note 4).....	-0.3V to 10V	MSOP .....	300°C
TMR.....	-0.3V to 5V		

## PIN CONFIGURATION



## ORDER INFORMATION <http://www.linear.com/product/LTC4380#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4380CDD-1#PBF	LTC4380CDD-1#TRPBF	LGHQ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-1#PBF	LTC4380IDD-1#TRPBF	LGHQ	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC4380HDD-1#PBF	LTC4380HDD-1#TRPBF	LGHQ	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC4380CMS-1#PBF	LTC4380CMS-1#TRPBF	LTGHR	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-1#PBF	LTC4380IMS-1#TRPBF	LTGHR	10-Lead Plastic MSOP	-40°C to 85°C
LTC4380HMS-1#PBF	LTC4380HMS-1#TRPBF	LTGHR	10-Lead Plastic MSOP	-40°C to 125°C
LTC4380CDD-2#PBF	LTC4380CDD-2#TRPBF	LGHS	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-2#PBF	LTC4380IDD-2#TRPBF	LGHS	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC4380HDD-2#PBF	LTC4380HDD-2#TRPBF	LGHS	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC4380CMS-2#PBF	LTC4380CMS-2#TRPBF	LTGHT	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-2#PBF	LTC4380IMS-2#TRPBF	LTGHT	10-Lead Plastic MSOP	-40°C to 85°C
LTC4380HMS-2#PBF	LTC4380HMS-2#TRPBF	LTGHT	10-Lead Plastic MSOP	-40°C to 125°C
LTC4380CDD-3#PBF	LTC4380CDD-3#TRPBF	LGXZ	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-3#PBF	LTC4380IDD-3#TRPBF	LGXZ	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC4380HDD-3#PBF	LTC4380HDD-3#TRPBF	LGXZ	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC4380CMS-3#PBF	LTC4380CMS-3#TRPBF	LTGYD	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-3#PBF	LTC4380IMS-3#TRPBF	LTGYD	10-Lead Plastic MSOP	-40°C to 85°C

4380f

## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4380HMS-3#PBF	LTC4380HMS-3#TRPBF	LTGYD	10-Lead Plastic MSOP	-40°C to 125°C
LTC4380CDD-4#PBF	LTC4380CDD-4#TRPBF	LGYC	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4380IDD-4#PBF	LTC4380IDD-4#TRPBF	LGYC	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC4380HDD-4#PBF	LTC4380HDD-4#TRPBF	LGYC	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 125°C
LTC4380CMS-4#PBF	LTC4380CMS-4#TRPBF	LTGYF	10-Lead Plastic MSOP	0°C to 70°C
LTC4380IMS-4#PBF	LTC4380IMS-4#TRPBF	LTGYF	10-Lead Plastic MSOP	-40°C to 85°C
LTC4380HMS-4#PBF	LTC4380HMS-4#TRPBF	LTGYF	10-Lead Plastic MSOP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 12\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$	Operating Voltage Range	LTC4380-1/LTC4380-2	●	4	80	V
		LTC4380-3/LTC4380-4 (Note 6)	●	4	72	V
$V_{OUT}$	Operating Voltage Range		●		72	V
$I_Q$	Total Supply Current, ON (Note 5)	$V_{CC} = OUT = SNS = DRN = 12\text{V}$ C-Grade and I-Grade	●	8	11	$\mu\text{A}$
		H-Grade	●		12	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Current, OFF	$V_{CC} = OUT = SNS = DRN = 4\text{V}$	●	22	28	$\mu\text{A}$
			●		35	$\mu\text{A}$
$I_{CC}$	$V_{CC}$ Current, ON	$ON = OUT = SNS = 0\text{V}$	●	6	10	$\mu\text{A}$
		$V_{CC} = OUT = SNS = DRN = 12\text{V}$	●	7	9	$\mu\text{A}$
		$V_{CC} = OUT = SNS = DRN = 4\text{V}$	●	20	25	$\mu\text{A}$
			●		30	$\mu\text{A}$
$I_{SNS}$	SNS Current, ON	$V_{CC} = OUT = SNS = DRN$	●	0.5	1.4	$\mu\text{A}$
$I_{OUT}$	OUT Current, ON OUT Current, OFF	$SNS = OUT = DRN = 12\text{V}$	●	1.5	2	$\mu\text{A}$
		$SNS = OUT = DRN = 12\text{V}$ , C-Grade and I-Grade	●	5	12	$\mu\text{A}$
		H-Grade	●		80	$\mu\text{A}$
$I_R$	Reverse Input Current	$V_{CC} = -60\text{V}$ , ON Open, SEL = 0	●	-0.4	-2	mA
		$V_{CC} = ON = SEL = -60\text{V}$	●	-1.2	-5	mA
$\Delta V_{GATE}$	GATE Drive (GATE – OUT)	SEL = SNS = OUT = $V_{CC}$ $8\text{V} \leq V_{CC} \leq 30\text{V}$ ; $I_{GATE} = -1\mu\text{A}$ , $0\mu\text{A}$	●	10	11.5	V
		$V_{CC} = 4\text{V}$ ; $I_{GATE} = -1\mu\text{A}$ , $0\mu\text{A}$	●	5	8	V
$\Delta V_{CLAMP}$	GATE Clamp to $V_{CC}$ (GATE – $V_{CC}$ )	$SNS = OUT = 20\text{V}$ , $I_{GATE} = 0\mu\text{A}$	●	12	13.5	V
$V_{GATE}$	GATE Clamp to GND	$V_{CC} = 30\text{V}$ , SEL = 0V	●	30	31.5	V
		$V_{CC} = 60\text{V}$ , SEL = $V_{CC}$	●	47.5	50	52.5
$I_{GATE(UP)}$	GATE Pull-Up Current	$V_{CC} = GATE = OUT = 12\text{V}$ , SEL = 0V	●	-10	-20	$\mu\text{A}$
		$V_{CC} = GATE = OUT = 24\text{V}$ , SEL = $V_{CC}$	●	-12	-25	-35
$I_{GATE(DN)}$	GATE Pull-Down Current Overcurrent Shutdown Input UV Fault Time Out	$\Delta V_{SNS} = 200\text{mV}$ , GATE = 12V, OUT = 0V	●	50	100	mA
		ON = 0V, GATE = 20V	●	0.3	5	mA
		$V_{CC} = 2\text{V}$ , GATE = 10V	●	2	5	mA
		TMR = 2V, GATE = 10V	●	1.5	3.5	mA
			●			

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 12\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\Delta V_{SNS}$	Current Limit Sense Voltage (SNS – OUT)	$V_{CC} = 12\text{V}, 24\text{V}, \text{OUT} = 6\text{V}, 12\text{V}$	● 44	50	55	mV
		$V_{CC} = 12\text{V}, 24\text{V}, \text{OUT} = 0\text{V}$	● 42	62	95	mV
$I_{SEL}$	SEL Input Current	SEL = 0V to 80V	●		±0.1	μA
$V_{SEL}$	SEL Input Threshold		● 0.4		3	V
$I_{ON}$	ON Input Current	$V_{ON} = 1\text{V}$	● -1	-2		μA
$V_{ON}$	ON Input Threshold	ON Rising	● 0.99	1.05	1.1	V
$V_{ON(HYST)}$	ON Input Hysteresis			45		mV
$I_{FLT}$	FLT Leakage Current	FLT = 80V	●		2	μA
$V_{FLT(LOW)}$	FLT Output Low	$I_{SINK} = 0.1\text{mA}$	●	0.1	0.5	V
		$I_{SINK} = 3\text{mA}$	●	1	4	V
$\Delta V_{DRN}$	DRN Voltage (DRN – OUT)	$I_{DRN} = 0.1\text{mA}, \text{OUT} = \text{SNS} = 12\text{V}$	● 0.7	1.5	2.5	V
$V_{DS(MAX)}$	Overvoltage $V_{DS}$ Threshold (DRN – OUT)	TMR = 0.8V, $I_{DRN} = 2\mu\text{A}$	● 0.6	0.7	0.8	V
		SNS = OUT = 12V	● 0.3		1.0	V
$I_{TMR(DN)}$	TMR Pull-Down Current	TMR = 0.8V	● 1.25	2	2.75	μA
$I_{TMR(UP,COOL)}$	TMR Pull-Up Current, Cool Down	TMR = 2V	● -1	-2	-3	μA
$I_{TMR(UP)}$	TMR Pull-Up Current, Overvoltage	TMR = 0.8V, OUT = 11V, $V_{DS} = 1.1\text{V}, \Delta V_{SNS} = 0\text{mV}$	● -0.8	-1.6	-2.4	μA
	Small OV, Light Load	OUT = 28V, TMR = 0.8V	● -3.5	-6.7	-11.6	μA
	High OV, Light Load	$I_{DRN} = 0.1\text{mA}, \Delta V_{SNS} = 10\text{mV}$	● -13	-30	-61	μA
	Small OV, Heavy Load	$I_{DRN} = 1\text{mA}, \Delta V_{SNS} = 10\text{mV}$	● -10	-20	-30	μA
	High OV, Heavy Load	$I_{DRN} = 1\text{mA}, \Delta V_{SNS} = 40\text{mV}$	● -60	-120	-180	μA
	TMR Pull-Up Current, Overcurrent	TMR = 0.8V	● -4	-6	-9	μA
		$I_{DRN} = 0\text{mA}, \text{OUT} = 11\text{V}$	● -17	-27	-34	μA
	$I_{DRN} = 0\text{mA}, \text{OUT} = 0\text{V}$	●				
$V_{TMR(F)}$	TMR Gate Off Threshold	TMR Rising	● 1.178	1.215	1.251	V
		Small OV, Light Load	● -16	-27	-38	μA
		High OV, Light Load	● -80	-142	-200	μA
$D$	Retry Duty Cycle; Overvoltage, LTC4380-2/LTC4380-4	$\Delta V_{SNS} = 40\text{mV}, I_{DRN} = 5\mu\text{A}, \text{OUT} = 28\text{V}, V_{CC} = 29\text{V}$	●	2.8	3.5	%
		$\Delta V_{SNS} = 40\text{mV}, I_{DRN} = 500\mu\text{A}, \text{OUT} = 28\text{V}, V_{CC} = 80\text{V}$	●	0.1	0.2	%
		Retry Duty Cycle; Overcurrent, LTC4380-2/LTC4380-4	●			
		$I_{DRN} = 500\mu\text{A}$	●	0.1	0.2	%
		OUT = 0V	●	0.35	0.7	%
		OUT = 6V	●			
$t_{ON(ON)}$	Turn-On Propagation Delay	ON Steps from 0V to 1.5V, OUT = SNS = 0V	●	5	25	ms
$t_{OFF(ON)}$	Turn-Off Propagation Delay	ON Steps from 1.5V to 0V, OUT = SNS = $V_{CC}$	●	1	5	μs
$t_{OFF(OC)}$	Overcurrent Turn-Off Propagation Delay	$\Delta V_{SNS}$ Steps from 0V to 200mV, OUT = 6V	●	2	4	μs
		$\Delta V_{SNS}$ Steps from 0V to 200mV, OUT = 0V	●	2	4	μs

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

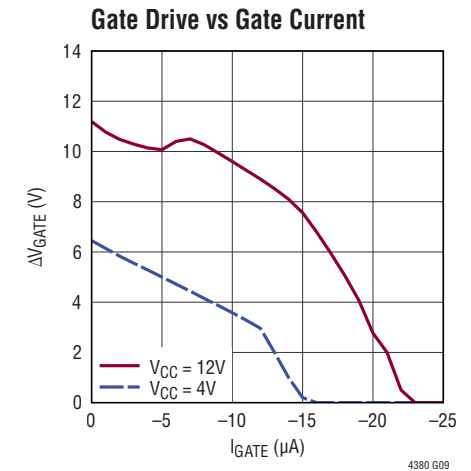
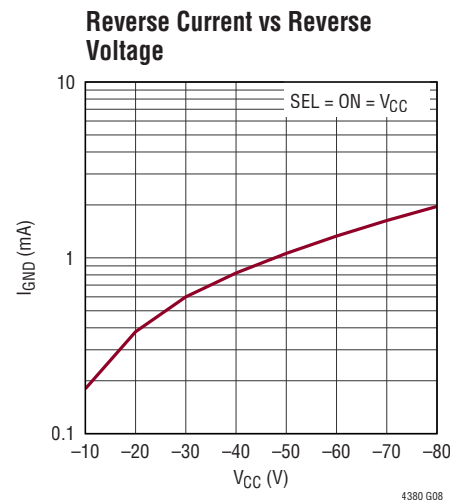
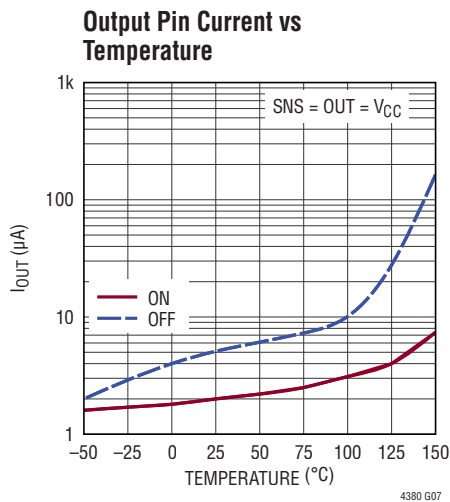
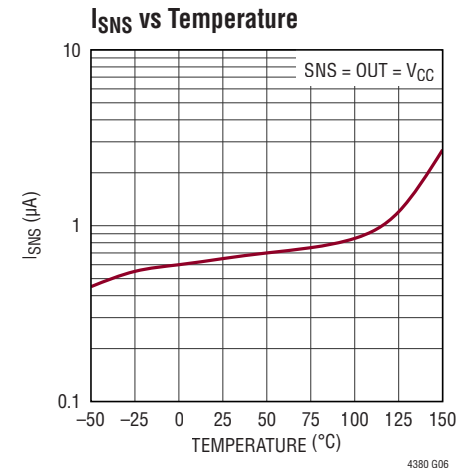
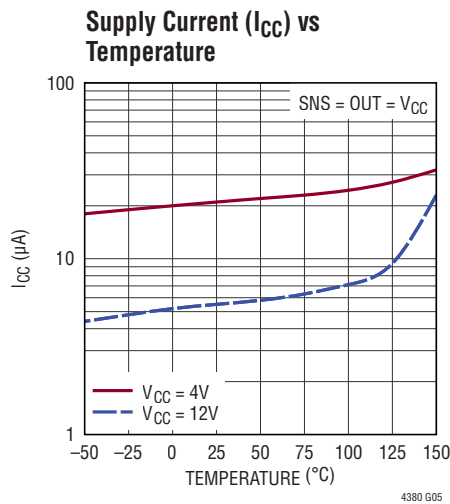
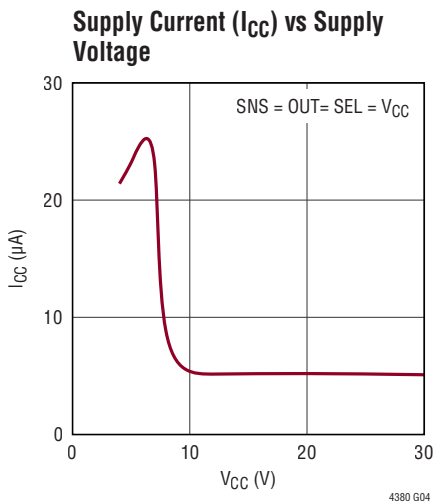
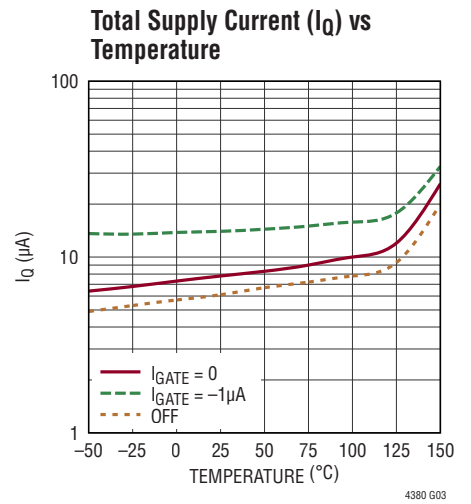
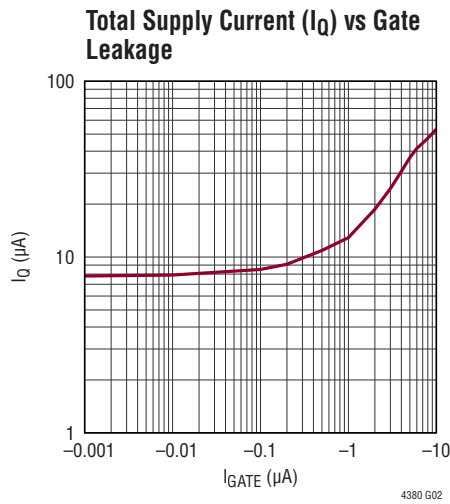
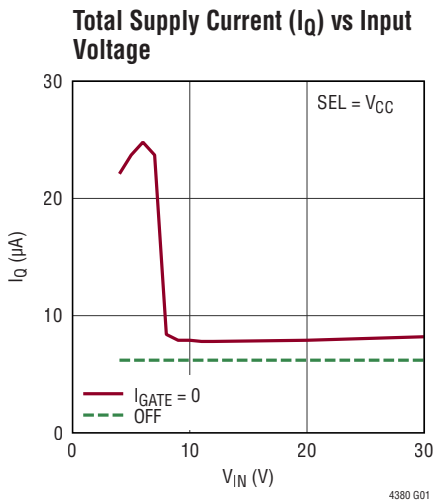
**Note 3:** Internal clamps limit the DRN pin to a minimum of 10V above the OUT and SNS pins.

**Note 4:** Internal clamps limit the GATE pin to a minimum of 10V above the OUT pin or  $V_{CC}$  pin, or 50V (SEL =  $V_{CC}$ ) or 31.5V (SEL = GND) above the GND pin (LTC4380-1/LTC4380-2). Driving this pin to voltages beyond the clamp may damage the device.

**Note 5:** Total supply current is the sum of the current into the  $V_{CC}$ , OUT, SNS and DRN pins.

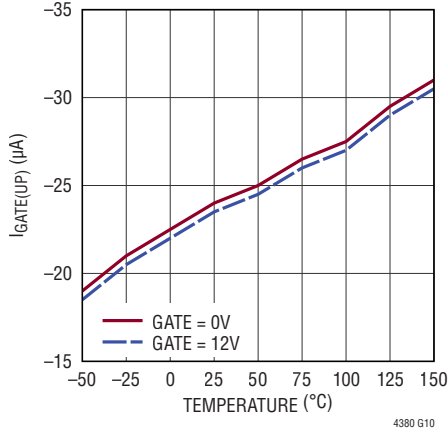
**Note 6:** Operating voltage is limited by the maximum GATE voltage of 86V.

**TYPICAL PERFORMANCE CHARACTERISTICS**  $V_{CC} = 12V$ , unless otherwise noted.



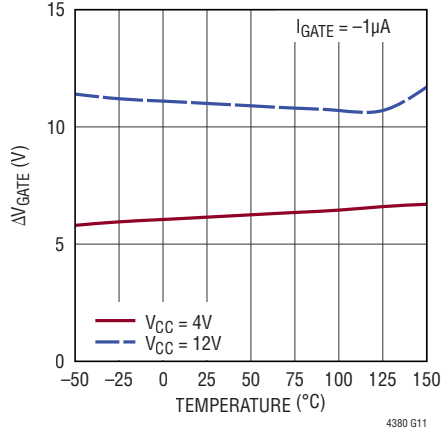
## TYPICAL PERFORMANCE CHARACTERISTICS $V_{CC} = 12V$ , unless otherwise noted.

**Gate Pull Up Current vs Temperature**



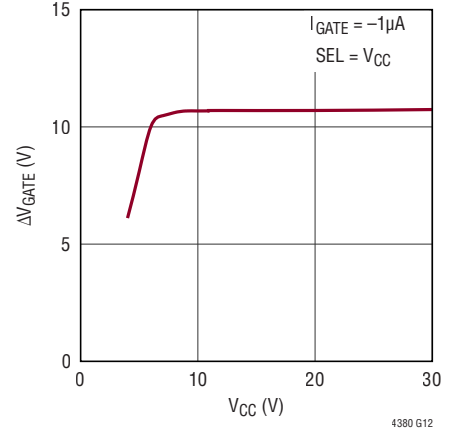
4380 G10

**Gate Drive vs Temperature**



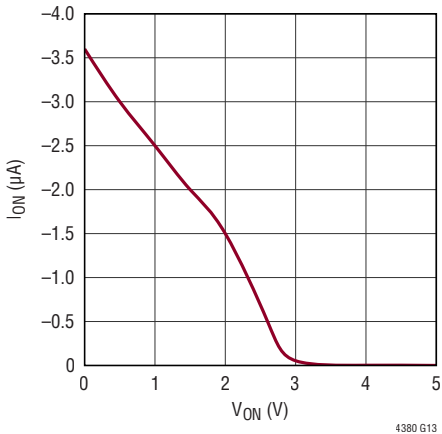
4380 G11

**Gate Drive vs Supply Voltage**



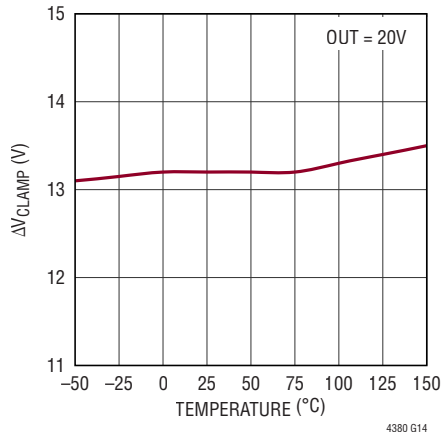
4380 G12

**ON Pin Current vs Voltage**



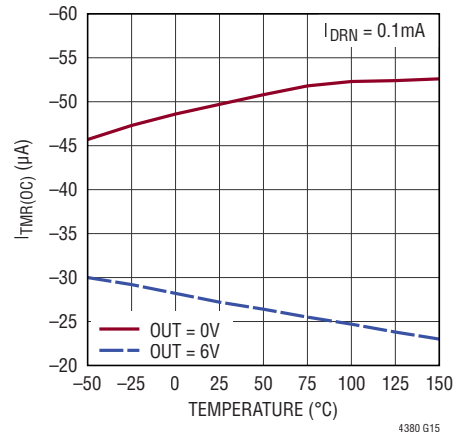
4380 G13

**Gate Clamp to  $V_{CC}$  vs Temperature**



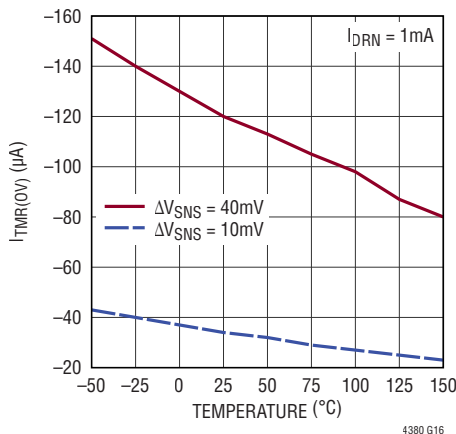
4380 G14

**TMR Pin Current vs Temperature**



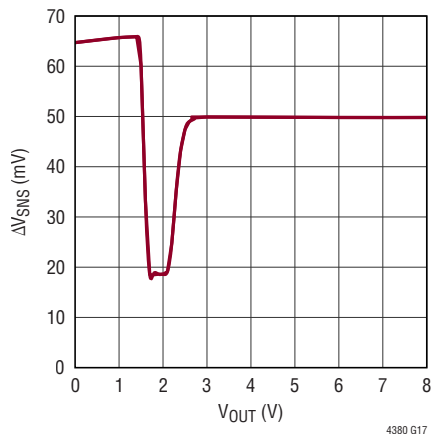
4380 G15

**TMR Pin Current vs Temperature**



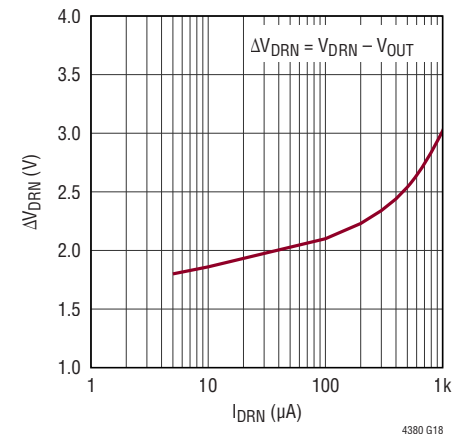
4380 G16

**Current Limit vs Output Voltage**



4380 G17

**DRN Voltage vs Current**



4380 G18

## PIN FUNCTIONS

**DRN:** External MOSFET Drain-Source Sense. The DRN pin voltage tracks the OUT pin. The resulting DRN pin current through external resistor  $R_{DRN}$  is proportional to the external MOSFET  $V_{DS}$ . The DRN pin current and  $\Delta V_{SNS}$  ( $SNS - OUT$ ) are multiplied internally to produce a TMR pin current approximately proportional to the MOSFET's power dissipation. This reduces the SOA requirement of the MOSFET by timing out faster during more severe faults. Choose  $R_{DRN}$  to limit the current to 1mA at the peak input voltage. Connect to OUT if unused.

**Exposed Pad:** Exposed Pad. May be left open or connected to device ground (GND).

**$\overline{FLT}$ :** Fault Output. This open drain logic output pin pulls low after the voltage at the TMR pin has reached the fault threshold of 1.215V. It indicates that the MOSFET is off because either the supply voltage has stayed at an elevated level for an extended period of time (voltage fault) or the device is in an overcurrent condition (current fault). The fault output is capable of sinking up to 3mA. Leave open if unused.

**GATE:** Gate Drive for N-Channel MOSFET. The GATE pin is pulled up by an internal 20 $\mu$ A charge pump that is regulated to 11.5V above the OUT pin. An amplifier controls the GATE pin to limit the current through the MOSFET. The GATE pin is clamped during an overvoltage event, thus indirectly limiting the output voltage. The clamp voltage is set to 31.5V with  $SEL = 0V$  or 50V when  $SEL = V_{CC}$  for the fixed voltage versions, LTC4380-1/LTC4380-2. The LTC4380-3 and LTC4380-4 are adjustable versions without the internal gate clamp. The voltage at the GATE pin is limited to 13.5V above  $V_{CC}$  when not in regulation mode. A minimum of 47nF of capacitance and 33 $\Omega$  series resistor at the pin is necessary to compensate the current limit amplifier. To avoid damaging the external MOSFET during an output short, GATE is also clamped internally to 17V above OUT.

**GND:** Device Ground.

**ON:** Turn-On Control Input. The LTC4380 can be turned on by pulling this pin above 1.05V or by leaving it open to allow an internal 1M resistor to turn the part on. Pulling the pin below the threshold turns off the part and reduces the supply current to 6 $\mu$ A. Limit the leakage current to ground

at the pin to no more than 1 $\mu$ A if no external pull-up is used. The ON pin can be pulled up to 80V or below GND by 60V without damage.

**OUT:** Output Voltage Sense. This pin senses the output voltage at the output terminal of the current sense resistor. An internal clamp limits the voltage in between the GATE and OUT pins to 17V. Bypass the OUT pin with a minimum of 22 $\mu$ F as close to the pin as possible.

**SEL:** Gate Clamp Voltage Select for LTC4380-1 and LTC4380-2. Connect the SEL pin to GND to set the internal gate clamp voltage to 31.5V. Connect it to  $V_{CC}$  or OUT for a 50V gate clamp voltage. The SEL pin can be pulled up to 80V or below GND by 60V without damage. Connect SEL to GND for LTC4380-3 and LTC4380-4.

**SNS:** Current Sense Input. Connect to the input terminal of the current sense resistor. The current limit amplifier controls the GATE pin to limit the current sense voltage to 50mV. This voltage increases to 62mV in a severe fault when OUT is below 1.5V. A fixed 7 $\mu$ A is added to the TMR pin current during an overcurrent condition to shorten the timer. In a severe short condition when output voltage is below 1.5V, the extra current increases to 27 $\mu$ A to reduce the power dissipation in the MOSFET.  $\Delta V_{SNS}$  ( $SNS - OUT$ ) must be limited to less than 5V. Connect to OUT if unused.

**TMR:** Fault Timer Input. Connect a capacitor between this pin and ground to set the fault turn-off time and cool down period. The charging current during fault conditions varies depending on the power dissipation of the MOSFET. When TMR reaches 1.215V, the MOSFET turns off and  $\overline{FLT}$  pulls low. Upon gate off, the part immediately enters a cool down period with a 2 $\mu$ A current pull up and pull down on the TMR pin. After the cool down period has concluded the LTC4380-2 and LTC4380-4 immediately restart, while the LTC4380-1 and LTC4380-3 remain off until the ON pin is pulled low momentarily for more than 100 $\mu$ s or power is cycled.

**$V_{CC}$ :** Positive Supply Voltage Input. The positive supply input ranges from 4V to 80V for normal operation. It can go below ground by up to 60V during a reverse battery condition, without damaging the part. For applications where the input voltage is expected to exceed 80V, the

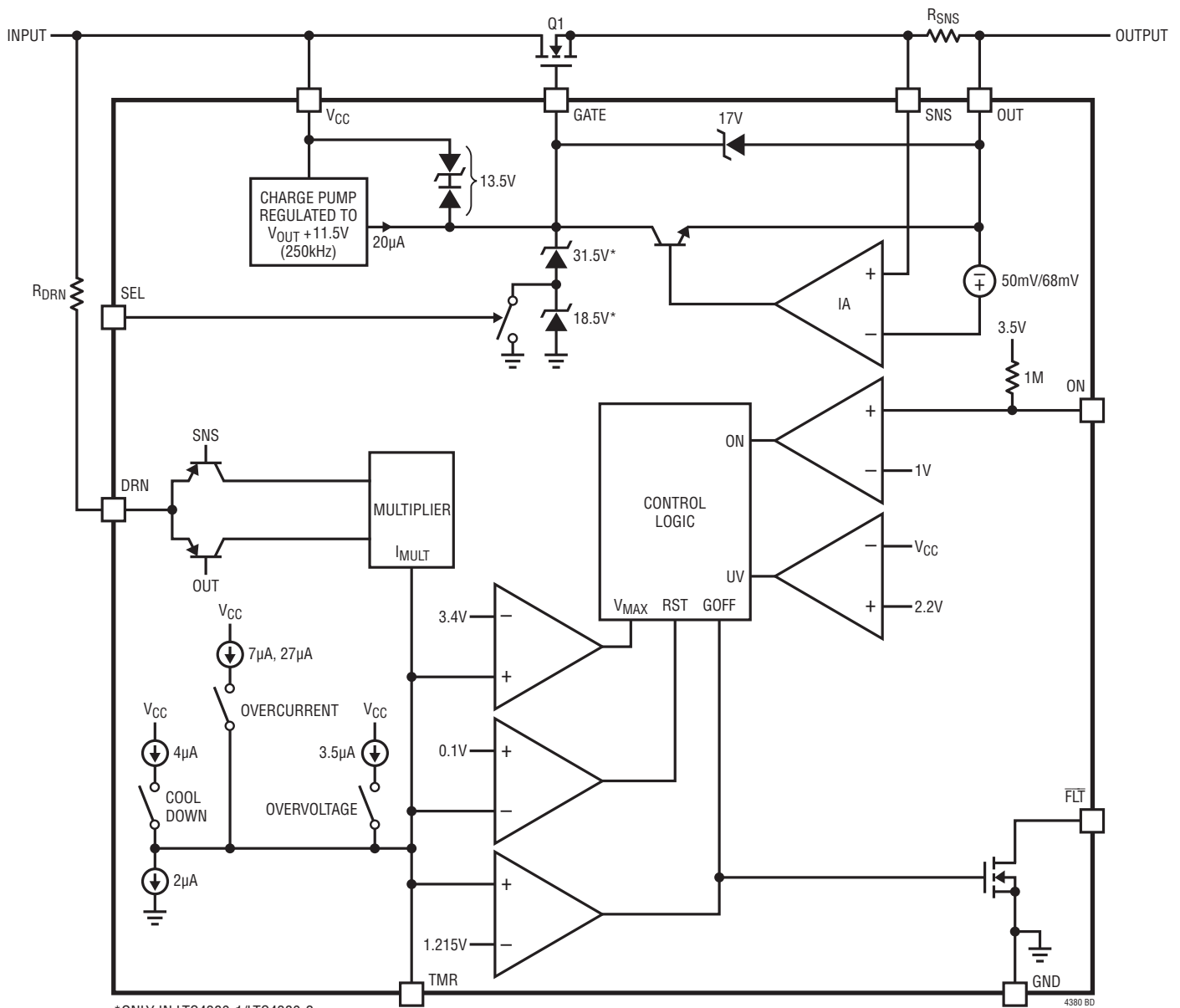


## PIN FUNCTIONS

$V_{CC}$  pin may be protected by a Zener diode clamp or, in the case of short duration spikes, by a simple RC filter. Clamping the  $V_{CC}$  pin with a Zener diode can also be used as a means of adjusting the GATE pin clamp voltage to a value less than the internal 31.5V or 50V clamps for

the LTC4380-1/LTC4380-2. For the adjustable versions, LTC4380-3/LTC4380-4, which have no internal gate clamp, a Zener diode at the  $V_{CC}$  pin is the only way to limit the voltage at the GATE pin.

## BLOCK DIAGRAM





## OPERATION

The LTC4380 is a low quiescent current surge stopper that drives an external N-channel MOSFET as the pass device. In normal operation, a 20 $\mu$ A charge pump (see Block Diagram) drives the MOSFET (Q1) high, turning it fully on and providing a low impedance path from input to the load. The MOSFET gate is clamped to ground by a Zener stack. If the input voltage rises to the point where the output approaches the gate clamp, the output is effectively limited to one threshold voltage below the gate clamp and the input surge is blocked from reaching the load.

For the LTC4380-1 and LTC4380-2 versions, two internal gate clamping voltages to ground are available: 31.5V, which limits the output to about 27V for use in 12V systems, and 50V, which limits the output to about 45V for use in 24V and 28V systems. The clamping voltage is selectable using the SEL pin. Besides the gate to ground clamp, the GATE pin is also limited to 13.5V above the  $V_{CC}$  pin voltage.

There is no internal gate clamp to ground for the LTC4380-3 and LTC4380-4 versions and the gate pin is only limited to 13.5V above the voltage at the  $V_{CC}$  pin. A Zener diode clamp connected from the  $V_{CC}$  pin to ground thus clamps the voltages at both the  $V_{CC}$  and GATE pins during over-voltage events.

Load current is limited by a current limit amplifier (IA), using a sense resistor in series with the MOSFET source to monitor the current. The current limit threshold is 50mV rising to 62mV when the output is less than 3V.

MOSFET stress is monitored by a timer, whose current is a function of Q1's  $V_{DS}$  as well as  $I_D$ .  $V_{DS}$  is monitored by  $R_{DRN}$  at the DRN pin, while  $I_D$  is monitored by sensing the voltage drop across  $R_{SNS}$ . The timer allows the load to continue functioning during short transient events while protecting the MOSFET from being damaged by a sustained overvoltage, such as load dump in vehicles, or an output overload or short circuit.

A multiplier sets the timer period depending on the power dissipation in the MOSFET. Higher power dissipation corresponds to a shorter timer period, helping to keep the MOSFET within its safe operating area (SOA).

The timer responds to stresses at start-up, during voltage limiting, and during current limiting. TMR pin current is integrated on timing capacitor  $C_{TMR}$  and if TMR charges to 1.215V, the MOSFET is turned off. At this point the LTC4380-1 and LTC4380-3 latch off, and can be reset by cycling power or by pulling the ON pin low for at least 100 $\mu$ s. For the LTC4380-2 and LTC4380-4, the TMR pin enters a cool down phase, allowing time for the MOSFET temperature to equalize with its surroundings before automatically restarting. The TMR pin slowly charges up and down in between 3.4V and 1.215V for 15 times and discharges to ground at the last cycle. When the TMR pin has reached the 100mV threshold, the MOSFET is turned back on. The cool down interval can be curtailed by pulling the ON pin low for at least 10ms/ $\mu$ F of  $C_{TMR}$ .

In addition to resetting the timer, the ON pin is used for on/off control and for undervoltage detection. The ON pin threshold is 1.05V.

The open drain  $\overline{FLT}$  pin pulls low whenever the timer is faulted off, and goes high again when reset by a power cycle, by pulling the ON pin low for at least 100 $\mu$ s or in the case of the LTC4380-2 and LTC4380-4, when the TMR pin discharges to 100mV.

**Table 1. LTC4380 Options**

LTC4380	GATE CLAMP	FAULT BEHAVIOR
-1	Internal 31.5V/50V to GND	Latchoff
-2	Internal 31.5V/50V to GND	Auto Retry
-3	Externally Adjustable	Latchoff
-4	Externally Adjustable	Auto Retry

## APPLICATIONS INFORMATION

The LTC4380 limits the voltage and current delivered to the load during supply transient or output overload events. The N-channel MOSFET provides a low resistance path from the input to the load during normal operation, while in overvoltage conditions it limits the output to a threshold voltage below the clamped gate voltage. The total fault timer period is set to ride through short-duration faults, while longer events cause the output to shut off and protect the MOSFET from damage.

### Startup

Figure 1 shows a 12V, 1A application which limits the output to approximately 27V. When power is first applied with  $V_{CC} \geq 4V$  and  $ON \geq 1.05V$ , there is a delay of about 10ms before the GATE pin begins charging C2 and Q1's gate terminal with a fixed, 20 $\mu$ A current source. Q1, operating as a source follower, ramps the output up at a rate of  $I_{GATE(UP)}/C2$ . Inrush current in the load capacitance  $C_L$  is given by

$$I_{INRUSH} = I_{GATE(UP)} \cdot \frac{C_L}{C2}$$

where  $I_{GATE(UP)}$  is typically 20 $\mu$ A.

Eventually the GATE pin charges to the point where  $V_{IN} \approx V_{OUT}$  and stops only when  $\Delta V_{GATE}$  ( $V_{GATE} - V_{OUT}$ ) reaches its regulation point of 11.5V, fully enhancing Q1.

### Overcurrent Fault Protection

The LTC4380 features an adjustable current limit that protects against short circuits and excessive load current. During an overcurrent event, the GATE pin is regulated to limit the current sense voltage across the SNS and OUT pins ( $\Delta V_{SNS}$ ) to 50mV when out is above 3V. In the case of a severe short at the output, where OUT is less than 1.5V, the current sense voltage is 62mV. Output current is thereby limited to  $\Delta V_{SNS}/R_{SNS}$ . Current limit may control the startup ramp rate in extreme cases, such as if  $C_L$  is unusually large or if current limit is set to an unusually low value, and artificially reduces  $C_L$ 's inrush current below the value previously calculated.

### Overvoltage Fault Protection

The LTC4380 limits the voltage at the output during an overvoltage at the input. For the LTC4380-1/LTC4380-2 illustrated in Figure 1, an internal clamp limits the GATE pin to either 31.5V or 50V, depending on the state of the SEL pin. With the SEL pin grounded as shown, the GATE pin is clamped at 31.5V. Assuming a threshold voltage of 5V for Q1, this limits the output to approximately 26.5V. Tying the SEL pin high causes the GATE pin to clamp at 50V, and limits the output to approximately 45V.

The GATE pin may also be limited by the compliance of the internal 20 $\mu$ A current source, to  $V_{CC} + 13.5V$ . In the LTC4380-3/LTC4380-4 the GATE pin clamp is entirely disconnected, leaving only the  $V_{CC} + 13.5V$  compliance limit. This arrangement allows the GATE pin to be effectively clamped at any voltage from 18V to 86V, by clamping  $V_{CC}$  to between 4V and 72V.

### V<sub>CC</sub> Pin

The  $V_{CC}$  pin operating range extends from 4V to 80V. In the presence of an input overvoltage exceeding 80V, the  $V_{CC}$  pin must be protected by filtering or clamping. For short duration spikes and transients exceeding 80V, filtering is the most sensible means of protecting the  $V_{CC}$  pin. R1 and C1 provide filtering in Figure 1. Owing to the LTC4380's low  $I_{CC}$ , values up to 20k may be used for R1 without seriously impairing the lower end of the operating voltage range. For long duration surges such as automotive load dump, C1 becomes prohibitively large and Zener D1 is the most

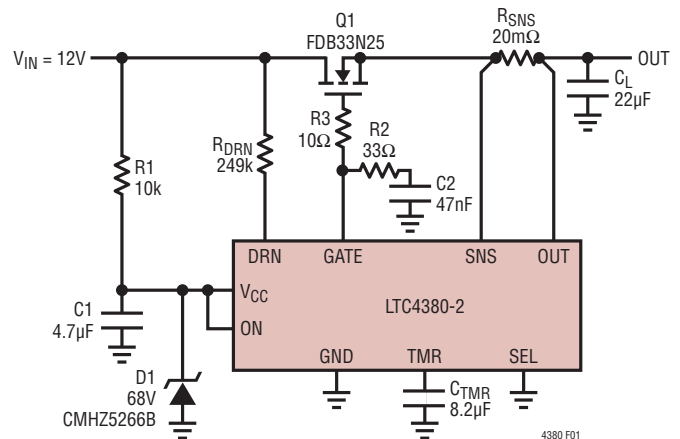


Figure 1. 12V/1A, Output Limited to 27V

## APPLICATIONS INFORMATION

effective means of limiting the  $V_{CC}$  voltage. Using a 68V Zener assures that D1 will not override the internal GATE pin clamp in the LTC4380-1 and LTC4380-2 devices. For the LTC4380-3 and LTC4380-4, the  $V_{CC}$  operating range extends from 4V to 72V. Since the GATE pin is regulated to  $V_{OUT} + 11.5V$ , D1 is chosen to achieve the desired output clamping effect while at the same time keeping the  $V_{CC}$  pin within its 4V to 72V range.

### Fault Timer Overview

Overvoltage and overcurrent conditions, and high  $V_{DS}$  conditions in Q1 are limited in duration by an adjustable fault timer. A capacitor at the TMR pin  $C_{TMR}$  sets the delay time before a fault condition is reported at the  $\overline{FLT}$  pin and Q1 is turned off.  $C_{TMR}$  also sets the cool down time before Q1 is permitted to turn back on for the LTC4380-2 and LTC4380-4 auto retry versions. The LTC4380-1 and LTC4380-3 versions simply latch off at the end of the timer delay.

Fault timing starts as soon as the input power is applied with the part in the on condition, or when the part is turn on after application of power. A  $1.5\mu A$  current is generated to pull up the TMR pin when the voltage across the MOSFET is higher than 0.7V. The timer speeds up with an additional current that varies with the power dissipated in the MOSFET, Q1. The power dissipation is the product of the voltage across the MOSFET ( $V_{DS}$ ) and the current flowing through it ( $I_D$ ).  $V_{DS}$  is inferred from the voltage drop across the drain pin resistor,  $R_{DRN}$ , while  $\Delta V_{SNS}$  represents  $I_D$ .

At initial power-up, the  $1.5\mu A$  pilot current charges the TMR pin capacitor because the input supply is, at least for a short time, more than 0.7V above the output voltage. When the output rises to within 0.7V of the input supply voltage, the pull-up current disappears and an internal  $2\mu A$  current source discharges the TMR pin capacitor. The capacitor must be sized to ride through the initial start-up interval for successful power-up.

In the presence of a sustained fault, the timer current charges the TMR pin to 1.215V. At this point the  $\overline{FLT}$  pin pulls low to indicate a fault condition and the GATE pin pulls low, shutting off the MOSFET. After faulting off, the timer enters the cool down phase. At the end of the cool down period the LTC4380-1/LTC4380-3 remain off until manually reset,

while the LTC4380-2/LTC4380-4 automatically restart.

### Fault Timer Operation in Overvoltage

During an overvoltage condition, where the MOSFET's  $V_{DS}$  exceeds 0.7V, the TMR pin charges from 0V to 1.215V with a current that varies principally as a function of  $V_{DS}$  and  $I_D$ .  $V_{DS}$  is inferred from the current flowing in the DRN pin resistor,  $R_{DRN}$ , while the voltage difference between the SNS and OUT pins ( $\Delta V_{SNS}$ ) represents the MOSFET current,  $I_D$ .

The TMR pin current is given by

$$I_{TMR} = 1.5 \cdot 10^{-6} A + 0.0917 \left[ \frac{\sqrt{A}}{V} \right] \cdot \Delta V_{SNS} \cdot \sqrt{I_{DRN}}$$

Where  $1.5 \cdot 10^{-6} A$  is the minimum TMR current and  $0.0917 \sqrt{A}/V$  is the gain term of the multiplier.

Substituting for  $\Delta V_{SNS}$  and  $I_{DRN}$

$$I_{TMR} = 1.5 \cdot 10^{-6} A + 0.0917 \left[ \frac{\sqrt{A}}{V} \right] \cdot I_D \cdot \sqrt{V_{DS}} \frac{R_{SNS}}{\sqrt{R_{DRN}}}$$

When TMR reaches 1.215V, the  $\overline{FLT}$  pin pulls low and the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of output clamping and turning off is given by:

$$t_{TMR} = V_{TMR(F)} \cdot \frac{C_{TMR}}{I_{TMR}}$$

Because  $I_{TMR}$  is a function of  $V_{DS}$  and  $I_D$ , the exact time spent in overvoltage before turning off depends upon the input waveform and the load current.

### Fault Timer Operation in Overcurrent

TMR pin behavior in overcurrent is substantially the same as in overvoltage. In the presence of an overcurrent condition when the LTC4380 regulates the output current, the TMR pin charges from 0V to 1.215V with a current that varies principally as a function of the power dissipated on the MOSFET. In addition to the variable current, an additional  $27\mu A$  hastens timeout in a low impedance short where the output is less than 1.5V. This additional current is reduced to  $7\mu A$  when  $V_{OUT}$  is above 3V.

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The TMR pin current with  $V_{OUT}$  less than 1.5V is given by

$$I_{TMR} = (27 + 1.5) \cdot 10^{-6} \text{A} + 0.0917 \left[ \frac{\sqrt{A}}{V} \right] \cdot I_D \cdot \sqrt{V_{DS}} \frac{R_{SNS}}{\sqrt{R_{DRN}}}$$

Where  $27 \cdot 10^{-6} \text{A}$  is the extra TMR current during overcurrent condition.

And with  $V_{OUT}$  above 3V

$$I_{TMR} = (7 + 1.5) \cdot 10^{-6} \text{A} + 0.0917 \left[ \frac{\sqrt{A}}{V} \right] \cdot I_D \cdot \sqrt{V_{DS}} \frac{R_{SNS}}{\sqrt{R_{DRN}}}$$

Where  $7 \cdot 10^{-6} \text{A}$  is the extra TMR current during overcurrent condition.

When TMR reaches 1.215V, the  $\overline{FLT}$  pin pulls low and the MOSFET is turned off and allowed to cool for an extended period. The total elapsed time between the onset of output clamping and turning off is given by

$$t_{TMR} = V_{TMR(F)} \cdot \frac{C_{TMR}}{I_{TMR}}$$

Because  $I_{TMR}$  is a function of  $V_{DS}$  and  $I_D$ , the exact time spent in overcurrent before turning off depends upon the input waveform, the output voltage and the time required for the output current to come into regulation.

### Cool Down Phase

Cool down behavior is the same whether initiated by overvoltage or overcurrent. During the cool down phase, the timer continues to charge from 1.215V to 3.4V with  $2\mu\text{A}$ , and then discharge back down to 1.215V with  $2\mu\text{A}$ . This cycle repeats 14 times and at the 15th cycle the TMR pin is pulled all the way to ground. The total cool down time is given by:

$$t_{COOL} = C_{TMR} \frac{15 \cdot 4.37\text{V} + (1.215\text{V} - 0.1\text{V})}{2\mu\text{A}}$$

Up to this point the operation of the LTC4380-1/LTC4380-3 and LTC4380-2/LTC4380-4 is the same. Behavior at the end of the cool down phase is entirely different.

At the end of the cool down phase, when TMR crosses the 100mV reset threshold, the LTC4380-1/LTC4380-3 remain latched off and  $\overline{FLT}$  remains low. They may be restarted by pulling the ON pin low for at least  $100\mu\text{s}$  or by cycling the power supply. The cool down phase may be interrupted at anytime by pulling the ON pin low for at least  $10\text{ms}/\mu\text{F}$  of  $C_{TMR}$ ; the LTC4380-1/LTC4380-3 will restart when ON goes high. The LTC4380-2/LTC4380-4 will automatically retry at the end of the cool down phase without cycling the ON pin and the cool down phase may be interrupted by pulling the ON pin low for at least  $10\text{ms}/\mu\text{F}$  of  $C_{TMR}$ .

For both versions, the  $\overline{FLT}$  pin goes high in shutdown and is cleared high when power is first applied to  $V_{CC}$ . If  $\overline{FLT}$  is set low, it can be reset during the cool down phase by pulling the ON pin low for at least  $10\text{ms}/\mu\text{F}$  of  $C_{TMR}$ .

### Supply Transient Protection

The LTC4380 is tested to operate to 72V and guaranteed to be safe from damage up to 80V. Nevertheless, voltage transients above 80V may cause permanent damage. During a short-circuit condition, the large change in current flowing through power supply traces and associated wiring can cause inductive voltage transients which can exceed 80V. To minimize the voltage transients, minimize the power trace parasitic inductance by using short, wide traces. An RC filter at the  $V_{CC}$  pin is an effective measure against voltage spikes.

Another way to limit transients to less than 80V at the  $V_{CC}$  pin is to use a small Zener diode and a resistor, D1 and R1 in Figure 1. The Zener diode limits the voltage at the pin while the resistor limits the current through the diode to a safe level during the surge. However, D1 can be omitted if the filtered voltage at the  $V_{CC}$  pin, due to R1 and C1, stays below 80V. The inclusion of R1 in series with the  $V_{CC}$  pin modestly increases the minimum required voltage at  $V_{IN}$  due to the extra voltage drop across it from the small  $V_{CC}$  current of the LTC4380 and the leakage current of D1.

A total bulk capacitance of at least  $22\mu\text{F}$  low ESR electrolytic or ceramic is required close to the source pin of MOSFET Q1.



## APPLICATIONS INFORMATION

### MOSFET Selection

The LTC4380 drives an N-channel MOSFET to carry the load current. The important features of the MOSFET are on-resistance  $R_{DS(ON)}$ , the maximum drain-source voltage  $V_{(BR)DSS}$ , the threshold voltage, and the safe operating area (SOA).

The maximum allowable drain-source voltage must be higher than the peak supply voltage. If the output is off or shorted to ground during an overvoltage event, the full supply voltage will appear across the MOSFET.

The gate drive for the MOSFET is guaranteed to be more than 10V and less than 14V above the OUT pin for those applications with  $V_{CC}$  higher than 8V. This allows the use of a standard threshold voltage N-channel MOSFET. For systems with steady state  $V_{CC}$  less than 8V, a logic level MOSFET is required since the gate drive can be as low as 5V.

The SOA of the MOSFET must encompass all fault conditions. In normal operation the MOSFET is fully on, dissipating very little power. But during overvoltage or overcurrent faults, the GATE pin is either clamped to limit the output voltage or controlled to regulate the current through the MOSFET. Large current and high voltage drop across the MOSFET can coexist and dissipate significant power in these cases. The SOA curves of the MOSFET must be considered carefully in conjunction with the selection of the fault timer capacitor.

### Transient Stress in the MOSFET

During an overvoltage event, the LTC4380 clamps the gate of the pass MOSFET to limit the output voltage at an acceptable level. The load circuitry may continue operating throughout this interval, but only at the expense of dissipation in the MOSFET pass device. MOSFET dissipation or stress is a function of the input voltage waveform, output voltage and load current. The MOSFET must be sized to survive this stress.

Most transient event specifications use the prototypical waveshape shown in Figure 2, comprising a linear ramp of rise time  $t_r$ , reaching a peak voltage of  $V_{PK}$  and exponentially decaying back to  $V_{IN}$  with a time constant of  $\tau$ . A common automotive transient specification has constants of  $t_r = 10\mu s$ ,  $V_{PK} = 80V$  and  $\tau = 1ms$ . A surge

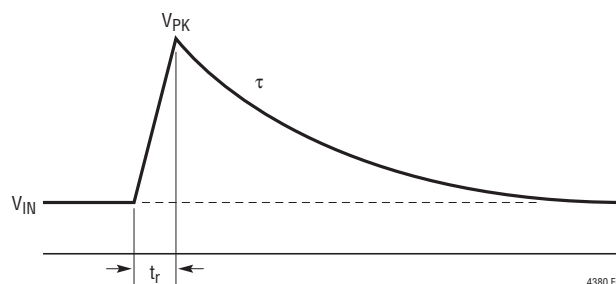


Figure 2. Prototypical Transient Waveform

condition known as load dump commonly has constants of  $t_r = 5ms$ ,  $V_{PK} = 60V$  and  $\tau = 200ms$ .

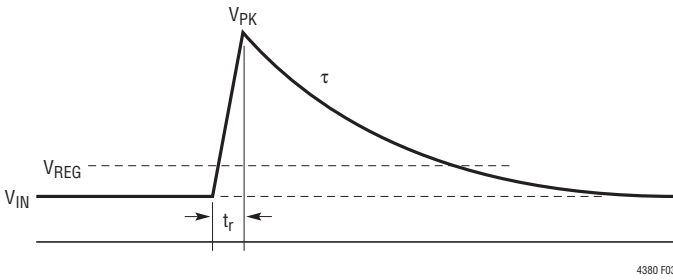
MOSFET stress is the result of power dissipated within the device. For long duration surges of 100ms or more, stress is increasingly dominated by heat transfer out of the package; this is a matter of device packaging and mounting, and heat sink thermal mass. This is best analyzed by simulation, using the MOSFET thermal model.

For short duration transients of less than 100ms, MOSFET survival is a matter of safe operating area (SOA), an intrinsic property of the MOSFET. SOA quantifies the time required at any given condition of  $V_{DS}$  and  $I_D$  to raise the junction temperature of the MOSFET to its rated maximum. MOSFET SOA can be expressed in units of watt-squared-seconds ( $P^2t$ ). This figure is essentially constant for intervals of less than 100ms for any given device type, and rises to infinity under DC operating conditions. Destruction mechanisms other than bulk die temperature distort the lines of an accurately drawn SOA graph so that  $P^2t$  is not the same for all combinations of  $I_D$  and  $V_{DS}$ . In particular  $P^2t$  tends to degrade as  $V_{DS}$  approaches the maximum rating, rendering some devices useless for absorbing energy above a certain voltage.

### Calculating Transient Stress

To select a MOSFET suitable for any given application, the SOA stress must be calculated or simulated for each input transient which shall not interrupt operation. It is then a simple matter to choose a device which has adequate SOA to survive the maximum calculated stress.  $P^2t$  for a prototypical transient waveform is calculated as follows (Figure 3):

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**Figure 3. Safe Operating Area Required to Survive Prototypical Transient Waveform**

Let

$$a = V_{REG} - V_{IN}$$

$$b = V_{PK} - V_{IN}$$

( $V_{IN}$  = Nominal Input Voltage)

Then

$$P^2t = I_{LOAD}^2 \cdot$$

$$\left[ \frac{1}{3} t_r \frac{(b-a)^3}{b} + \frac{1}{2} \tau \left( 2a^2 \ln \frac{b}{a} + 3a^2 + b^2 - 4ab \right) \right]$$

For the transient conditions of  $V_{PK} = 100V$ ,  $V_{IN} = 12V$ ,  $V_{REG} = 27V$ ,  $t_r = 10\mu s$ ,  $\tau = 1ms$ , and a load current of 3A,  $P^2t$  is  $18W^2s$  which can be handled by a MOSFET in a DPAK package. The  $P^2t$  of other transient waveshapes is evaluated by integrating the square of MOSFET power over time. LTspice® can be used to simulate timer behavior for more complex transients and cases where overvoltage and overcurrent faults coexist, as well as the peak temperature rise of the MOSFET.

### Calculating Short-Circuit Stress

SOA stress must also be calculated for a short-circuit condition. Short-circuit  $P^2t$  is given by:

$$P^2t = \left( \Delta V_{DS} \cdot \frac{\Delta V_{SNS}}{R_{SNS}} \right)^2 \cdot t_{TMR} \quad [W^2s]$$

Where  $\Delta V_{DS}$  is the voltage across the MOSFET,  $\Delta V_{SNS}$  is the current limit threshold and  $t_{TMR}$  is the overcurrent timer interval.

For  $V_{IN} = 15V$ ,  $\Delta V_{DS} = 12V$  ( $V_{OUT} = 3V$ ),  $\Delta V_{SNS} = 50mV$ ,  $R_{SNS} = 12m\Omega$ ,  $R_{DRN} = 100k\Omega$  and  $C_{TMR} = 68nF$ ,  $P^2t$  is  $24.5W^2s$  – somewhat higher than the transient SOA calculated in the previous example.

### Limiting Inrush Current and GATE Pin Compensation

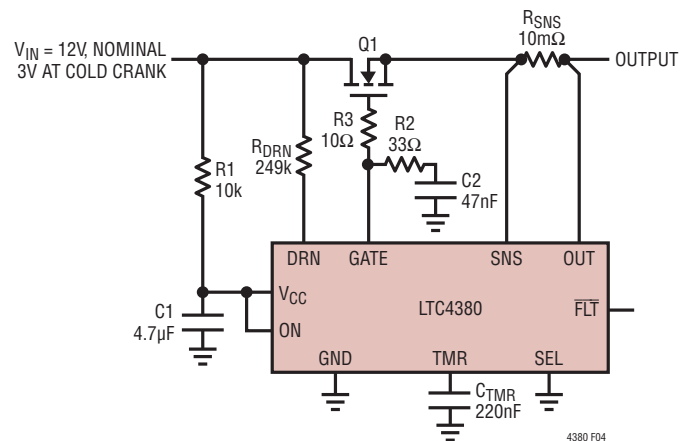
The LTC4380 limits the inrush current to any load capacitance by controlling the GATE pin voltage slew rate. An external capacitor, C2, can be connected from GATE to ground to reduce the inrush current at the expense of slower turn-off time. The gate capacitor is set at:

$$C2 = I_{GATE(UP)} \cdot \frac{C_L}{I_{INRUSH}}$$

The LTC4380 needs a minimum of 47nF capacitance (C2) and a 33Ω (R2) resistor in series at the GATE pin to stabilize the current limit amplifier during an overcurrent event. C2 also limits self enhancement of the MOSFET. A 10Ω resistor, R3, is connected to the gate of the MOSFET to suppress parasitic oscillations.

### Automobile Cold Crank Ride Through

During cold crank the battery potential drops from the 12V nominal to as low as 3V for up to 40ms. The LTC4380 needs at least 4V at the  $V_{CC}$  pin to function correctly. The low quiescent current requirement of the part allows an RC filter with reasonable values to be placed at the  $V_{CC}$  pin to ride through cold crank, as shown in Figure 4.



**Figure 4. Automotive Cold Crank Ride Through**





## APPLICATIONS INFORMATION

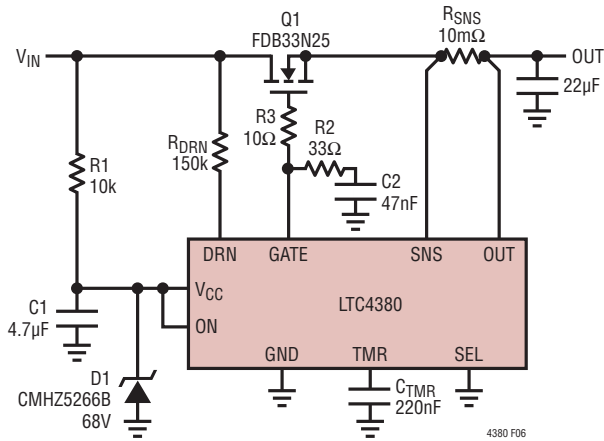


Figure 6. Design Example

CMHZ5266B can handle 500mW indefinitely and 1W for 1 second.

The  $V_{CC}$  pin needs at least 4V to operate through cold crank from 12V down to 3V for 40ms. The value of C1 can be calculated as:

$$C1 = \frac{-40\text{ms}}{10\text{k}\Omega \cdot \ln\left(\frac{1}{9}\right)} = 1.82\mu\text{F}$$

4.7µF is chosen to accommodate for the supply current of the part and other conditions.

With  $C1 = 4.7\mu\text{F}$  and  $R1 = 10\text{k}\Omega$ , high voltage transients up to 200V with a pulse width of less than 10ms are filtered out at the  $V_{CC}$  pin. Longer surges are suppressed by D1.

Next calculate the sense resistor ( $R_{SNS}$ ) value where the current limit threshold is 50mV:

$$R_{SNS} = \frac{50\text{mV}}{I_{LIM}} = \frac{50\text{mV}}{5\text{A}} = 10\text{m}\Omega$$

$R_{DRN}$  is chosen to produce a current into the DRN pin of 1mA, during the maximum overvoltage transient event:

$$R_{DRN} = \frac{150\text{V} - 27\text{V}}{1\text{mA}} = 123\text{k}\Omega$$

150kΩ is chosen to ensure enough margin.

Next  $C_{TMR}$  is chosen to power up the output before the TMR pin reaches the gateoff threshold of 1.215V:

$$C_{TMR} = \frac{I_{TMR(UP)} \cdot t_{INRUSH}}{V_{TMR}}$$

Where

$$t_{INRUSH} = \frac{V_{IN} \cdot C2}{I_{GATE(UP)}} = V_{IN} \frac{C_{LOAD}}{I_{INRUSH}}$$

$$= \frac{14\text{V} \cdot 47\text{nF}}{20\mu\text{A}} = 32.9\text{ms}$$

$I_{TMR(UP)} \approx 1.5\mu\text{A}$ . To limit the rise of  $V_{TMR}$  to 0.4V

$$C_{TMR} = \frac{1.5\mu\text{A} \cdot 32.9\text{ms}}{0.4\text{V}} \approx 123\text{nF}$$

220nF is chosen to accommodate all conditions.

The pass transistor, Q1, should be chosen to withstand an output short with  $V_{CC} = 14\text{V}$ . In the case of a severe output short where  $V_{OUT} = 0\text{V}$ , the total overcurrent fault time is:

$$t_{oc} = \frac{220\text{nF} \cdot 1.215\text{V}}{30.5\mu\text{A}} = 8.76\text{ms}$$

The power dissipation in Q1 is:

$$P = \frac{14\text{V} \cdot 68\text{mV}}{10\text{m}\Omega} = 95.2\text{W}$$

and  $P^2t = 79.4\text{W}^2\text{S}$

During an output overload or soft short, the voltage at the OUT pin could stay at 3V or higher. The total overcurrent fault time when  $V_{OUT} = 3\text{V}$  is:

$$t_{oc} = \frac{220\text{nF} \cdot 1.215\text{V}}{9.75\mu\text{A}} = 27.4\text{ms}$$

The power dissipation in Q1 is:

$$P = \frac{(14\text{V} - 3\text{V}) \cdot 50\text{mV}}{10\text{m}\Omega} = 55\text{W}$$

and  $P^2t \approx 83\text{W}^2\text{S}$

These conditions are well within the safe operating area of the FDB33N25.

APPLICATIONS INFORMATION

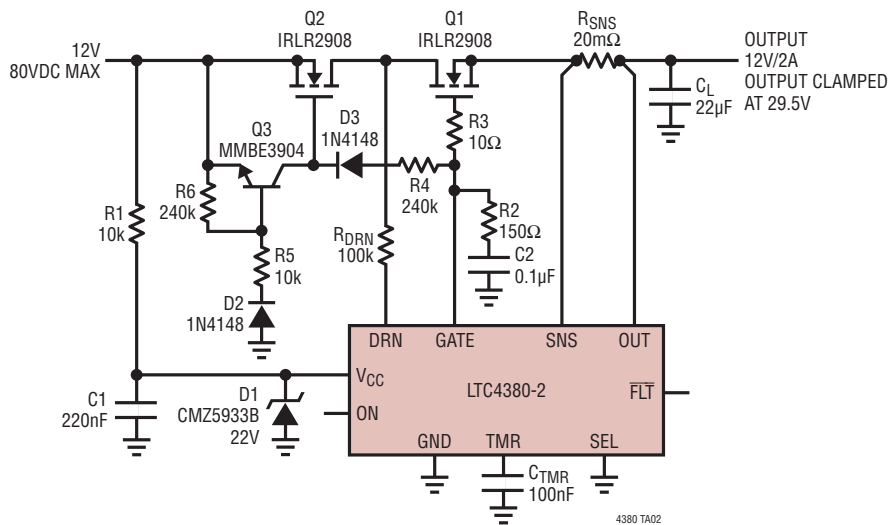


Figure 7. 12V Overcurrent Protected High Side Switch

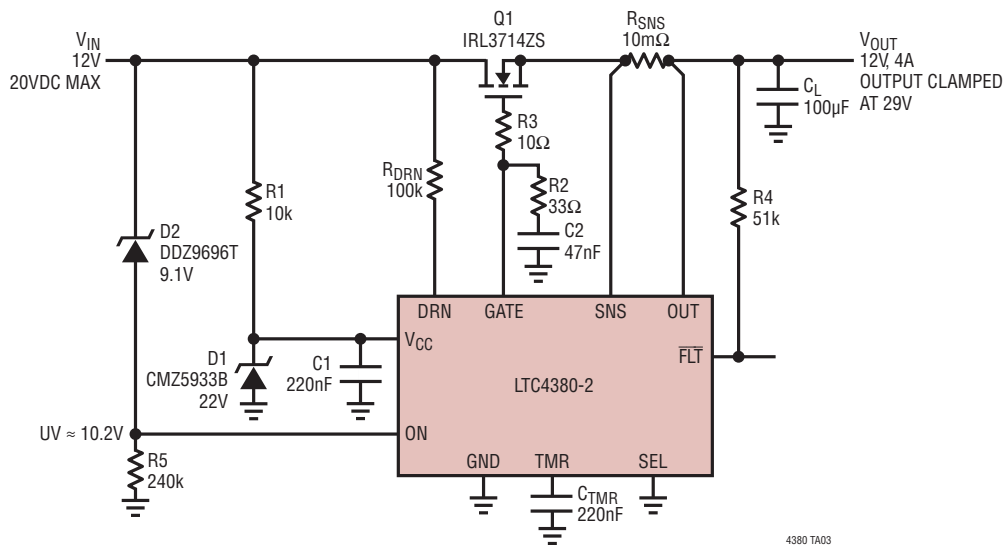


Figure 8. 12V Hot Swap Controller with Input UV Detection

## APPLICATIONS INFORMATION

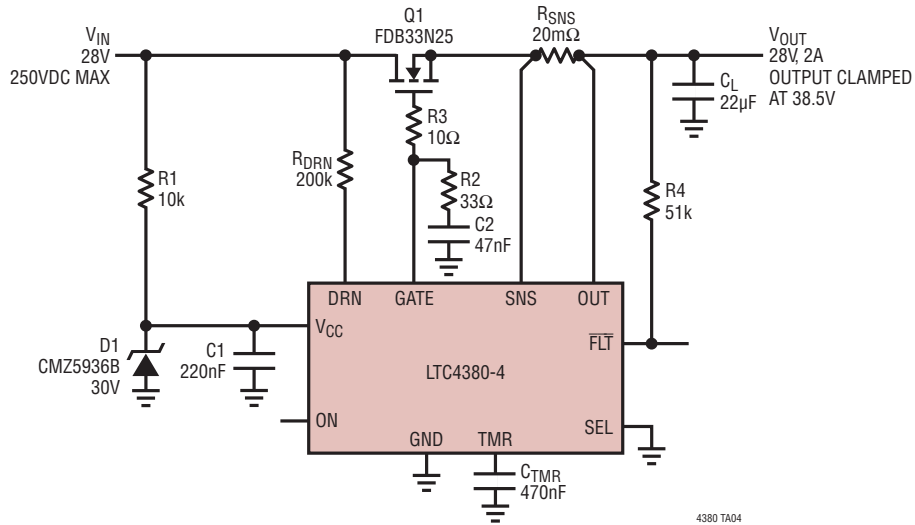


Figure 9. 28V Surge Stopper with Output Clamped to Below 40V

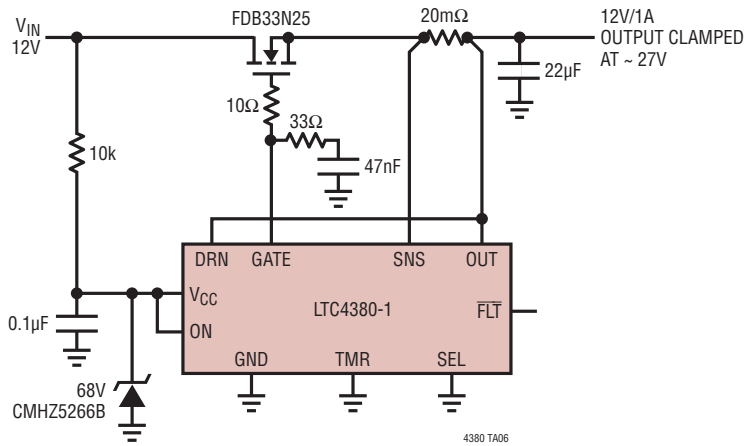
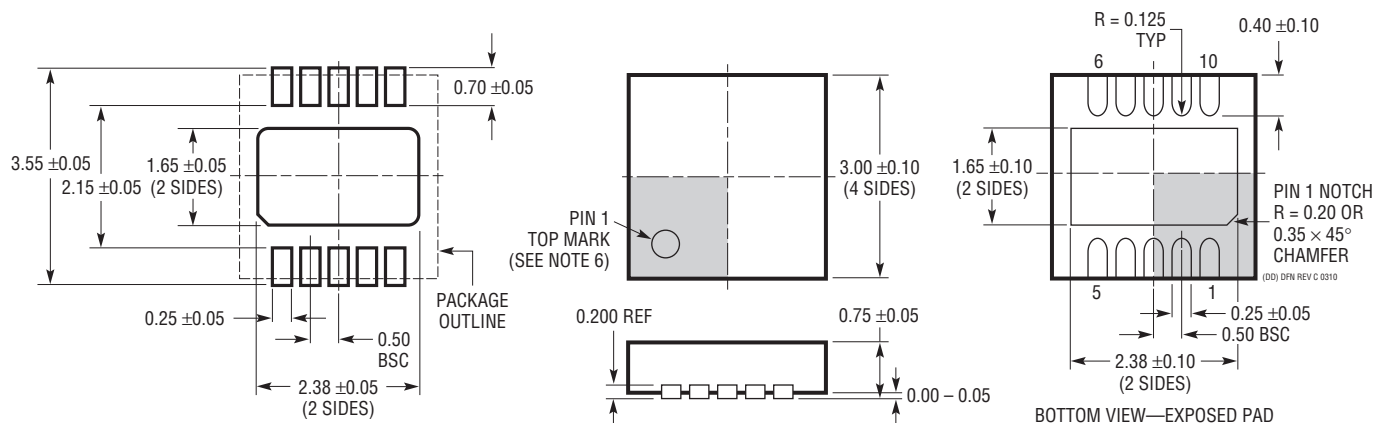


Figure 10. 12V Surge Stopper with Fault Timer Disabled

# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC4380#packaging> for the most recent package drawings.

## DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699 Rev C)

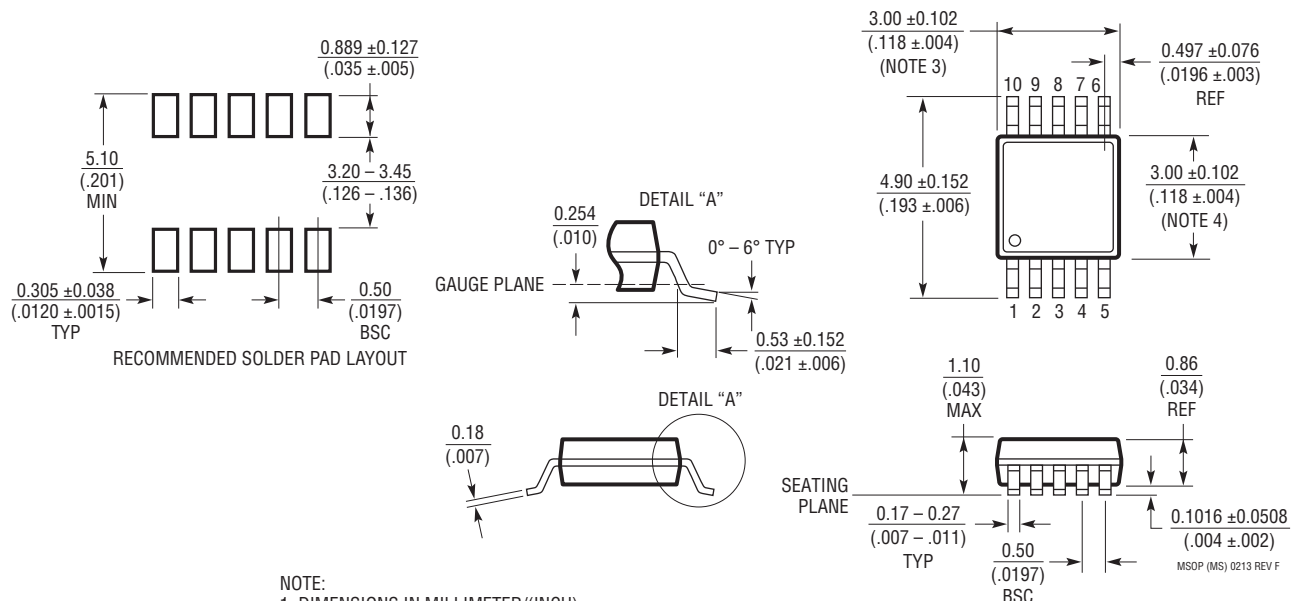


### RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

**NOTE:**

- DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE MO-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
- DRAWING NOT TO SCALE
- ALL DIMENSIONS ARE IN MILLIMETER
- DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
- EXPOSED PAD SHALL BE SOLDER PLATED
- SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## MS Package 10-Lead Plastic MSOP (Reference LTC DWG # 05-08-1661 Rev F)



**NOTE:**

- DIMENSIONS IN MILLIMETER/(INCH)
- DRAWING NOT TO SCALE
- DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
- DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
- LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

## TYPICAL APPLICATION

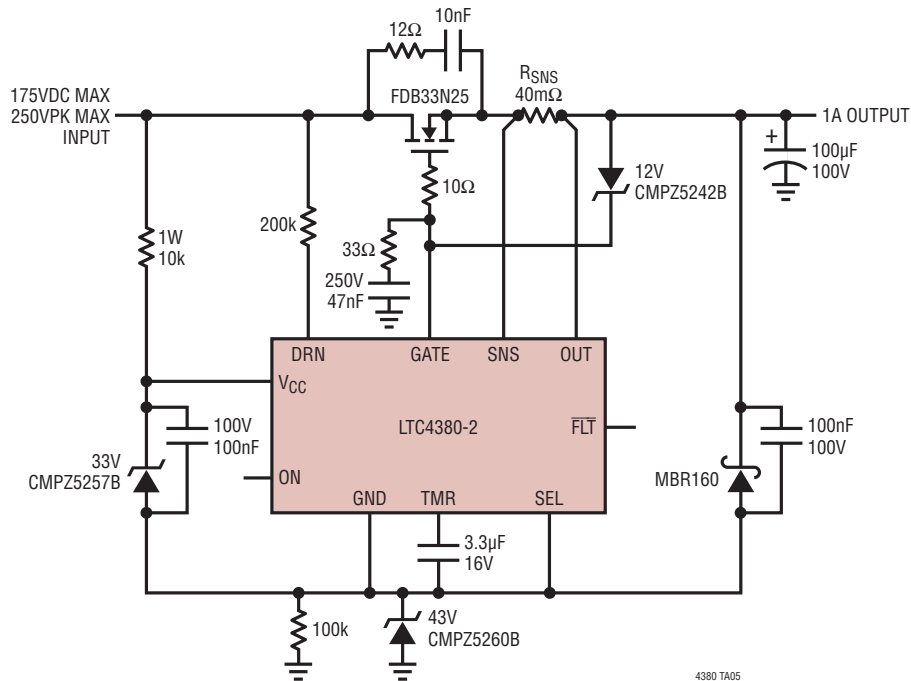


Figure 11. 48V Floating Surge Stopper

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LT4356</a>	Surge Stopper with Current Limit	4V to 80V Operation, 100V Protection, DFN-12, MSOP-10 and SO-16 Packages
<a href="#">LTC4359</a>	Ideal Diode Controller	4V to 80V Operation, -40V Input Protection, DFN-8, MSOP-8 Packages
<a href="#">LTC4361</a>	Overvoltage/Overcurrent Protection Controller	2.5V to 5.5V Operation, 80V Protection, TSOT-8 and DFN-8 Packages
<a href="#">LT4363</a>	Surge Stopper with Current Limit	4V to 80V Operation, >100V Protection, DFN-12, MSOP-12 and SO-16 Packages
<a href="#">LTC4364</a>	Surge Stopper with Ideal Diode	4V to 80V Operation, -40V to >100V Protection, DFN-14, MSOP-16 and SO-16 Packages
<a href="#">LTC4365</a>	OV, UV and Reverse Input Protection Controller	2.5V to 34V Operation, -40V to 60V Protection, DFN-8 and TSOT-8 Packages
<a href="#">LTC4366</a>	High Voltage Surge Stopper	9V to >500V Operation, Floating Topology, TSOT-8 and DFN-8 Packages
<a href="#">LTC4367</a>	OV, UV and Reverse Input Protection Controller	2.5V to 60V Operation, -40V to 100V Protection, DFN-8 and MSOP-8 Packages
<a href="#">LTC7860</a>	Switching Surge Stopper	3.5V to 60V Operation, >100V Protection, MSOPE-12 Package