ispLEVER™

THE SIMPLE MACHINE FOR COMPLEX DESIGN

Lattice® Semiconductor Corporation

ispLEVER™

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The Simple Machine for Complex Design

Lattice's ispLEVER software features a comprehensive set of powerful tools, including everything you need to take your FPGA or CPLD design from concept to a programmed device. The ispLEVER software family supports all Lattice programmable products with a push-button design environment and advanced features for design optimization and debug.

There are four variations of ispLEVER tailored to meet your specific design requirements. A handy reference chart detailing the features of each ispLEVER variation is provided at the end of this brochure.

ispLEVER

ispLEVER is the flagship design environment for the newest Lattice FPGA products. It is provided on CD-ROM and DVD for Windows, UNIX, or Linux platforms, and can be ordered from your local sales representative or purchased online.

ispLEVER for Windows also includes industry leading 3rd party tools from Lattice partners Synplicity® and Mentor Graphics® for synthesis and simulation.

ispLEVER for Windows and Linux include a USB download cable for programming Lattice silicon devices.

ispLEVER PRO

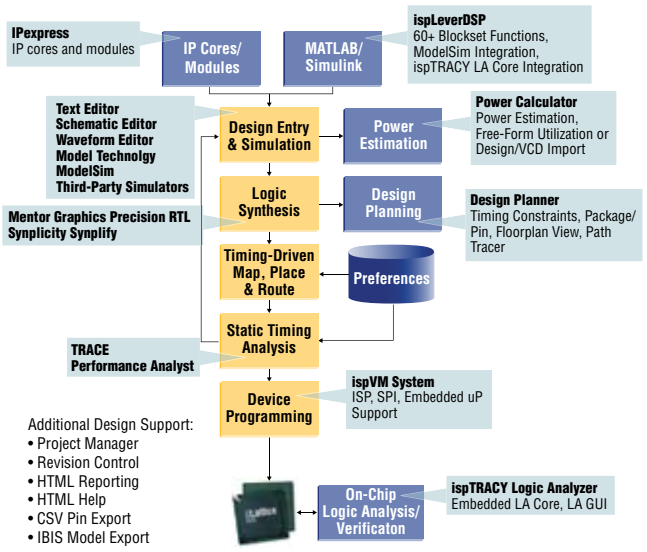
ispLEVER PRO includes all the features and functionality of the ispLEVER software, and adds the Lattice IP Value suite, which includes DDR, DDR2, FIR Filter, FFT and Tri-Speed MAC IP cores. These IP cores can be used repeatedly on multiple FPGA platforms during the license period. ispLEVER Pro is available via a 1-year subscription license on the Windows platform.

ispLEVER Starter

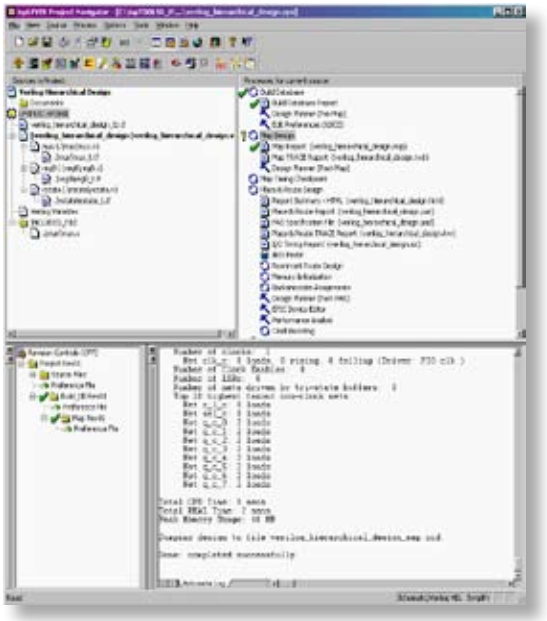
ispLEVER Starter is a downloadable version of ispLEVER for Windows XP or 2000. It is a complete design environment for selected Lattice digital devices.

ispLEVER Classic

ispLEVER Classic is a complete design environment for mature Lattice programmable products. It is downloadable from the Lattice website.



ispLEVER Design Flow



ispLEVER Project Navigator

Key Features

Project Navigator

Project Navigator is the ispLEVER project management interface. The entire set of ispLEVER tools can be accessed from this interface. Your project files, including the current target device, are shown in heirarchical format on the left side of the screen. Tasks associated with those project files are shown on the right side. Other optional windows

Key Features, Cont.

display revision control information, a log file, reports and more. Completing your design can be as simple as double-clicking the task you want to perform and letting ispLEVER do the rest.

Power Calculator

The ispLEVER Power Calculator includes an environment-aware power model, graphical power displays and a variety of useful reports. Thermal resistance options model real world thermal conditions, including heatsinks, airflow, and the printed circuit board complexity, while graphical power curves illustrate operating temperature profiles.

FPGA Design Planner

The Design Planner is a centralized interface where you can perform all floorplanning, path analysis, I/O assignment, PLL definition, and other implementation tasks. All design preferences are stored in a centralized database file, which can be edited from any point in the design process.

Simulink Blockset – ispLeverDSP

ispLEVER includes DSP blocks that can be used to build DSP solutions within the MATLAB/Simulink environment. These solutions can then be exported in HDL optimized for Lattice FPGA architectures.

IPexpress

IPexpress is the interface to the Lattice catalog of functional modules, reference designs, and intellectual property (IP), all optimized for Lattice programmable products. IPexpress accelerates the design process by helping you smoothly configure and integrate these functions into your design.

Performance Analyst™ Timing Analyzer

Performance Analyst is a powerful static timing analyzer that allows users to rapidly analyze critical timing requirements and experiment with devices of differing speed grades without recompiling the design.

HTML-Based Reporting

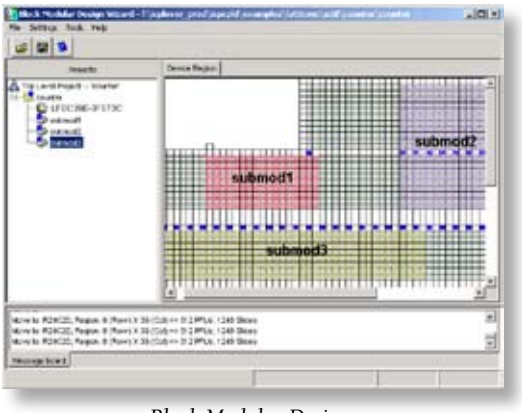
Report viewing is made easy through standard web browsers.

Reveal Logic Analyzer

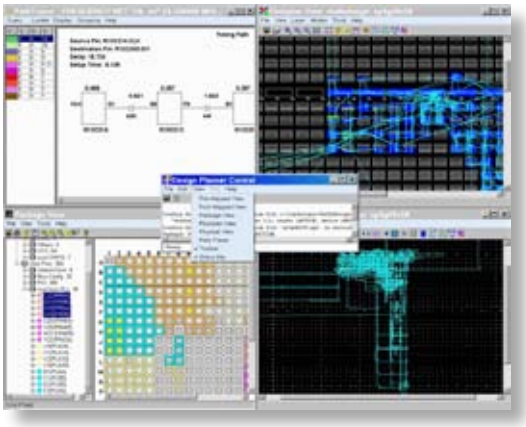
The Reveal Logic Analyzer uses a signal-centric model for embedded logic debug; the user first defines signals of interest and the Reveal tool then inserts the instrumentation along with the proper connections to enable the required observations. The ability to specify complex, multi-event triggering sequences makes system-level design debug smoother and faster.

HDL Explorer

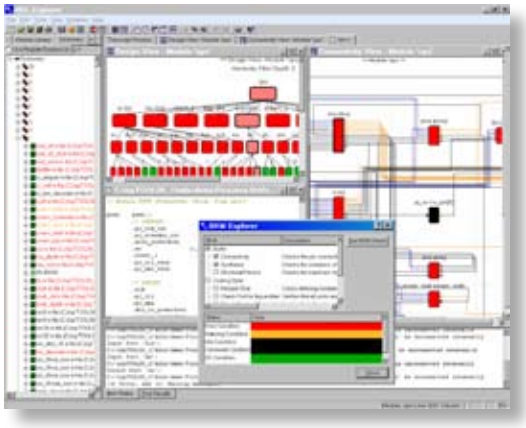
HDL Explorer generates graphic representations of your HDL's hierarchical structure and connectivity. You can use intelligent tools to cross-probe between views, pinpoint problems and more.



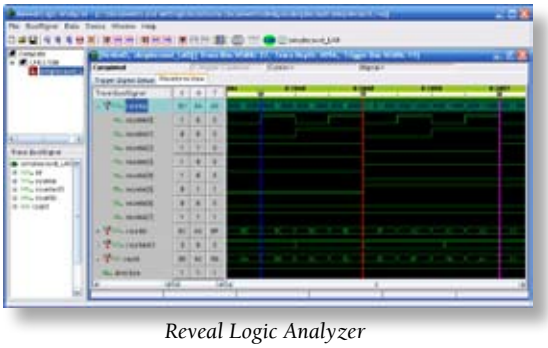
Block Modular Design



FPGA Design Planner



HDL Explorer



Reveal Logic Analyzer

Integrated Third-Party OEM Partner Tools

Lattice works closely with industry leaders Mentor Graphics® and Synplicity® to provide the best synthesis and simulation tools available. The tools described below are included with ispLEVER for Windows, fully integrated into the ispLEVER design flow.

Precision® RTL Synthesis

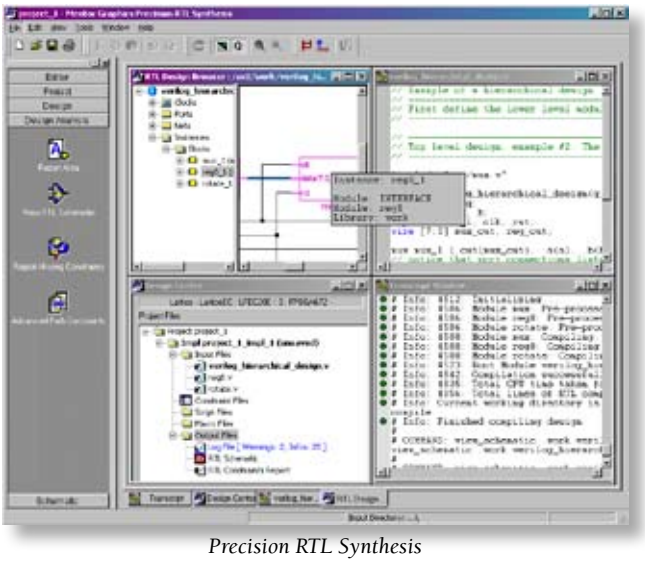
Precision RTL is Mentor Graphics' premier RTL synthesis solution. The intuitive Precision RTL interface gives easy access to powerful features and tools such as a schematic (RTL/Technology) viewer, constraint analyzer, PreciseTime (for advanced timing analysis iteration), re-timing support and more. These advanced tools help improve your efficiency and ultimately help optimize your quality of results.

Synplify® Synthesis

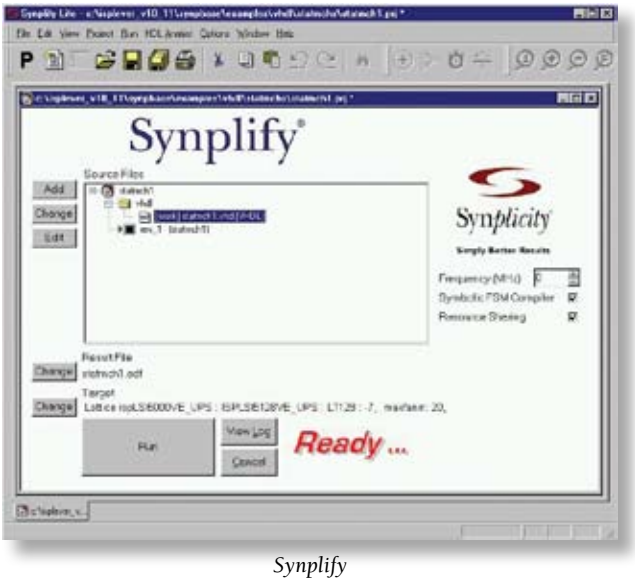
The Synplify solution from Synplicity is a high-performance, sophisticated logic synthesis engine that utilizes proprietary Behavior Extracting Synthesis Technology (B.E.S.T.™) to deliver fast, highly efficient FPGA and CPLD designs. Synplify uses Verilog and VHDL Hardware Description Languages as input and outputs an optimized netlist for the Lattice device.

ModelSim Simulation

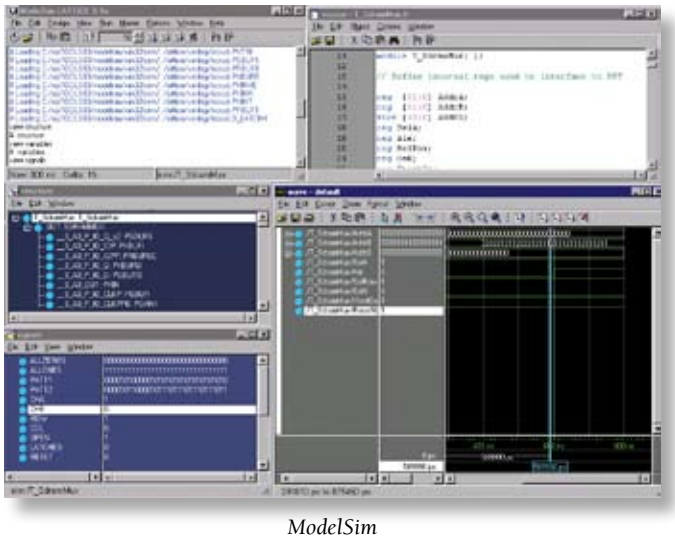
ModelSim offers VHDL and Verilog language and gate-level timing simulation. An easy-to-use graphical user interface enables users to quickly identify and debug problems. Dynamically updated windows enable design debug using a natural, intuitive thought process. For example, selecting a design region in the structure window automatically updates the Source, Signals, Process and Variables windows. If a problem is found, it can be edited, re-compiled and re-simulated without leaving the simulator.



Precision RTL Synthesis



Synplify



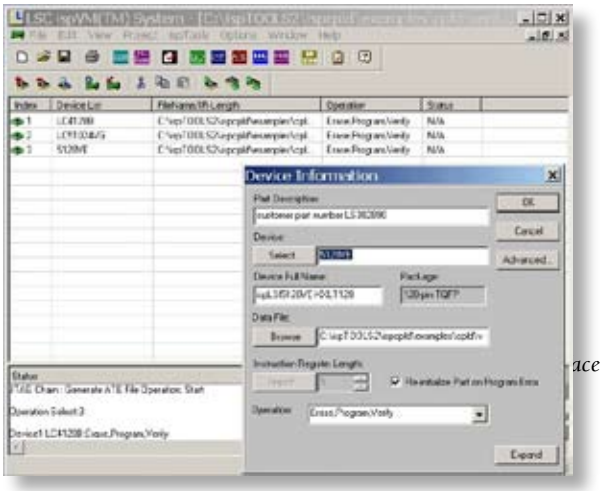
ModelSim

Programming Tools

ispVM® System Software

Lattice's ispVM System software is a comprehensive device programming manager. It provides an efficient method of programming Lattice devices using JEDEC and Bitstream files generated by ispLEVER, PAC-Designer®, and other design tools. ispVM System is available for download from the Lattice website at: www.latticesemi.com/ispvm.

- **ispVM-DLxConnect for Gang Programming**
- **New STAPL Programming Features:**
  - Accepts Non-Lattice STAPL file input
  - Outputs STAPL programming files for Lattice Flash based devices
  - STAPL Debugger
- **ISC Programming Features:**
  - Accepts ISC BSDL file input
  - Accepts ISC data file input
  - Supports 9 Lattice ISC-compliant device families
- **Supports Transparent Field Reconfiguration (TransFR) for the MachXO and LatticeXP FPGAs**
- **SPI Flash programming for the LatticeECP/EC, LatticeECP2/M, and LatticeSC/M FPGAs**
- **Supports Programming Through SVF File, ISC BSDL and data files, and STAPL files**
- **Support for IEEE 1532 (2000) programming standard**
- **Easy-to-Use Graphical User Interfaces (GUI)**
- **Command Line Mode**
- **Automatically Convert Existing .dld and .wch Files**
- **Built-in SVF (Serial Vector Format) File Editor**
- **Built-in ATE Programming Vector Generator**
  - Supports HP, Genrad, Teardyne, and Marconi ATE Equipment
  - Advanced ATE Vector Generation Features
- **Specify Programming Clock Frequency**
- **Specify Bypass Instructions**
- **USERCODE/UES Editor**
- **User Accessible Comment Field**



ispVM System, Main User Interface

Programming Cables

Lattice offers ispDOWNLOAD® cables for quick and easy programming of devices on a target system board directly from a PC. Lattice ispDOWNLOAD cables are available with either Parallel or USB PC Connections, and 1x8, 2x5 or versitile flywire programming connectors. Every ispLEVER for Windows design tool includes a USB download cable.

Lattice USB Download Cable

Desktop Programming

The Lattice Model 300 is a desktop programmer supporting desktop programming of all Lattice non-volatile programmable CPLD devices. Lattice's ispVM System software includes an interface for the Model 300 Programmer. Programming adapters for various devices and packages are required and available for purchase separately. See the Lattice web site for ordering details and more information.

Model 300 Desktop Programmer plus Programming Adapters

ispLEVER Family Summary

	ispLEVER	ispLEVER PRO	ispLEVER Starter	ispLEVER Classic
Lattice FPGA/CPLD Support				
LatticeECP2M/S, LatticeSC/M, FreedomChip™	✔	✔		
LatticeECP2/S	✔	✔	LatticeECP2 Only	
MachXO™, LatticeECP/EC, LatticeXP™, LatticeXP2™	✔	✔	✔	
ispXPGA®, ORCA®, ispXPLD®, ispMACH™, ispLSI®, ispGDX/2, ispGAL®, GAL®				✔
Key Software Features				
Project Navigator (Design Management)	✔	✔	✔	✔
sysDSP™ Library for MATLAB®/Simulink®	✔	✔	Requires Standalone ModelSim	
Block Modular Design for FPGAs	✔	✔	✔	
IPexpress™ (IP & Module Configuration)	✔	✔	✔	
Module/IP Manager (Module Configuration)				✔
Power Calculator	✔	✔	✔	
IP Value Suite		✔		
Static Timing Analyzer/Performance Analyst	✔	✔	✔	✔
Lattice Logic Simulator				✔
HDL/SDF Export	✔	✔	✔	✔
HDL Explorer™	✔	✔		
Constraint/Preference Editor				✔
Design Planner	✔	✔	✔	
I/O Assistant	✔	✔	✔	
Reveal Logic Analyzer	✔	✔	✔	
ispTRACY Logic Analyzer	✔	✔	✔	ispXPGA Only
3rd-Party Software Included				
Synplify® for Lattice - Synthesis from Synplicity®	Windows Only	✔	✔	Windows Only
Precision® RTL - Synthesis from Mentor Graphics	Windows Only	✔	✔	Windows Only
ModelSim - Simulation from Mentor Graphics	Windows Only	✔		
Operating Systems and Ordering Information				
Windows (2000, XP)	✔ (LS-HDL-BASE-PC-N)	✔ (LS-HDL-PRO-PC-N)	✔	✔
Linux (Redhat Enterprise v.3 and v.4)	✔ (LS-ADV-LS-F Includes Classic Linux)			With ispLEVER purchase
UNIX (Solaris 2.8, 10)	✔ (LS-ADV-WS-F Includes Classic UNIX)			With ispLEVER purchase
Licensing and Updates				
License Terms	Perpetual	1 Year Subscription Extensions Available	6 Months, Renewable	1 Year, Renewable
Node-Locked License	Windows	✔	✔	✔
Floating License	Windows: Upgrade Available		N/A	N/A
Software Service Packs	Downloadable	Downloadable	N/A	N/A
Software "New Version" Upgrades	Included with Valid Software Maintenance	Included with Software Subscription License	Downloadable	Downloadable

Additional Software and Hardware Products

Product	Ordering Part Number
Floating License Upgrade for Windows	LS-FLOAT-PC
ActiveHDL Lattice Designer Edition Lite *(Optional Simulation Tool Suite)*	LS-AH-LDEL
ispDOWNLOAD Cable *(1.8V-5V Programming Cable, Flywire Connector)*	HW-DLN-3C
ispDOWNLOAD Cable *(1.2V-5V USB Programming Cable, Flywire Connector)*	HW-USBN-2A
ISP Engineering Kit – Model 300 *(Desktop Programmer)*	pDS4102-PM300
Programming Adapters *(Device/Package Programming Adapters for ISP Engineering Kit – Model 300)*	See Lattice website for Complete Listing

For More Information
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