LP3992 Micropower 1.5V CMOS Voltage Regulator with Shutdown Control

Check for Samples: LP3992

FEATURES

- **Operation from a Low Input Voltage; 1.9V**
- **Low Quiescent Current; 29µA Typical**
- **Stable with a Ceramic Capacitor**
- **Logic Controlled Shutdown**
- **Fast Turn ON and OFF**
- **Thermal-Overload and Short Circuit Protection**
- **5 Pin SOT-23 Package**
- **-40°C to +125°C Junction Temperature Range**

DESCRIPTION

The LP3992 regulator is designed to meet the requirements of portable, battery-powered systems providing an accurate output voltage, low noise, and low quiescent current. Battery life will be prolonged by the ability of the LP3992 to provide a 1.5V output from the low input voltage of 1.9V. Additionally, when switched to a shutdown mode via a logic signal at the shutdown pin, the power consumption is reduced to virtually zero. The LP3992 also features short-circuit and thermal-shutdown protection.

The LP3992 is designed to be stable with space saving ceramic capacitors as small as 1.0µF.

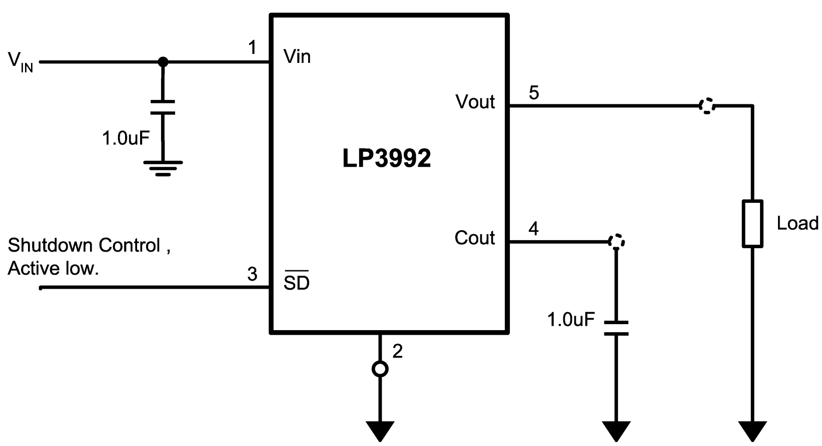
The device is available in a 5-pin, SOT-23 package. Performance is specified for a -40°C to 125°C temperature range.

For output voltages other than 1.5V and alternative package options, contact TI.

Table 1. Key Specifications

	VALUE	UNIT
Input range	1.9–5.2	V
Accurate output voltage	1.5V ± 0.09	V
Quiescent current in shutdown	Less than 1.5	µA
Stable with an output capacitor	1	µF
Guaranteed output current	30	mA
Low output voltage Noise	300	μV_{RMS}

Typical Application Circuit



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PIN DESCRIPTIONS

Pin No	Symbol	Name and Function
1	V_{IN}	Voltage Supply Input
2	GND	Common Ground
3	$\overline{SD}$	Shutdown input; Disables the regulator when ≤ 0.4V. Enables the regulator when ≥ 1.15V.
4	C_{OUT}	Output capacitor connection. Internally Connected to V_{OUT} connection. This is the recommended device connection for the 1.0µF output capacitor to guarantee a stable output.
5	V_{OUT}	Voltage output. Connect this output to the load circuit.

Connection Diagram

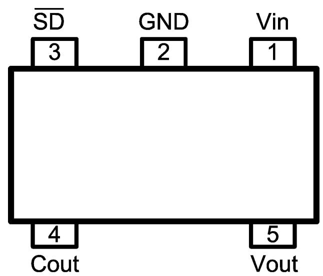

Figure 1. 5-Pin SOT-23 Package (DBV) – Top View
See Package Number DBV0005A

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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Absolute Maximum Ratings[1][2][3]

Input Voltage	-0.3 to 6.5V
Output Voltage	-0.3 to (V_{IN} + 0.3V) to 6.5V (max)
Shutdown Input Voltage	-0.3 to 6.5V
Junction Temperature	150°C
Lead Temp. [4]	260°C
Storage Temperature	-65 to 150°C
Thermal Resistance [5]	
θ_{JA}	220°C/W
Maximum Power Dissipation at 25°C	568mW
ESD [6]	
Human Body Model	2KV
Machine Model	200V

(1) All Voltages are with respect to the potential at the GND pin.
(2) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics.
(3) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(4) The package can pass MSL (moisture sensitivity level) 1 at 260°C. Additional information on lead temperature can be obtained from TI web pages: http://www.national.com/packaging/general.html and http://www.national.com/packaging/plastic.html
(5) The Maximum power dissipation of the device is dependant on the maximum allowable junction temperature for the device and the ambient temperature. This relationship is given by the formula
$P_D = (T_J - T_A)/\theta_{JA}$
Where T_J is the junction temperature, T_A is the ambient temperature, and θJA is the junction-to-ambient thermal resistance. The Maximum Power dissipation across the device related to the operational conditions can be calculated using the formula
$P_D = (V_{IN(MAX)} - V_{OUT(MAX)}) * (I_{OUT(MAX)})$.
Substituting the device values gives the max power dissipation = (5.2V - 1.5V)(0.03) = 0.111W. This figure for Maximum power dissipation can be used to derive the maximum ambient temperature. For the 5 pin SOT-23 package, θ_{JA} = 220°C/W; thus, for this device the maximum temperature difference, (T_J - T_A), is 24.4°C, (0.111 * 220). This gives the maximum ambient temperature for operation as 100.6°C, (125 - 24.4). Similarly the numbers for the absolute maximum case can be derived using a figure of 150°C for the junction temperature.
(6) The human body is 100pF discharge through 1.5kW resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Operating Conditions[1]

Input Voltage	1.9 to 5.2V
Shutdown Input Voltage	0 to 6.0V
Junction Temperature	-40°C to 125°C
Power Dissipation at 25°C	454mW

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see Electrical Characteristics.

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Electrical Characteristics

Unless otherwise noted, V_{SD} = 1.15, V_{IN} = V_{OUT} + 1.0V, C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 1 µF.
Typical values and limits appearing in normal type apply for T_J = 25°C. Limits appearing in **boldface** type apply over the full temperature range for operation, −40 to +125°C. (1)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{IN}	Input Voltage			1.9	5.2	V
ΔV_{OUT}	Output Voltage Tolerance	Over full line and load regulation.		**-90**	**+90**	mV
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 5.2V, I_{OUT} = 1mA		**-0.27**	**+0.27**	%/V
	Load Regulation Error	I_{OUT} = 1mA to 30mA	100		220	µV/mA
I_{LOAD}	Load Current	See (2) and (3)		0		µA
I_Q	Quiescent Current	V_{SD} = 1.15V, I_{OUT} = 0mA	26		**50**	µA
		V_{SD} = 1.15V, I_{OUT} = 30mA	29		**50**	
		V_{SD} = 0.4V	0.003		**1.5**	
I_{SC}	Short Circuit Current Limit	See (4)	90			mA
PSRR	Power Supply Rejection Ratio	f = 1kHz, I_{OUT} = 30mA	40			dB
		f = 20kHz, I_{OUT} = 30mA	30			
E_{EN}	Output noise Voltage (3)	BW = 10Hz to 1000kHz, V_{IN} = 4.2V	300			μV_{RMS}
$T_{SHUTDOWN}$	Thermal Shutdown Temperature		160			°C
	Thermal Shutdown Hysteresis		20			
Enable Control Characteristics						
I_{SD}	Maximum Input Current at SD Input	V_{EN} = 0.0V and V_{IN} = 5.2V	0.001			µA
V_{IL}	Low Input Threshold	V_{IN} = 1.8V to 5.2V			**0.4**	V
V_{IH}	High Input Threshold	V_{IN} = 1.8 to 5.2V		**1.15**		V
Timing Characteristics						
T_{ON1}	Turn On Time (3)	50 to 85% of $V_{OUT(NOM)}$ (5)			15	µS
T_{ON2}		To 95% Level (6)	40			
T_{OFF1}	Turn Off Time (3)	85 to 50% of $V_{OUT(NOM)}$ (7)			15	µS
T_{OFF2}		95 to 5% Level (8)	40			
Transient Response	Line Transient Response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 10µS (3)			60	mV
	Load Transient Response $\lvert\delta V_{OUT}\rvert$	T_{rise} = T_{fall} = 1µS I_{OUT} = 100µA to 5mA (3)			60	

(1) All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at T_J = 25°C or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The device maintains the regulated output voltage without the load.
(3) This electrical specification is guaranteed by design.
(4) Short circuit current is measured on the input supply line at the point when the short circuit condition reduces the output voltage to 95% of its nominal value.
(5) Time for V_{OUT} to rise from 50 to 85% of $V_{OUT(nom)}$. (Figure 2)
(6) Time from V_{SD} = 1.15V to V_{OUT} = 95%($V_{OUT(nom)}$). (Figure 2)
(7) Time for V_{OUT} to fall from 85 to 50% of $V_{OUT(nom)}$. (Figure 2)
(8) Time from V_{SD} = 0.4V to V_{OUT} = 5%($V_{OUT(nom)}$. (Figure 2)

Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
C_o	Output Capacitor	Capacitance (1)		1.0		µF
		ESR		5	500	mΩ

(1) Capacitor types recommended are X7R, Y5V, and Z5U. X7R tolerance is quoted as 15% over temperature.

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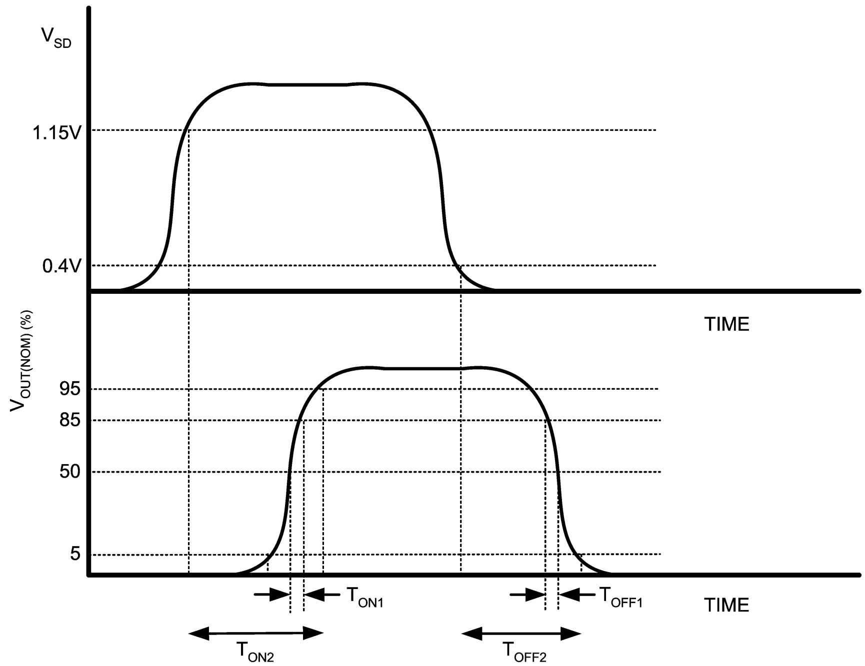

Figure 2. T_{on}/T_{off} Timing Diagram

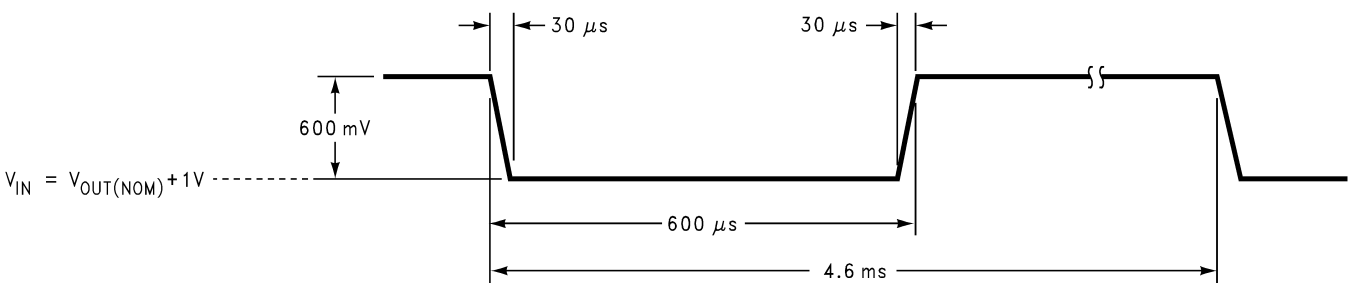

Figure 3. Line Transient Input Test Signal

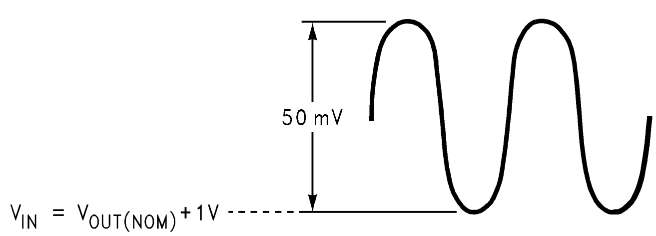

Figure 4. PSRR Input Test Signal

Typical Performance Characteristics

Unless otherwise specified, C_{IN} = C_{OUT} = 1.0 µF Ceramic, V_{IN} = 2.8V, T_A = 25°C, Shutdown pin is tied to V_{IN}.

Output Voltage Change vs Temperature

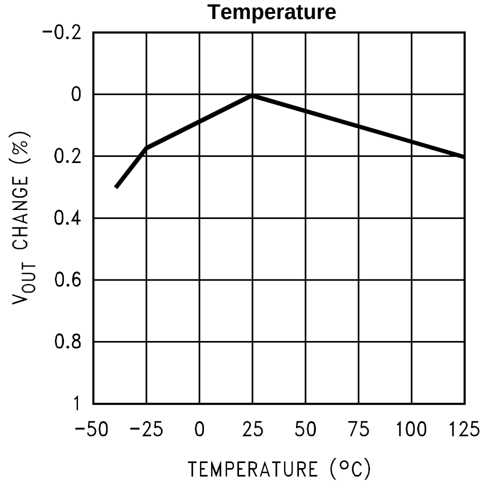

Figure 5.

Ground Current vs Load Current

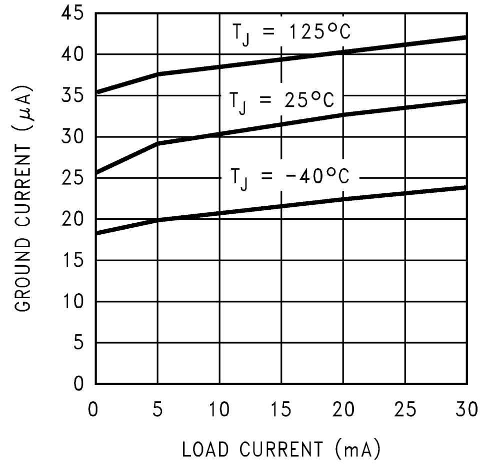

Figure 6.

Ground Current vs V_{IN} at 25°C

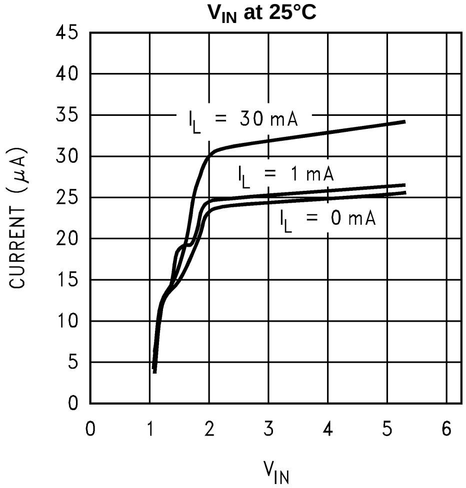

Figure 7.

Ground Current vs V_{IN} at 125°C

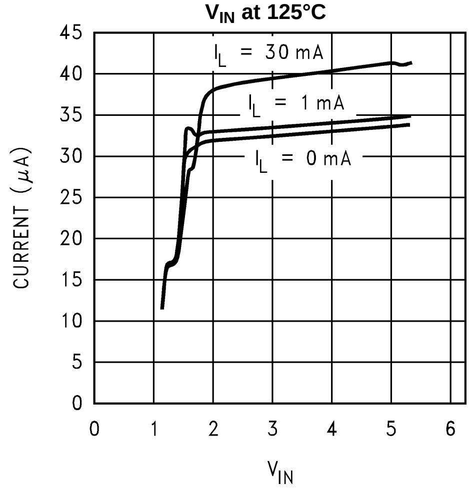

Figure 8.

Short Circuit Current

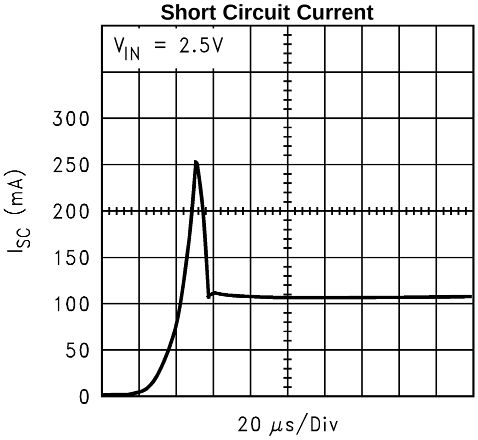

Figure 9.

Short Circuit Current

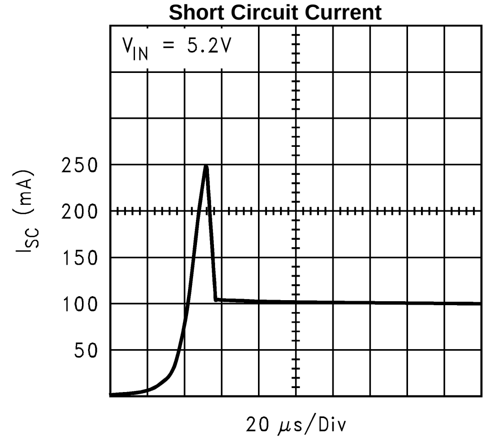

Figure 10.

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Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = C_{OUT} = 1.0 µF Ceramic, V_{IN} = 2.8V, T_A = 25°C, Shutdown pin is tied to V_{IN}.

Line Transient Response

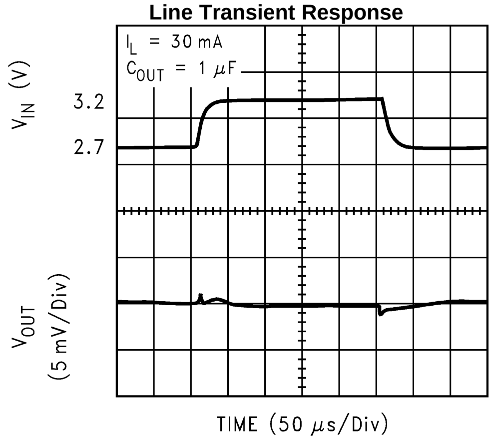

Figure 11.

Line Transient Response

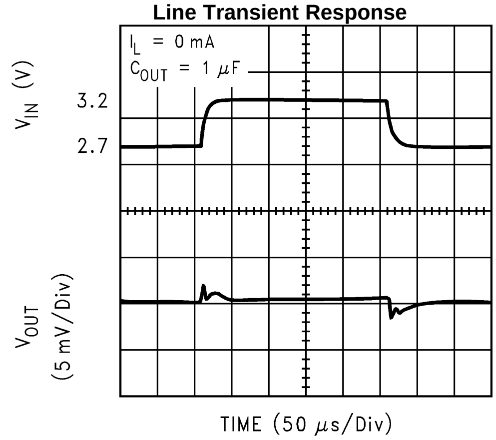

Figure 12.

Turn ON/OFF Timing

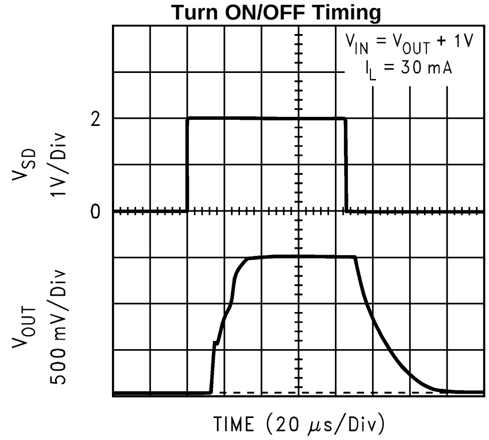

Figure 13.

Turn ON/OFF Timing

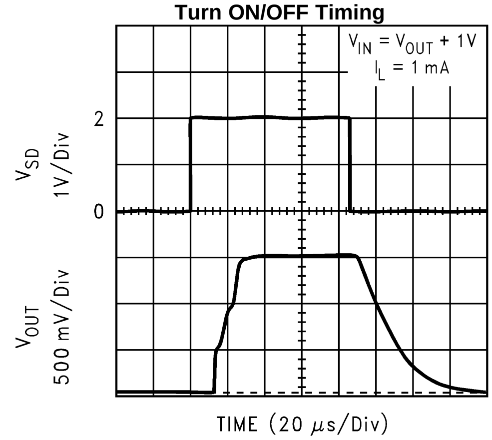

Figure 14.

Ripple Rejection

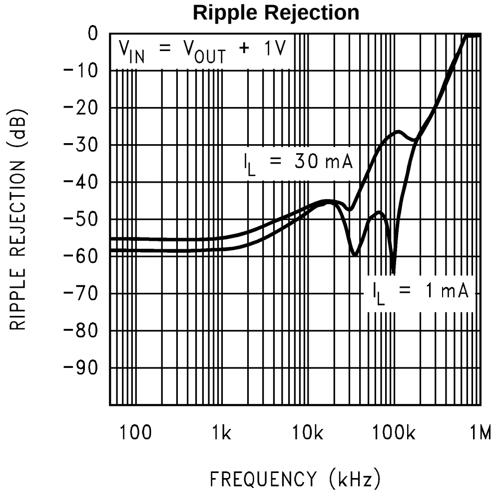

Figure 15.

Load Transient Response

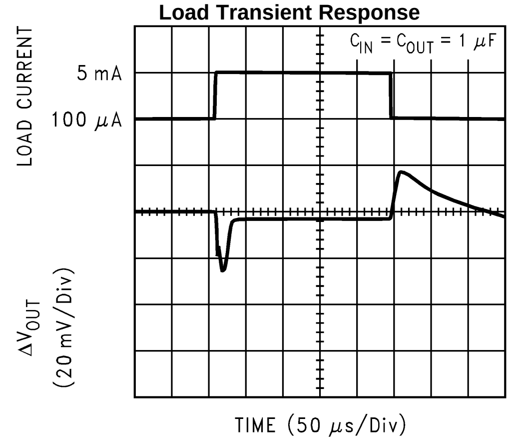

Figure 16.

Typical Performance Characteristics (continued)

Unless otherwise specified, $C_{IN} = C_{OUT}$ = 1.0 µF Ceramic, V_{IN} = 2.8V, T_A = 25°C, Shutdown pin is tied to V_{IN}.

Load Transient Response

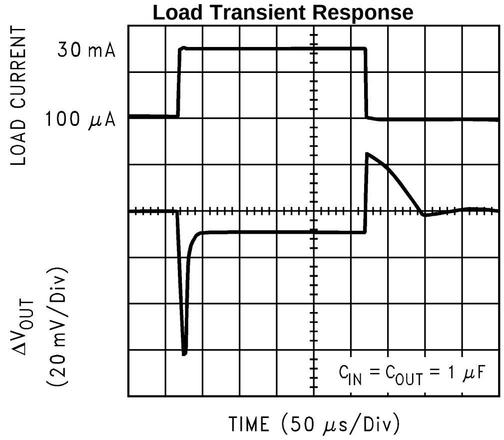

Figure 17.

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APPLICATION HINTS

EXTERNAL CAPACITORS

In common with most regulators, the LP3992 requires external capacitors for regulator stability. The LP3992 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

INPUT CAPACITOR

An input capacitor is required for stability. It is recommended that a 1.0µF capacitor be connected between the LP3992 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain ≅ 1.0µF over the entire operating temperature range.

OUTPUT CAPACITOR

The LP3992 is designed specifically to work with very small ceramic output capacitors. A 1.0µF ceramic capacitor (dielectric types Z5U, Y5V or X7R) with ESR between 5mΩ to 500mΩ, is suitable in the LP3992 application circuit.

For this device the output capacitor should be connected between the C_{OUT} pin and ground. It is also possible to connect the output capacitor directly to the V_{OUT} pin. In this case C_{OUT} should be left open-circuit or tied directly to V_{OUT}.

It may also be possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see CAPACITOR CHARACTERISTICS).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5mΩ to 500mΩ for stability.

NO-LOAD STABILITY

The LP3992 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

CAPACITOR CHARACTERISTICS

The LP3992 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 1µF to 4.7µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1µF ceramic capacitor is in the range of 20mΩ to 40mΩ, which easily meets the ESR requirement for stability for the LP3992.

The temperature performance of ceramic capacitors varies by type. Most large value ceramic capacitors (≥ 2.2µF) are manufactured with Z5U or Y5V temperature characteristics, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

A better choice for temperature coefficient in a ceramic capacitor is X7R. This type of capacitor is the most stable and holds the capacitance within ±15% over the temperature range.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

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Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

SHUTDOWN AND ENABLE

The LP3992 features an active low shutdown pin, V_{SD}, which turns the device off when pulled low. The device output is enabled when the shutdown pin is pulled high. In the shutdown mode the regulator output is off and the device typically consumes 3nA.

If the application does not require the shutdown feature, the V_{SD} pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the V_{SD} input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics under V_{IL} and V_{IH}.

FAST TURN ON AND OFF

The controlled shutdown feature of the device provides a fast turn off by discharging the output capacitor via an internal FET device. This discharge is current limited by the RDS_{ON} of this switch. Fast turn-on is guaranteed by control circuitry within the reference block allowing a very fast ramp of the output voltage to reach the target voltage.

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REVISION HISTORY

Changes from Revision A (February 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	10

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3992IMFX-1.5/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LFHB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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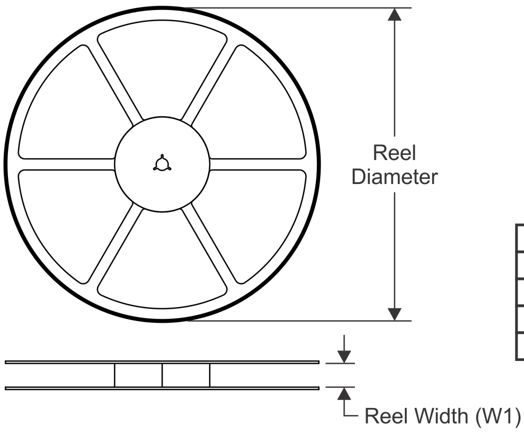
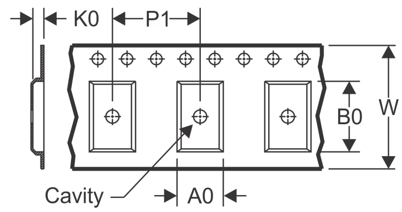
TAPE AND REEL INFORMATION

REEL DIMENSIONS

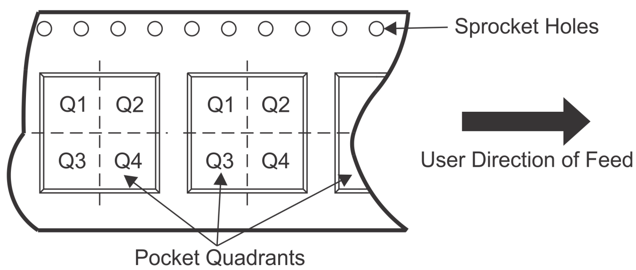


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

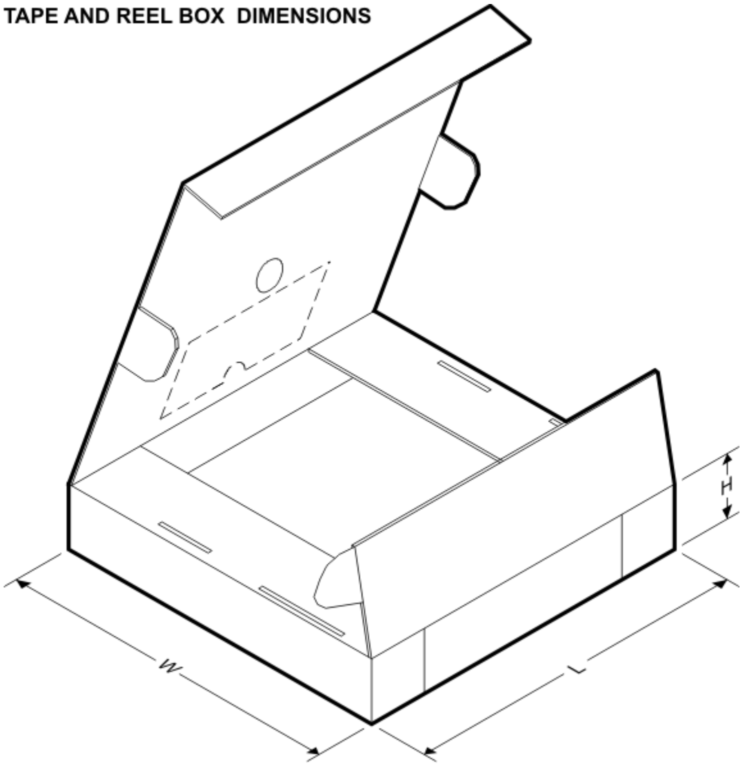
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3992IMFX-1.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

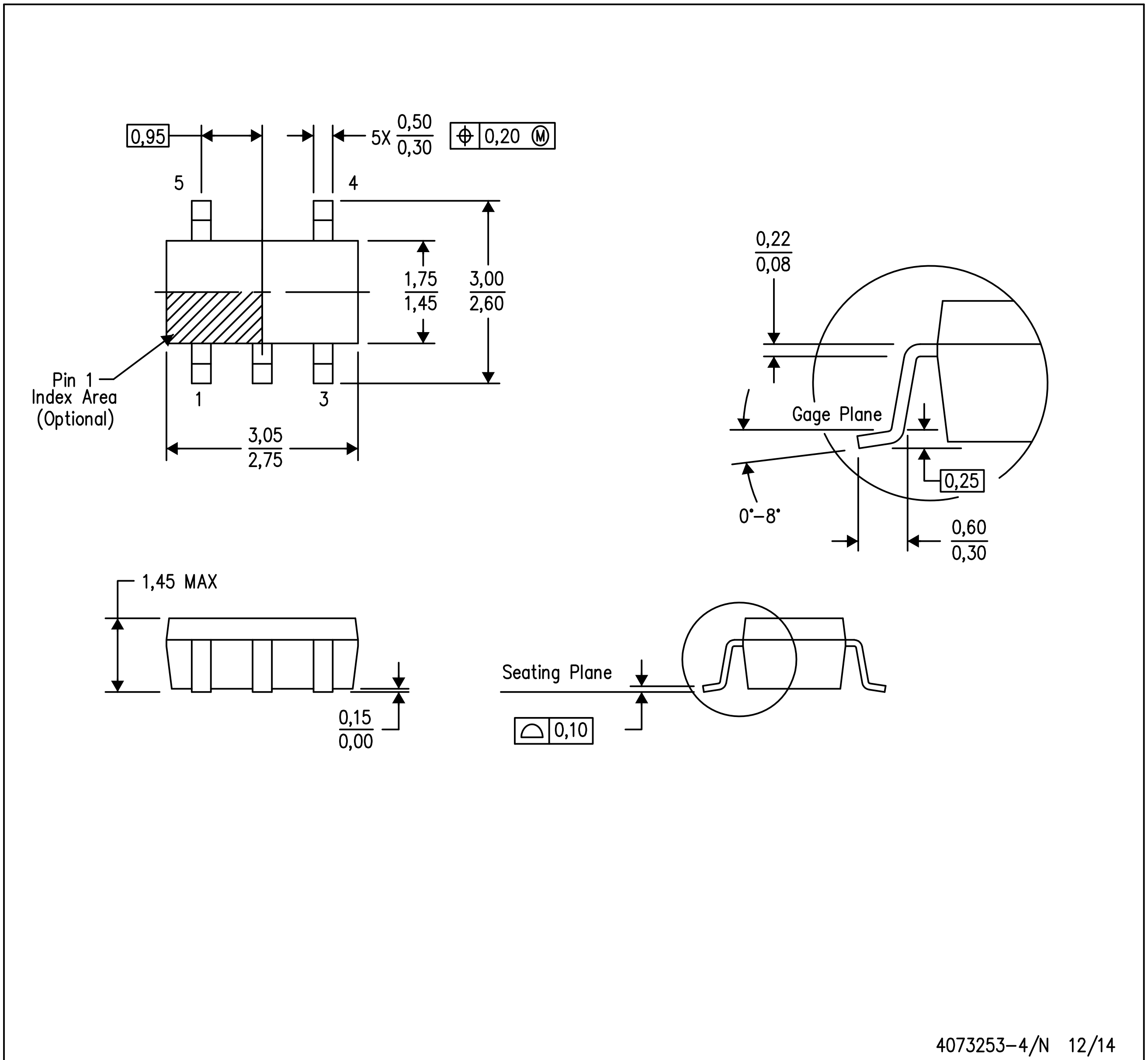
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

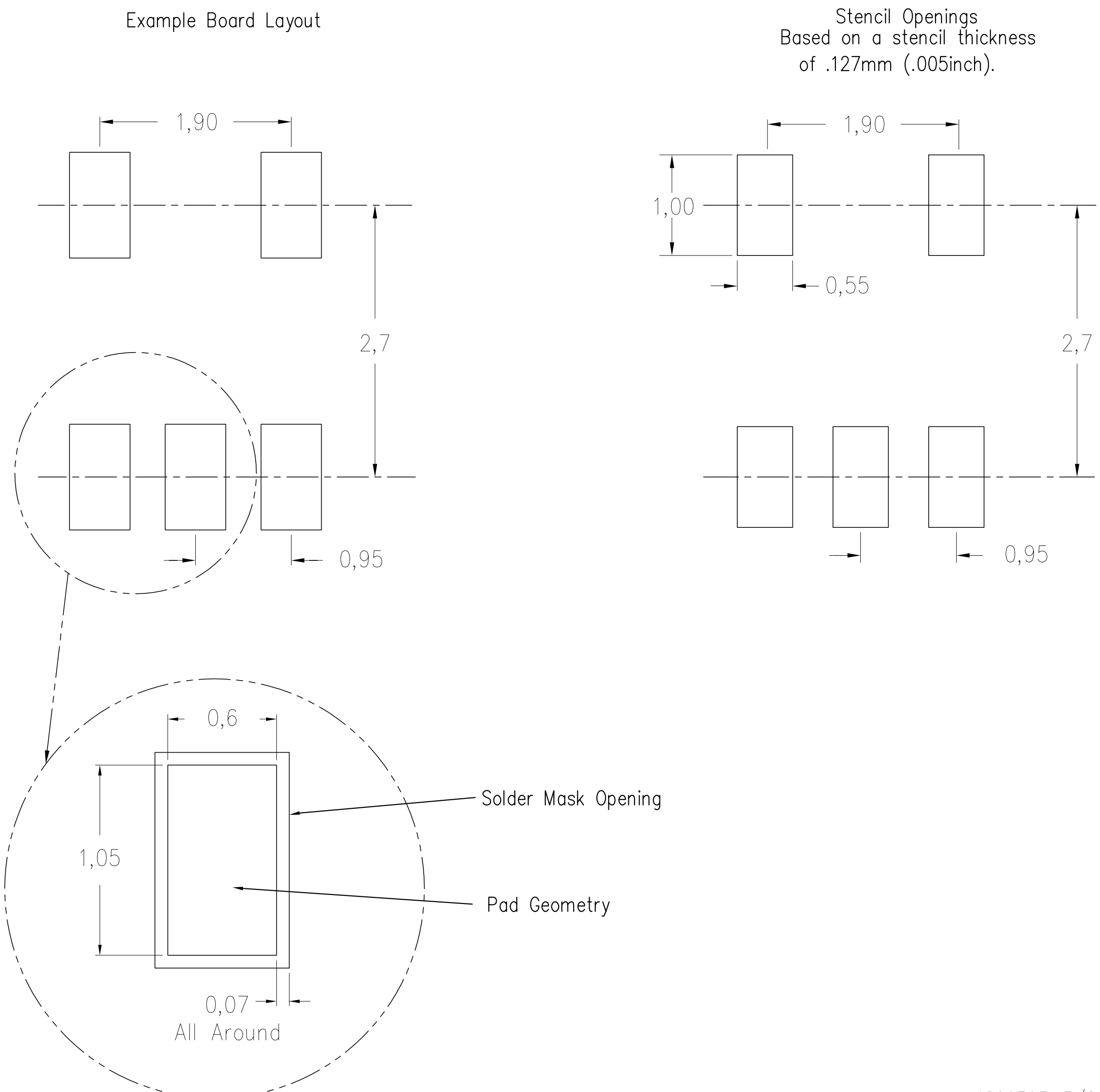
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3992IMFX-1.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

DBV (R-PDSO-G5) PLASTIC SMALL OUTLINE



4209593-3/C 08/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

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