

LMC660

CMOS Quad Operational Amplifier

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It operates from +5V to +15.5V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS} , drift, and broadband noise as well as voltage gain into realistic loads (2 k Ω and 600 Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

Features

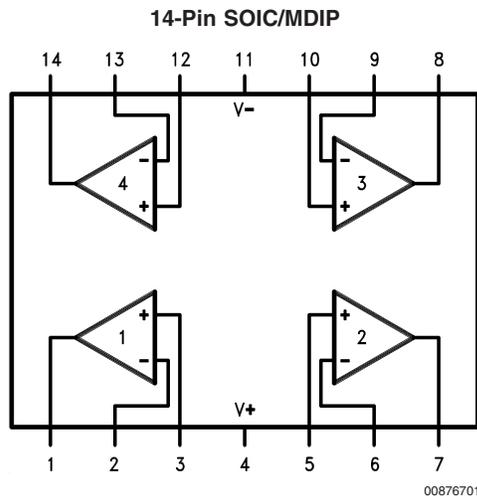
- Rail-to-rail output swing
- Specified for 2 k Ω and 600 Ω loads
- High voltage gain: 126 dB

- Low input offset voltage: 3 mV
- Low offset voltage drift: 1.3 $\mu\text{V}/^\circ\text{C}$
- Ultra low input bias current: 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15.5V supply
- $I_{SS} = 375 \mu\text{A}/\text{amplifier}$; independent of V^+
- Low distortion: 0.01% at 10 kHz
- Slew rate: 1.1 V/ μs

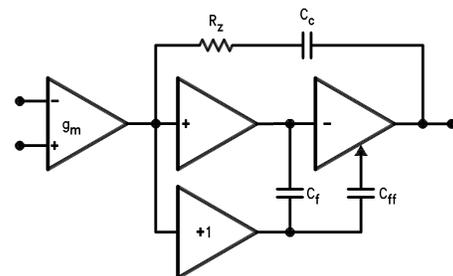
Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-Hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram



LMC660 Circuit Topology (Each Amplifier)



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Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage	16V
Output Short Circuit to V ⁺	(Note 11)
Output Short Circuit to V ⁻	(Note 1)
Lead Temperature (Soldering, 10 sec.)	260°C
Storage Temp. Range	-65°C to +150°C
Voltage at Input/Output Pins	(V ⁺) + 0.3V, (V ⁻) - 0.3V
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA

Power Dissipation	(Note 2)
Junction Temperature	150°C
ESD tolerance (Note 8)	1000V

Operating Ratings

Temperature Range	
LMC660AI	-40°C ≤ T _J ≤ +85°C
LMC660C	0°C ≤ T _J ≤ +70°C
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ _{JA}) (Note 10)	
14-Pin SOIC	115°C/W
14-Pin MDIP	85°C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V⁺ = 5V, V⁻ = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1MΩ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3 3.3	6 6.3	mV max
Input Offset Voltage Average Drift		1.3			μV/°C
Input Bias Current		0.002	4	2	pA max
Input Offset Current		0.001	2	1	pA max
Input Resistance		>1			TeraΩ
Common Mode Rejection Ratio	0V ≤ V _{CM} ≤ 12.0V V ⁺ = 15V	83	70 68	63 62	dB min
Positive Power Supply Rejection Ratio	5V ≤ V ⁺ ≤ 15V V _O = 2.5V	83	70 68	63 62	dB min
Negative Power Supply Rejection Ratio	0V ≤ V ⁻ ≤ -10V	94	84 83	74 73	dB min
Input Common-Mode Voltage Range	V ⁺ = 5V & 15V For CMRR ≥ 50 dB	-0.4	-0.1 0	-0.1 0	V max
		V ⁺ - 1.9	V ⁺ - 2.3 V⁺ - 2.5	V ⁺ - 2.3 V⁺ - 2.4	V min
Large Signal Voltage Gain	R _L = 2 kΩ (Note 5) Sourcing	2000	440 400	300 200	V/mV min
		500	180 120	90 80	V/mV min
	R _L = 600Ω (Note 5) Sourcing	1000	220 200	150 100	V/mV min
		250	100 60	50 40	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}\Omega$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units	
			Limit (Note 4)	Limit (Note 4)		
Output Swing	$V^+ = 5\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	4.87	4.82 4.79	4.78 4.76	V min	
		0.10	0.15 0.17	0.19 0.21	V max	
	$V^+ = 5\text{V}$ $R_L = 600\Omega$ to $V^+/2$	4.61	4.41 4.31	4.27 4.21	V min	
		0.30	0.50 0.56	0.63 0.69	V max	
	$V^+ = 15\text{V}$ $R_L = 2\text{ k}\Omega$ to $V^+/2$	14.63	14.50 14.44	14.37 14.32	V min	
		0.26	0.35 0.40	0.44 0.48	V max	
	$V^+ = 15\text{V}$ $R_L = 600\Omega$ to $V^+/2$	13.90	13.35 13.15	12.92 12.76	V min	
		0.79	1.16 1.32	1.45 1.58	V max	
	Output Current $V^+ = 5\text{V}$	Sourcing, $V_O = 0\text{V}$	22	16 14	13 11	mA min
		Sinking, $V_O = 5\text{V}$	21	16 14	13 11	mA min
Output Current $V^+ = 15\text{V}$	Sourcing, $V_O = 0\text{V}$	40	28 25	23 21	mA min	
	Sinking, $V_O = 13\text{V}$ (Note 11)	39	28 24	23 20	mA min	
Supply Current	All Four Amplifiers $V_O = 1.5\text{V}$	1.5	2.2 2.6	2.7 2.9	mA max	

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{\text{CM}} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}\Omega$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Slew Rate	(Note 6)	1.1	0.8 0.6	0.8 0.7	V/ μs min
Gain-Bandwidth Product		1.4			MHz
Phase Margin		50			Deg
Gain Margin		17			dB
Amp-to-Amp Isolation	(Note 7)	130			dB
Input Referred Voltage Noise	$F = 1\text{ kHz}$	22			$\text{nV}/\sqrt{\text{Hz}}$
Input Referred Current Noise	$f = 1\text{ kHz}$	0.0002			$\text{pA}/\sqrt{\text{Hz}}$

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ\text{C}$. **Boldface** limits apply at the temperature extremes. $V^+ = 5\text{V}$, $V^- = 0\text{V}$, $V_{CM} = 1.5\text{V}$, $V_O = 2.5\text{V}$ and $R_L > 1\text{M}\Omega$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Total Harmonic Distortion	$f = 10\text{ kHz}$, $A_V = -10$ $R_L = 2\text{ k}\Omega$, $V_O = 8\text{ V}_{PP}$ $V^+ = 15\text{V}$	0.01			%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150°C . Output currents in excess of $\pm 30\text{ mA}$ over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} , and T_A . The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15\text{V}$, $V_{CM} = 7.5\text{V}$ and R_L connected to 7.5V . For Sourcing tests, $7.5\text{V} \leq V_O \leq 11.5\text{V}$. For Sinking tests, $2.5\text{V} \leq V_O \leq 7.5\text{V}$.

Note 6: $V^+ = 15\text{V}$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15\text{V}$ and $R_L = 10\text{ k}\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\text{ V}_{PP}$.

Note 8: Human Body Model is $1.5\text{ k}\Omega$ in series with 100 pF .

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

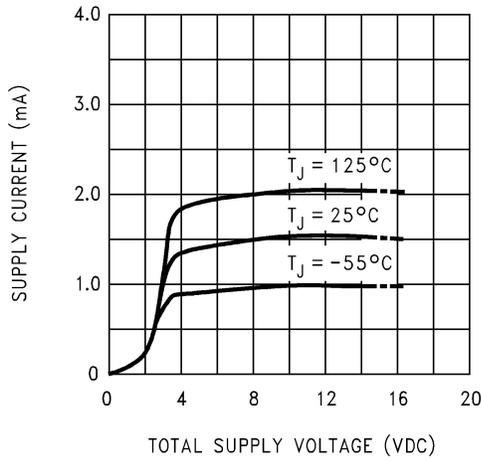
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial -40°C to $+85^\circ\text{C}$	Commercial 0°C to $+70^\circ\text{C}$		
14-Pin SOIC	LMC660AIM	LMC660CM	Rail	M14A
	LMC660AIMX	LMC660CMX	Tape and Reel	
14-Pin M DIP	LMC660AIN	LMC660CN	Rail	N14A

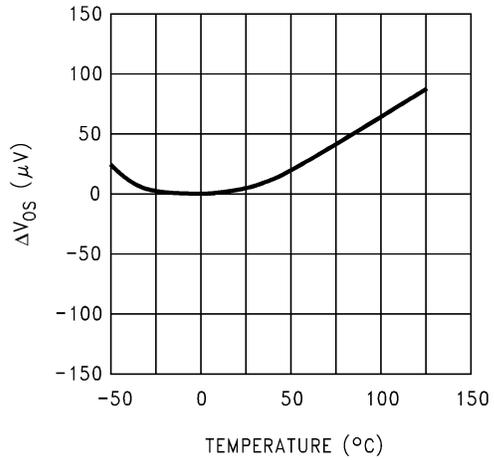
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified.

Supply Current vs. Supply Voltage



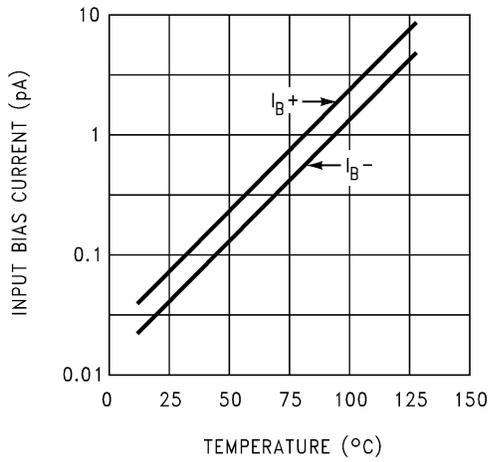
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Offset Voltage



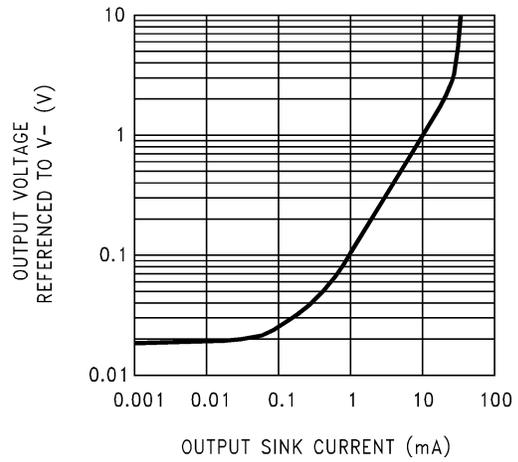
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Input Bias Current



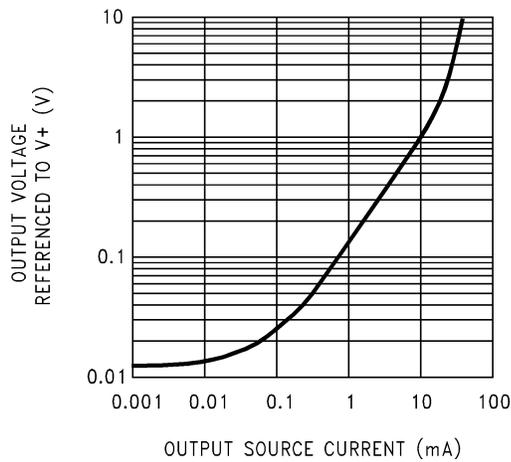
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Output Characteristics Current Sinking



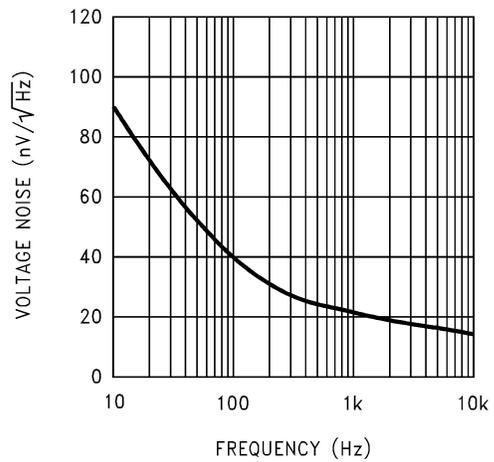
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Output Characteristics Current Sourcing



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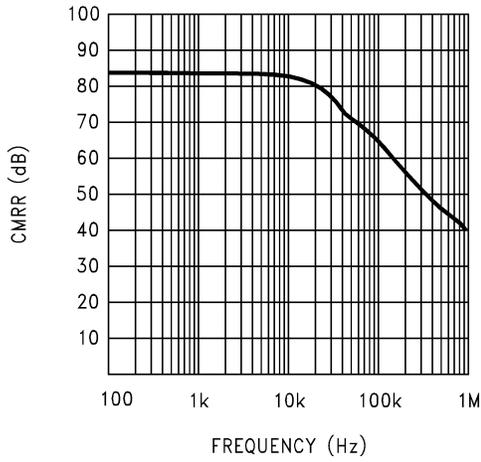
Input Voltage Noise vs. Frequency



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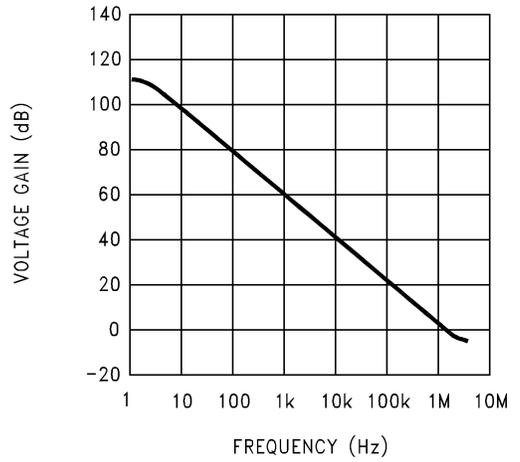
Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^\circ C$ unless otherwise specified. (Continued)

CMRR vs. Frequency



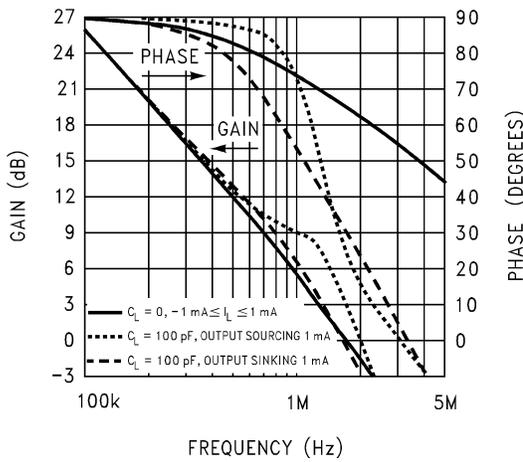
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Open-Loop Frequency Response



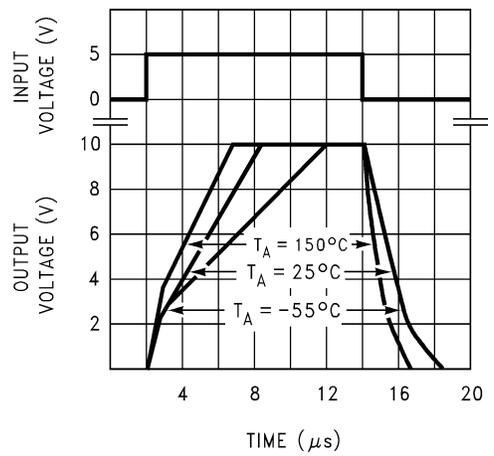
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Frequency Response vs. Capacitive Load



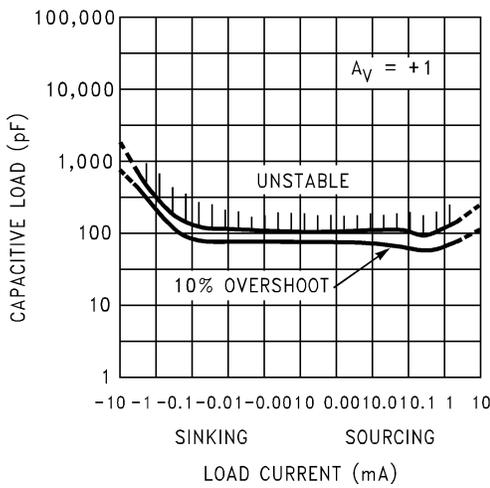
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Non-Inverting Large Signal Pulse Response



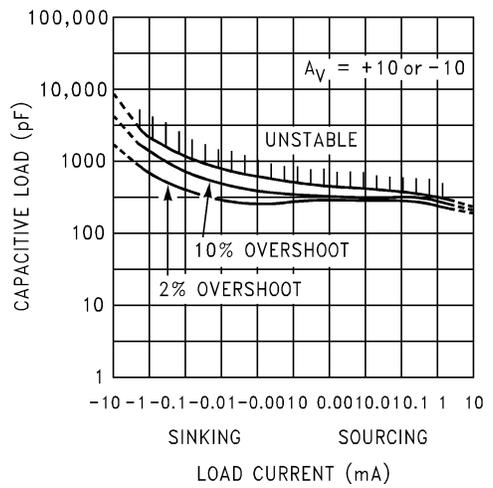
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Stability vs. Capacitive Load



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Stability vs. Capacitive Load

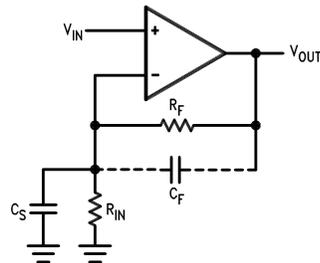


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Application Hints (Continued)

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$



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C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

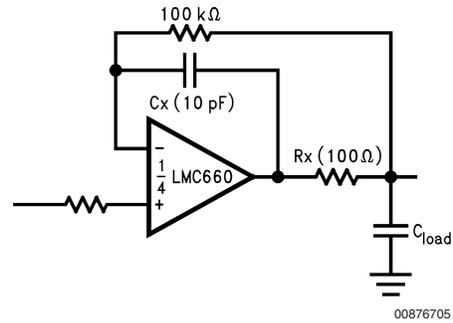
FIGURE 2. General Operational Amplifier Circuit

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

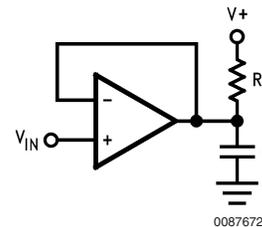
The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3*, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.



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FIGURE 3. R_x , C_x Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 4*). Typically a pull up resistor conducting $500 \mu\text{A}$ or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).



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FIGURE 4. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See *Figure 5*. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would

Application Hints (Continued)

cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figure 6a*, *Figure 6b*, *Figure 6c* for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 6d*.

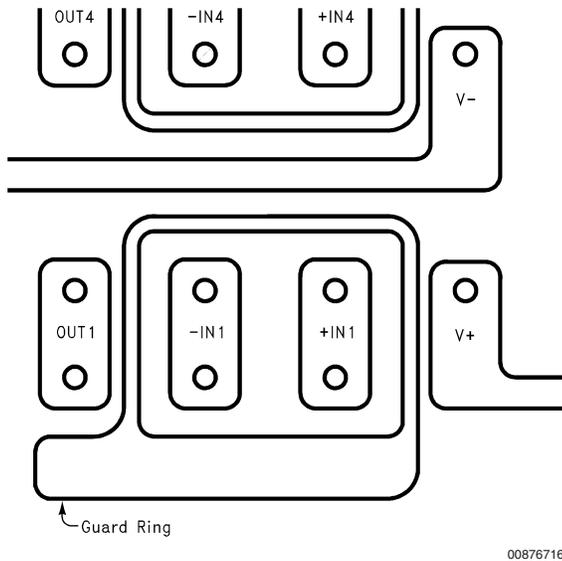
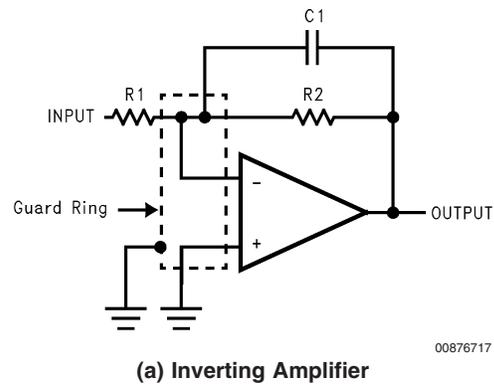
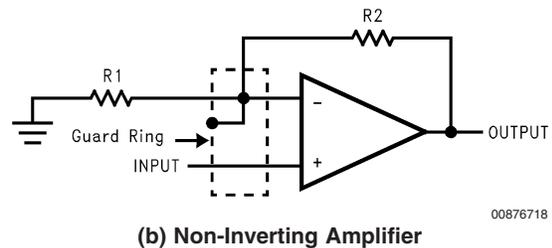


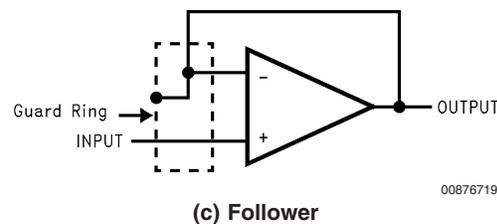
FIGURE 5. Example, using the LMC660, of Guard Ring in P.C. Board Layout



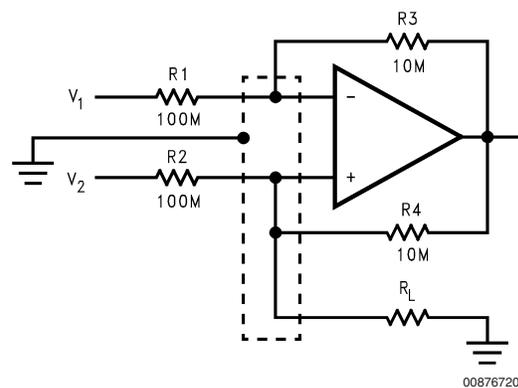
(a) Inverting Amplifier



(b) Non-Inverting Amplifier



(c) Follower

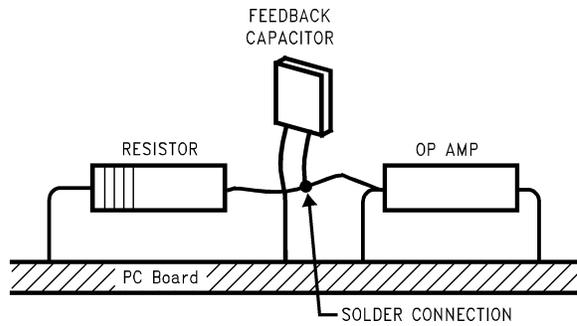


(d) Howland Current Pump

FIGURE 6. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 7*.

Application Hints (Continued)



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 7. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_{b^{-}} = \frac{dV_{OUT}}{dt} \times C2.$$

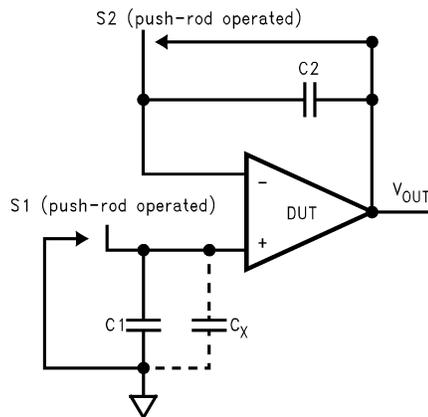


FIGURE 8. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of $I_{b^{-}}$, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I_{b^{+}} = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

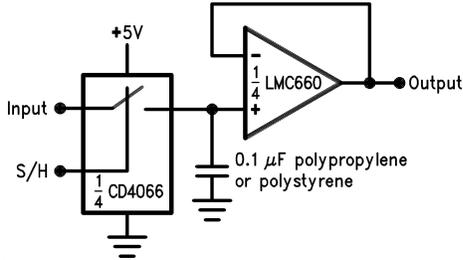
where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications

(V+ = 5.0 VDC)

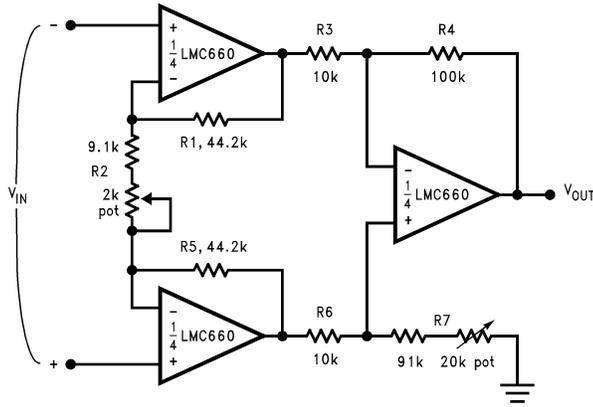
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC660 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC660 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold



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Instrumentation Amplifier



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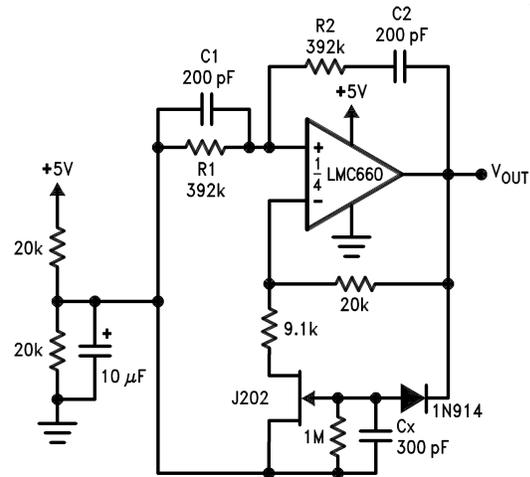
If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

∴ Av ≈ 100 for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



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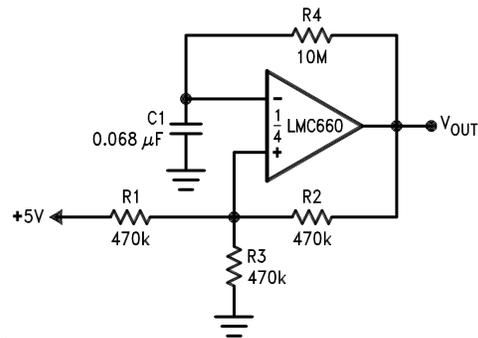
Oscillator frequency is determined by R1, R2, C1, and C2:

$$f_{osc} = 1/2\pi RC, \text{ where } R = R1 = R2 \text{ and}$$

$$C = C1 = C2.$$

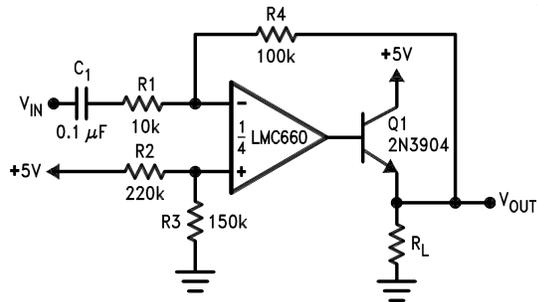
This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator



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Power Amplifier

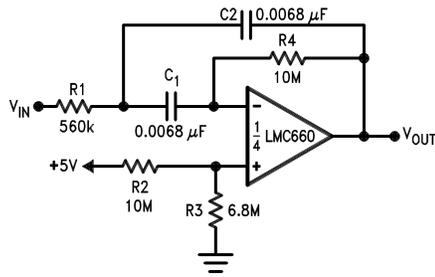


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Typical Single-Supply Applications

($V^+ = 5.0$ VDC) (Continued)

10 Hz Bandpass Filter



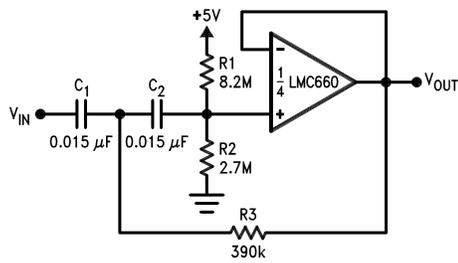
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$f_0 = 10$ Hz

$Q = 2.1$

Gain = -8.8

10 Hz High-Pass Filter



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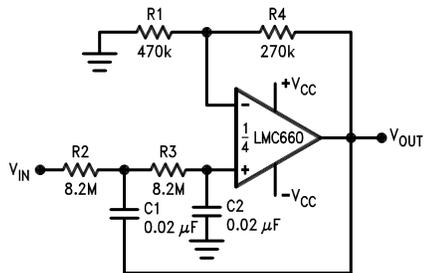
$f_c = 10$ Hz

$d = 0.895$

Gain = 1

2 dB passband ripple

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



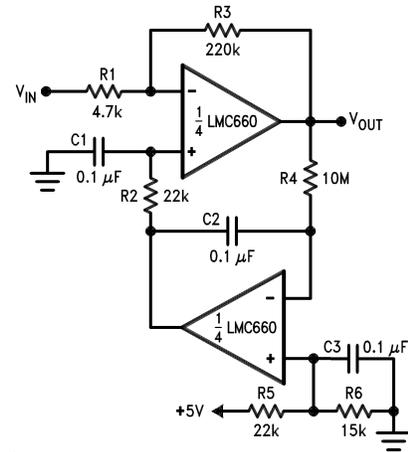
00876714

$f_c = 1$ Hz

$d = 1.414$

Gain = 1.57

High Gain Amplifier with Offset Voltage Reduction

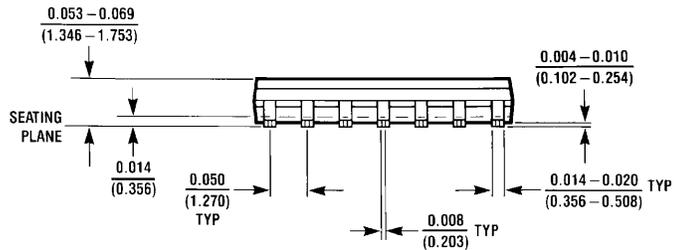
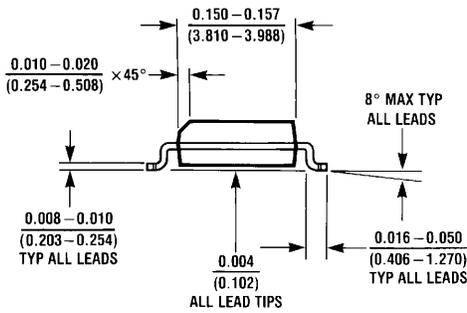
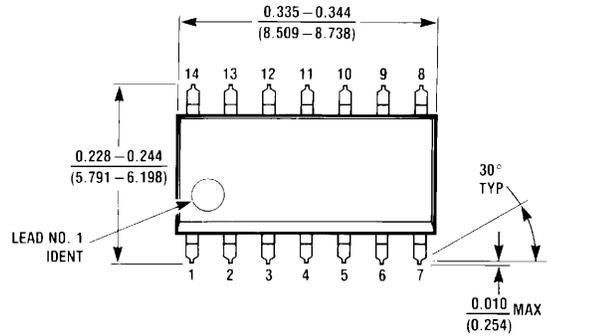


00876715

Gain = -46.8

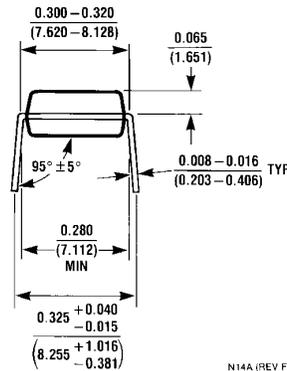
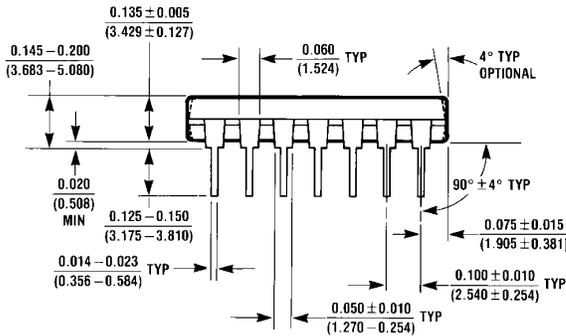
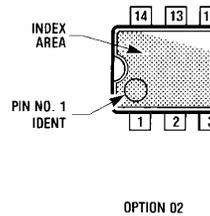
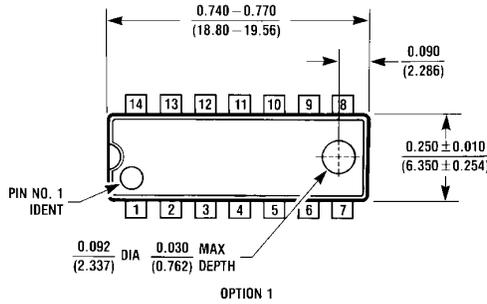
Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

Physical Dimensions inches (millimeters) unless otherwise noted



M14A (REV H)

14-Pin SOIC
NS Package Number M14A



N14A (REV F)

14-Pin MDIP
NS Package Number N14A

Notes

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

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- | | |
|--|---|
| <p>1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.</p> | <p>2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.</p> |
|--|---|

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