



LM158-LM258-LM358 LM158A-LM258A-LM358A

Low power dual operational amplifiers

Features

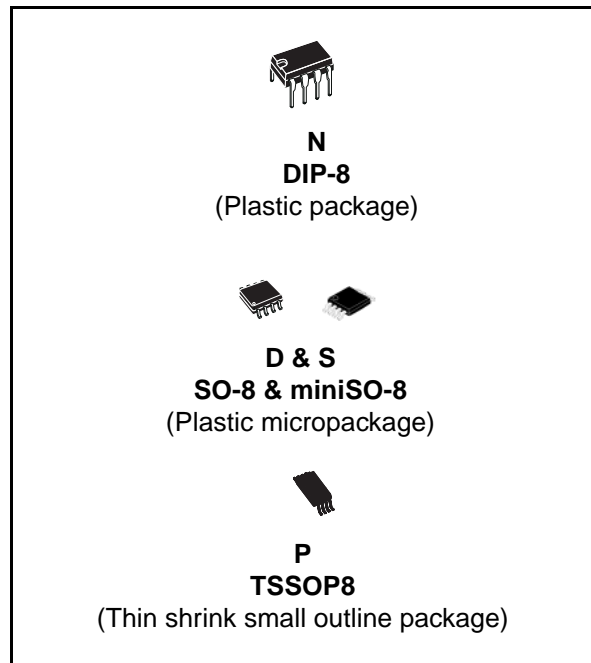
- Internally frequency compensated
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current/op (500 μ A) essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset voltage: 2 mV
- Low input offset current: 2 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to ($V_{CC} - 1.5$ V)

Description

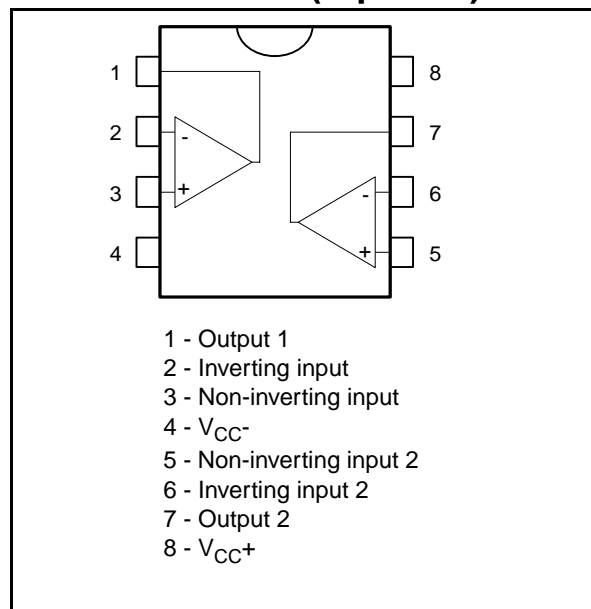
These circuits consist of two independent, high-gain, internally frequency-compensated op-amps which are designed specifically to operate from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op-amp circuits which now can be more easily implemented in single power supply systems. For example, these circuits can be directly supplied with the standard +5 V which is used in logic systems and will easily provide the required interface electronics without requiring any additional power supply.

In linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage.



Pin connections (top view)

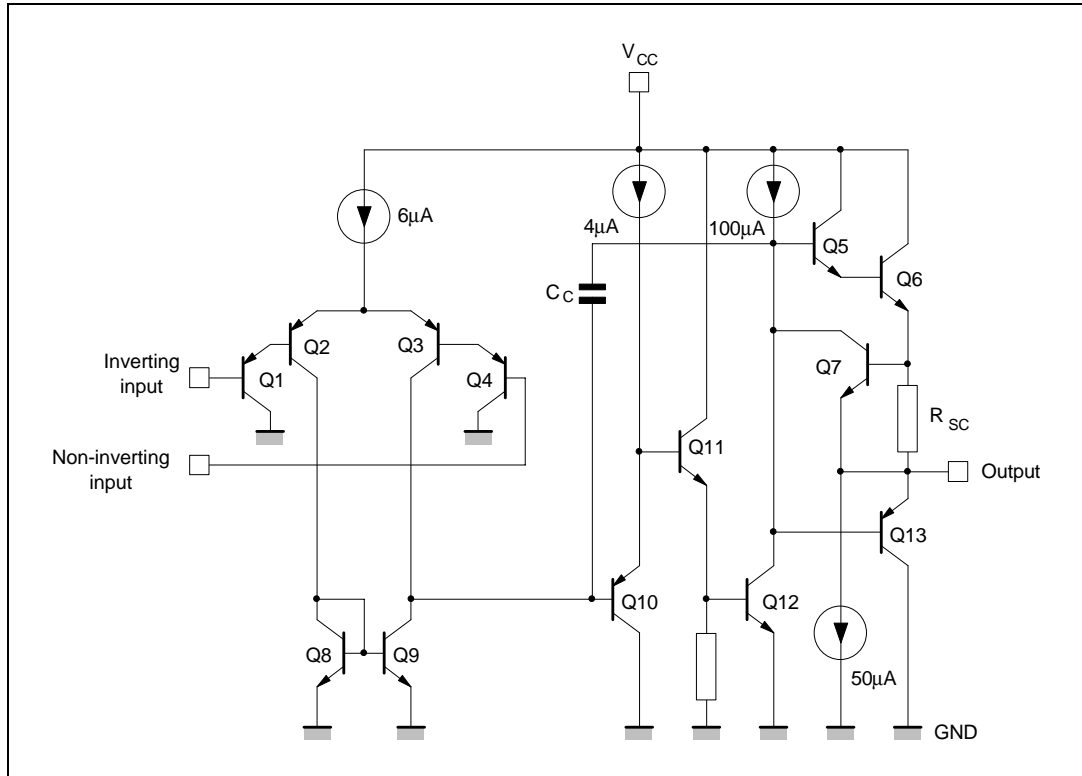


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1 Schematic diagram

Figure 1. Schematic diagram (1/2 LM158)



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	LM158,A	LM258,A	LM358,A	Unit
V_{CC}	Supply voltage	+/-16 or 32			V
V_i	Input voltage	32			V
V_{id}	Differential input voltage	32			V
P_{tot}	Power dissipation ⁽¹⁾	500			mW
	Output short-circuit duation ⁽²⁾	Infinite			
I_{in}	Input current ⁽³⁾	50			mA
T_{oper}	Operating free-air temperature range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150			°C
T_j	Maximum junction temperature	150			°C
R_{thja}	Thermal resistance junction to ambient ^{(4) (5)}				°C/W
	SO-8	125			
	MiniSO-8	190			
	TSSOP8	120			
	DIP-8	85			
R_{thjc}	Thermal resistance junction to case				°C/W
	SO-8	40			
	MiniSO-8	39			
	TSSOP8	37			
	DIP-8	41			
ESD	HBM: human body model ⁽⁶⁾	300			V
	MM: machine model ⁽⁷⁾	200			V
	CDM: charged device model	1.5			kV

1. Power dissipation must be considered to ensure that the maximum junction temperature (T_j) is not exceeded.
2. Short-circuits from the output to V_{CC} can cause excessive heating if $V_{CC} > 15$ V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC} . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the Op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model, 100 pF discharged through a 1.5 kΩ resistor into pin of device.
7. Machine model ESD, a 200 pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5 Ω), into pin-to-pin of device.

3 Electrical characteristics

Table 2. Electrical characteristics for $V_{CC^+} = +5V$, $V_{CC^-} = \text{Ground}$, $V_O = 1.4V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input offset voltage ⁽¹⁾ $T_{amb} = +25^\circ C$ LM158, LM258 LM158A		1	3		2	7 5	mV
	$T_{min} \leq T_{amb} \leq T_{max}$ LM158, LM258			4			9 7	
I_{io}	Input offset current $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		2	10 30		2	30 40	nA
I_{ib}	Input bias current ⁽²⁾ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		20	50 100		20	150 200	nA
A_{vd}	Large signal voltage gain $V_{CC} = +15 V$, $R_L = 2 k\Omega$, $V_O = 1.4 V$ to $11.4 V$ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	50 25	100		50 25	100		V/mV
SVR	Supply voltage rejection ratio ($R_s \leq 10 k\Omega$) $V_{CC^+} = 5 V$ to $30 V$ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	65 65	100		65 65	100		dB
I_{CC}	Supply current, all Amp, no load $T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC} = +5 V$ $T_{min} \leq T_{amb} \leq T_{max}$ $V_{CC} = +30 V$		0.7	1.2 2		0.7	1.2 2	mA
V_{icm}	Input common mode voltage range $V_{CC} = +30 V$ ⁽³⁾ $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	V
CMR	Common mode rejection ratio ($R_s \leq 10 k\Omega$) $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	70 60	85		70 60	85		dB
I_{source}	Output current source $V_{CC} = +15 V$, $V_O = +2 V$, $V_{id} = +1 V$	20	40	60	20	40	60	mA
I_{sink}	Output sink current ($V_{id} = -1V$) $V_{CC} = +15V$, $V_O = +2V$	10	20		10	20		mA
	$V_{CC} = +15V$, $V_O = +0.2V$	12	50		12	50		μA

Table 2. Electrical characteristics for $V_{CC^+} = +5V$, $V_{CC^-} = \text{Ground}$, $V_o = 1.4V$, $T_{amb} = +25^\circ C$ (unless otherwise specified)

Symbol	Parameter	LM158A-LM258A LM358A			LM158-LM258 LM358			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OPP}	Output voltage swing ($R_L = 2\text{ k}\Omega$) $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	0 0		$V_{CC^+} - 1.5$ $V_{CC^+} - 2$	
V_{OH}	High level output voltage ($V_{CC^+} = 30\text{ V}$) $T_{amb} = +25^\circ C$, $R_L = 2\text{ k}\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $T_{amb} = +25^\circ C$, $R_L = 10\text{ k}\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	26 26 27 27	27 28 		26 26 27 27	27 28 		V
V_{OL}	Low level output voltage ($R_L = 10\text{ k}\Omega$) $T_{amb} = +25^\circ C$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20		5	20 20	mV
SR	Slew rate $V_{CC} = 15V$, $V_i = 0.5\text{ to }3V$, $R_L = 2\text{ k}\Omega$ $C_L = 100\text{ pF}$, unity Gain	0.3	0.6		0.3	0.6		V/ μs
GBP	Gain bandwidth product $V_{CC} = 30\text{ V}$, $f = 100\text{ kHz}$, $V_{in} = 10\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$	0.7	1.1		0.7	1.1		MHz
THD	Total harmonic distortion $f = 1\text{ kHz}$, $A_v = 20\text{ dB}$, $R_L = 2\text{ k}\Omega$, $V_o = 2\text{ V}_{pp}$, $C_L = 100\text{ pF}$, $V_o = 2\text{ V}_{pp}$		0.02			0.02		%
e_n	Equivalent input noise voltage $f = 1\text{ kHz}$, $R_s = 100\ \Omega$, $V_{CC} = 30\text{ V}$		55			55		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	15		7	30	$\mu V/^\circ C$
DI_{io}	Input offset current drift		10	200		10	300	$pA/^\circ C$
V_{o1}/V_{o2}	Channel separation ⁽⁴⁾ $1\text{ kHz} \leq f \leq 20\text{ kHz}$		120			120		dB

- $V_o = 1.4\text{ V}$, $R_s = 0\ \Omega$, $5\text{ V} < V_{CC^+} < 30\text{ V}$, $0 < V_{ic} < V_{CC^+} - 1.5\text{ V}$
- The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.
- The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is $V_{CC^+} - 1.5\text{ V}$, but either or both inputs can go to +32 V without damage.
- Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

Figure 2. Open loop frequency response

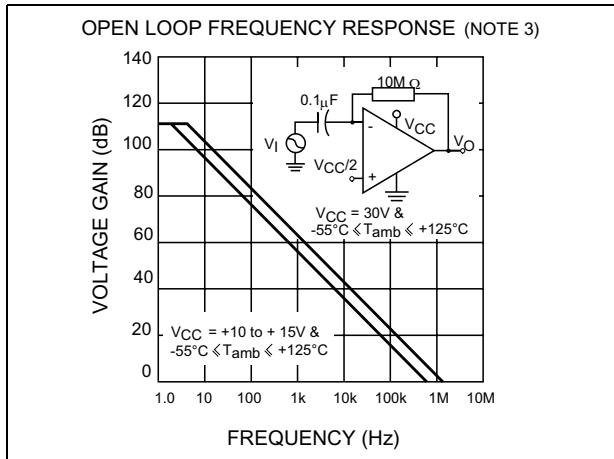


Figure 3. Large signal frequency response

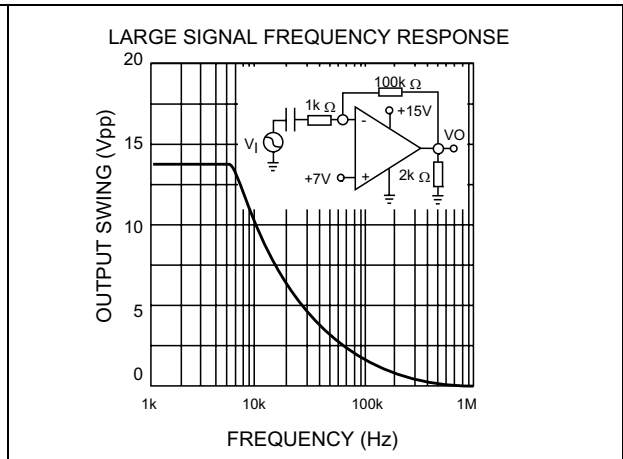


Figure 4. Voltage follower pulse response

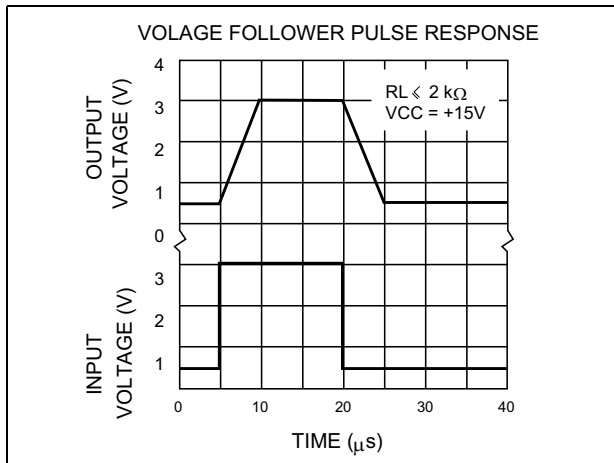


Figure 5. Voltage follower pulse response

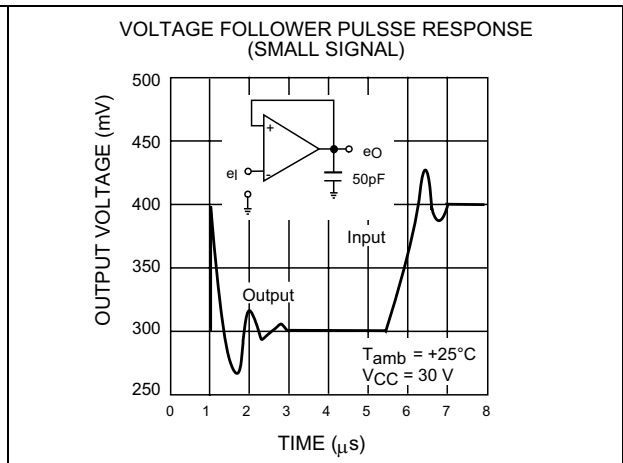


Figure 6. Input current

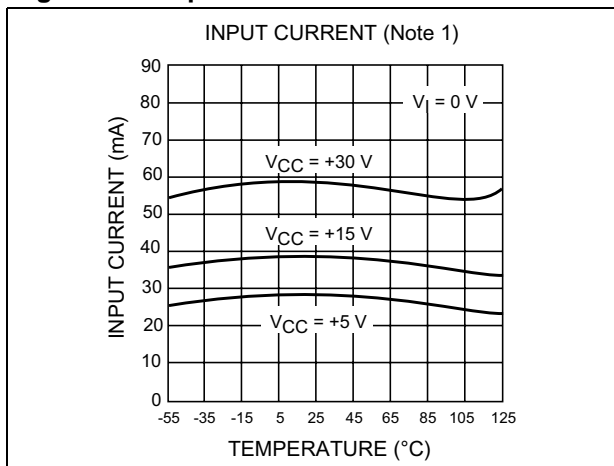


Figure 7. Output characteristics

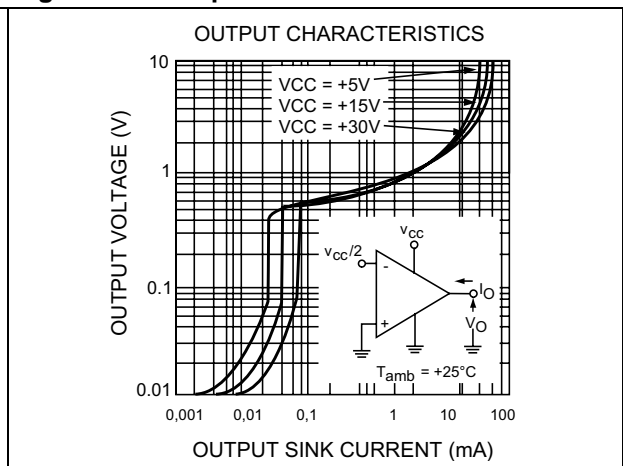


Figure 8. Output characteristics

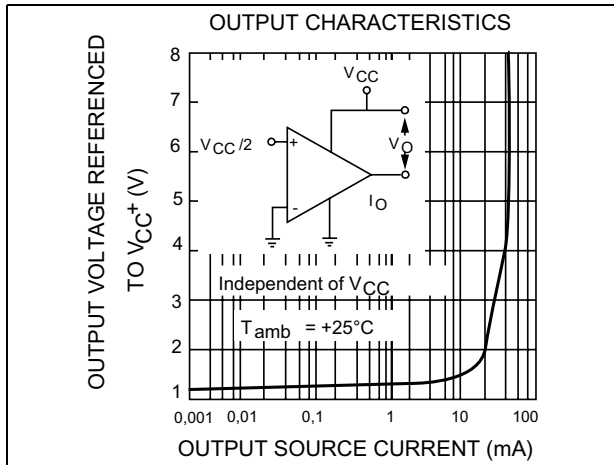


Figure 9. Current limiting

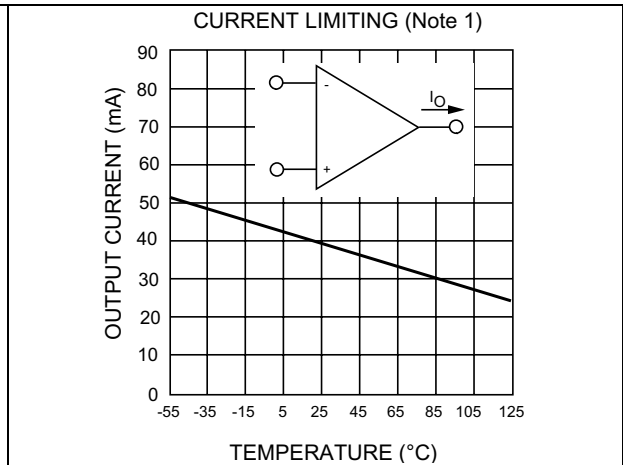


Figure 10. Input voltage range

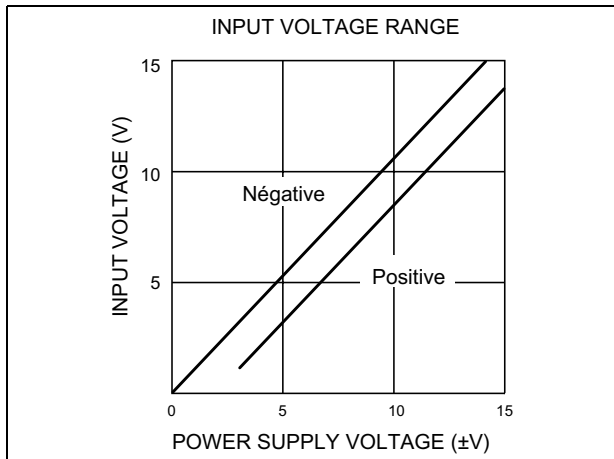


Figure 11. Positive supply voltage

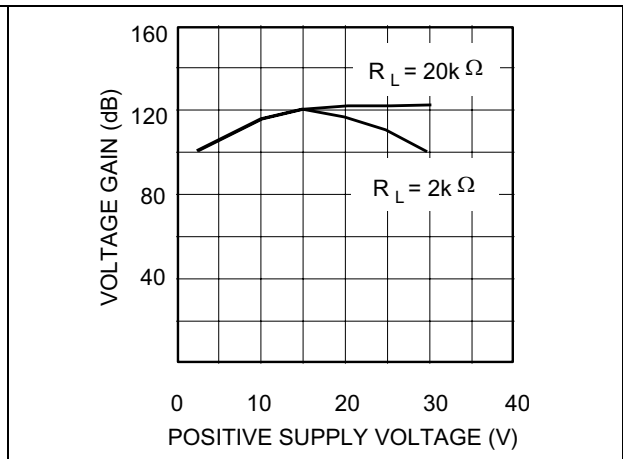


Figure 12. Input voltage range

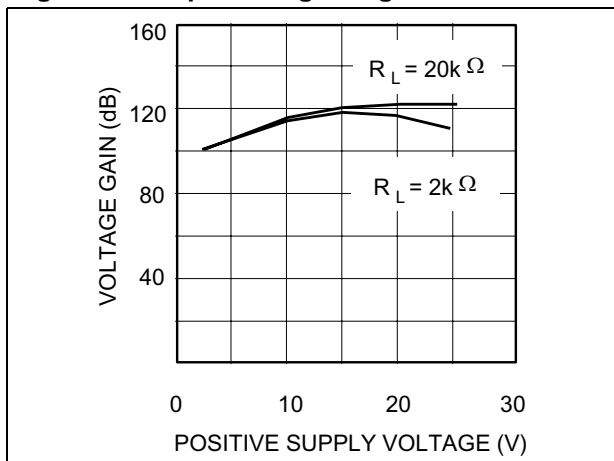


Figure 13. Supply current

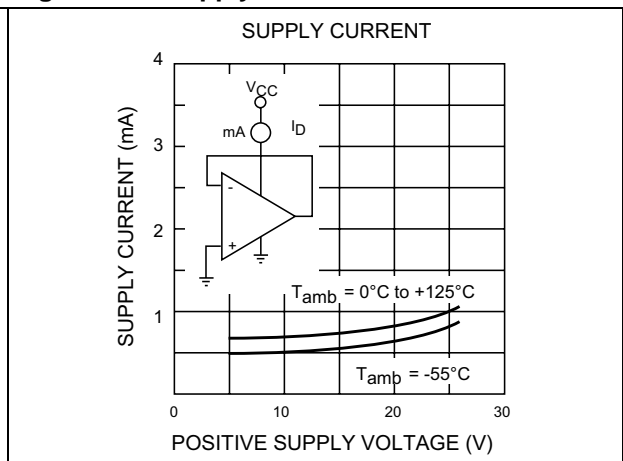


Figure 14. Input current

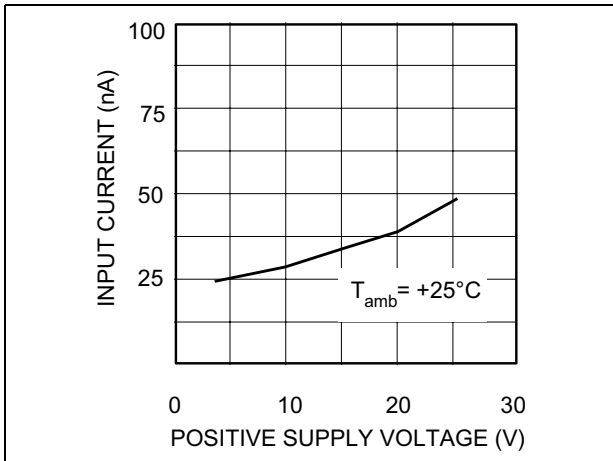


Figure 15. Gain bandwidth product

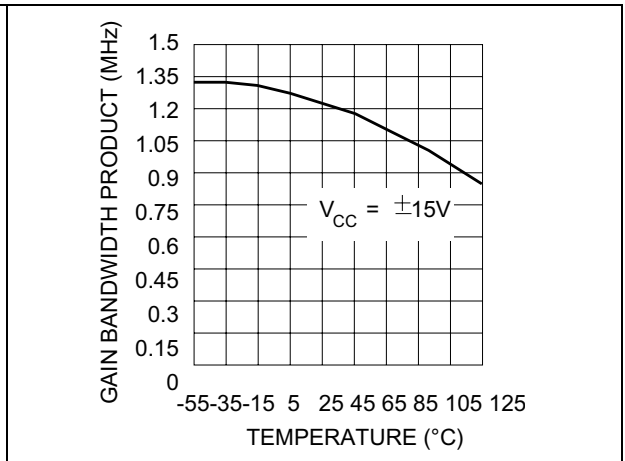


Figure 16. Power supply rejection ratio

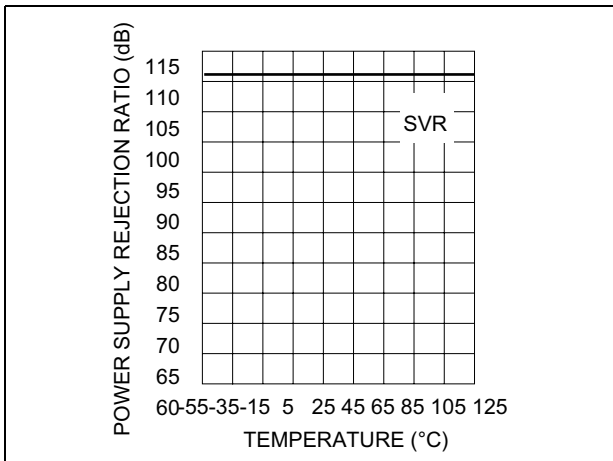


Figure 17. Common mode rejection ratio

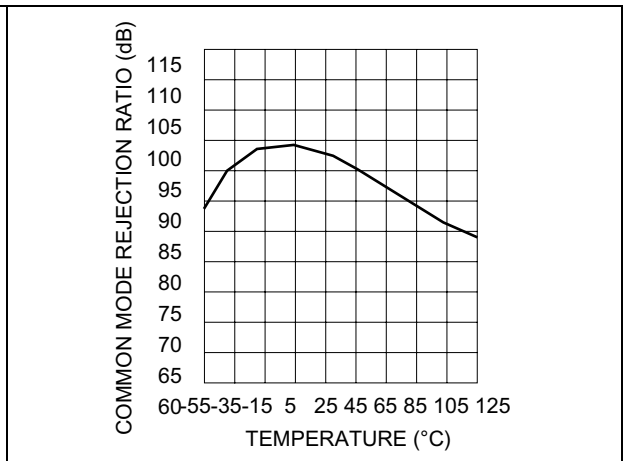
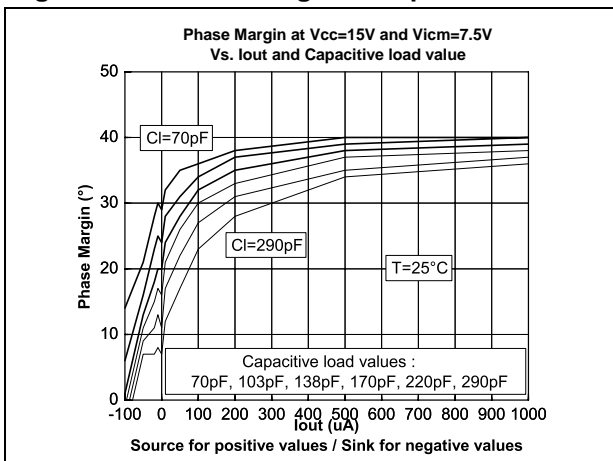


Figure 18. Phase margin vs capacitive load



4 Typical applications

Single supply voltage $V_{CC} = +5V_{dc}$.

Figure 19. AC coupled inverting amplifier

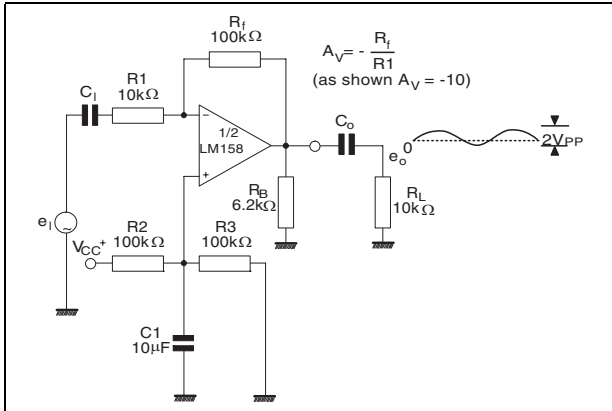


Figure 20. Non-inverting DC amplifier

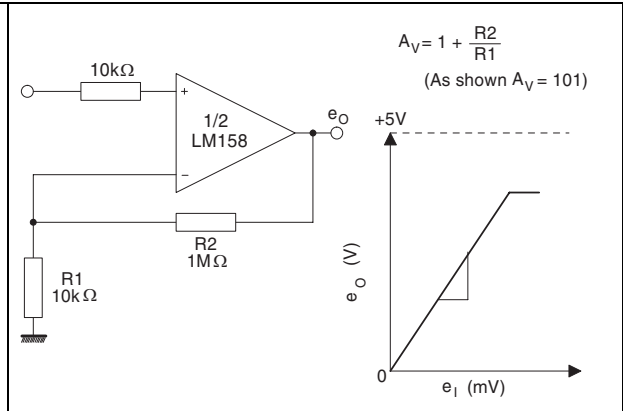


Figure 21. AC coupled non-inverting amplifier

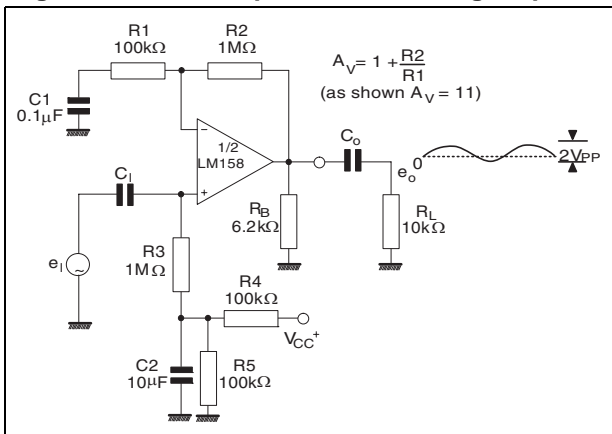


Figure 22. DC summing amplifier

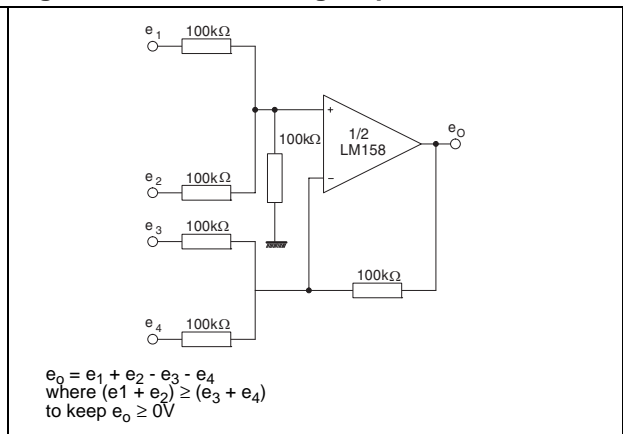


Figure 23. High input Z, DC differential amplifier

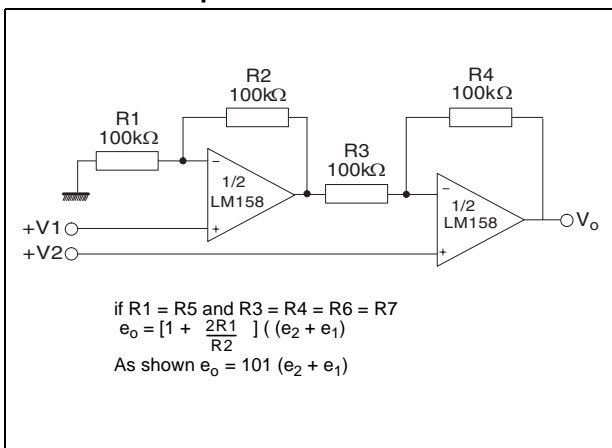


Figure 24. High input Z adjustable gain DC instrumentation amplifier

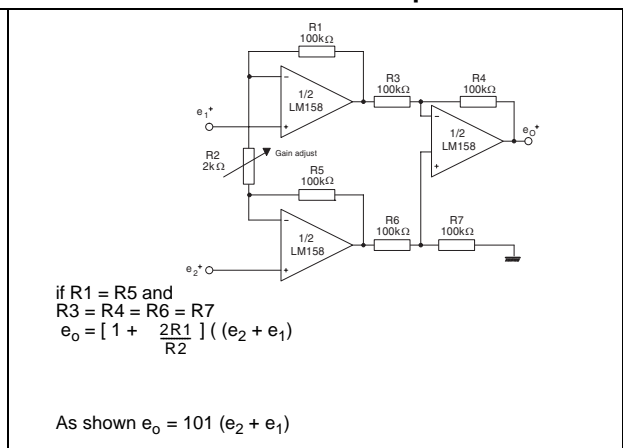


Figure 25. Using symmetrical amplifiers to reduce input current

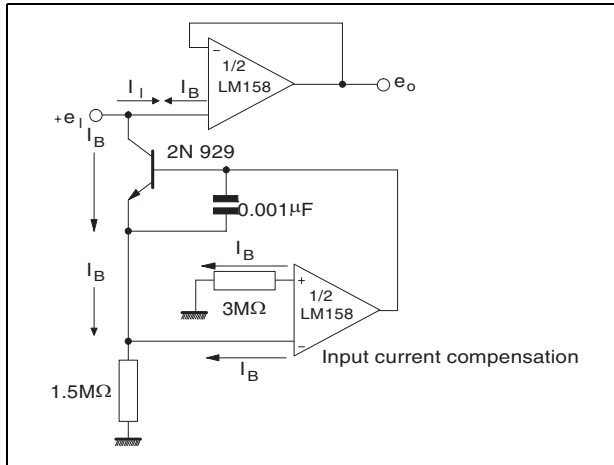


Figure 26. Low drift peak detector

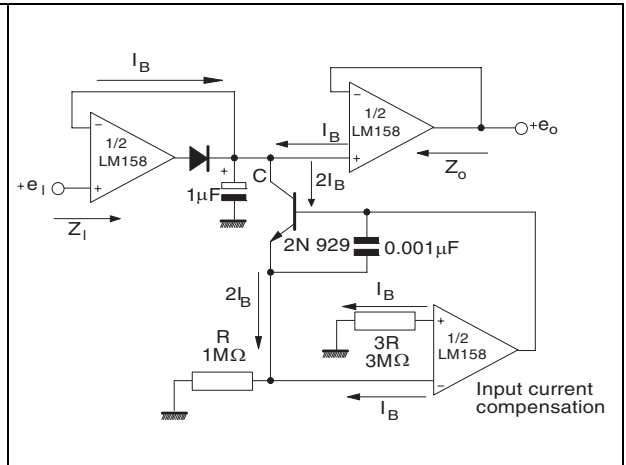
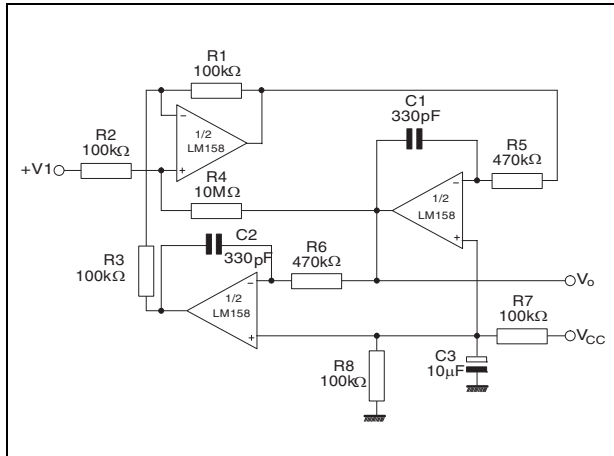


Figure 27. Active band-pass filter



5 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK[®] packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: www.st.com.

5.1 DIP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063

The figure shows three mechanical drawings of the DIP8 package:

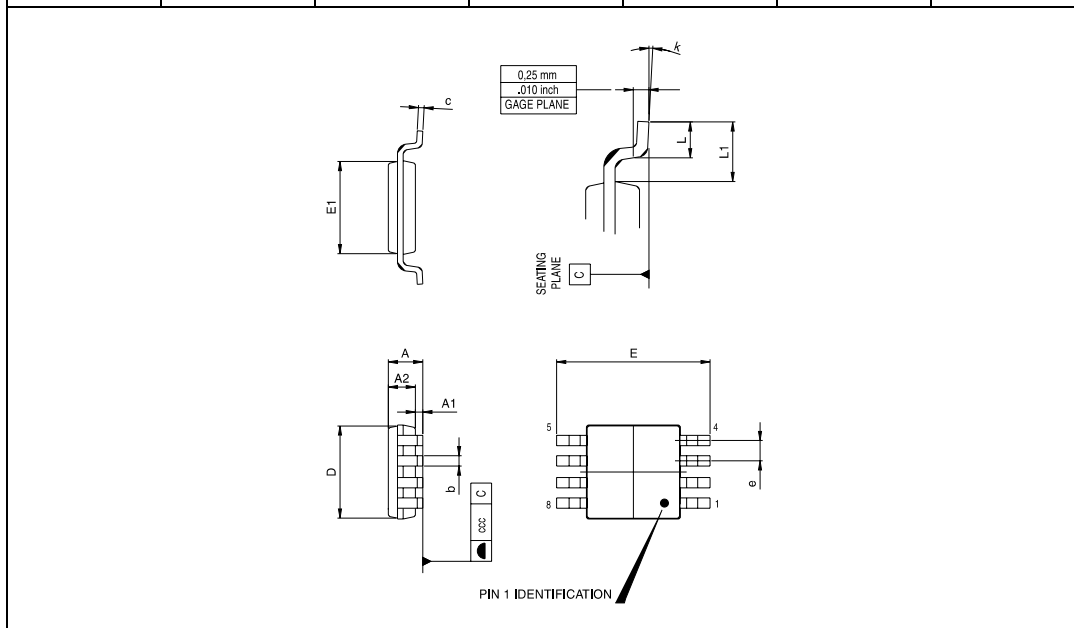
- Side View (Left):** Shows the package height and lead dimensions. Labels include A (total height), a1 (lead height), B (lead width), B1 (lead thickness), b (lead width), e (lead pitch), e3 (total lead length), and Z (lead thickness).
- Perspective View (Right):** Shows the package width and lead length. Labels include e4 (package width), b1 (lead length), and E (total package length).
- Top View (Bottom):** Shows the package footprint and pin locations. Labels include D (package width), L (package length), and pin numbers 1, 4, 5, and 8.

5.2 SO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04

5.3 MiniSO-8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.1			0.043
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.78	0.86	0.94	0.031	0.034	0.037
b	0.25	0.33	0.40	0.010	0.13	0.016
c	0.13	0.18	0.23	0.005	0.007	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.75	4.90	5.05	0.187	0.193	0.199
E1	2.90	3.00	3.10	0.114	0.118	0.122
e		0.65			0.026	
K	0°		6°	0°		6°
L	0.40	0.55	0.70	0.016	0.022	0.028
L1			0.10			0.04



5.4 TSSOP8 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	

The figure contains four mechanical drawings of the TSSOP8 package:

- Top View:** Shows the package footprint with dimensions A, A1, A2, D, b, and C. A gage plane is indicated at the bottom right.
- Side View:** Shows the package height with dimension E1 and lead length c.
- Detail View:** Shows the lead profile with dimensions k, j, and l. A gage plane is specified as 0.25 mm (.010 inch).
- Bottom View:** Shows the package from the underside with dimensions E, s, t, e, and l. A circle indicates the location of Pin 1, labeled "PIN 1 IDENTIFICATION".

6 Ordering information

Part number	Temperature range	Package	Packaging	Marking
LM158N	-55°C, +125°C	DIP-8	Tube	LM158N
LM158D LM158DT		SO-8	Tube or tape & reel	158
LM258AN		DIP-8	Tube	LM258A
LM258AD LM258ADT	-40°C, +105°C	SO-8	Tube or tape & reel	258A
LM258APT		TSSOP-8 (Thin shrink outline package)	Tape & reel	258A
LM258AST		miniSO-8	Tape & reel	K408
LM258N		DIP-8	Tube	LM258N
LM258D LM258DT		SO-8	Tube or tape & reel	258
LM258PT		TSSOP-8 (Thin shrink outline package)	Tape & reel	258
LM358N		0°C, +70°C	DIP-8	Tube
LM358AN				LM358AN
LM358D LM358DT	SO-8		Tube or tape & reel	358
LM358AD LM358ADT				358A
LM358PT	TSSOP-8 (Thin shrink outline package)		Tape & reel	358
LM358APT				358A
LM358ST	miniSO-8		Tape & reel	K405
LM358AST				K404

7 Revision history

Table 3. Document revision history

Date	Revision	Changes
1-Jul-2003	1	First release.
2-Jan-2005	2	R_{thja} and T_j parameters added in AMR Table 1 on page 4 .
1-Jul-2005	3	ESD protection inserted in Table 1 on page 4 .
5-Oct-2006	4	Added Figure 18: Phase margin vs capacitive load .
30-Nov-2006	5	Added missing ordering information.

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