March 9, 2012

TEXAS INSTRUMENTS

LM2941/LM2941C

1A Low Dropout Adjustable Regulator

General Description

The LM2941 positive voltage regulator features the ability to source 1A of output current with a typical dropout voltage of 0.5V and a maximum of 1V over the entire temperature range. Furthermore, a quiescent current reduction circuit has been included which reduces the ground pin current when the differential between the input voltage and the output voltage exceeds approximately 3V. The quiescent current with 1A of output current and an input-output differential of 5V is therefore only 30mA. Higher quiescent currents only exist when the regulator is in the dropout mode ($V_{IN} - V_{OUT} \leq 3V$).

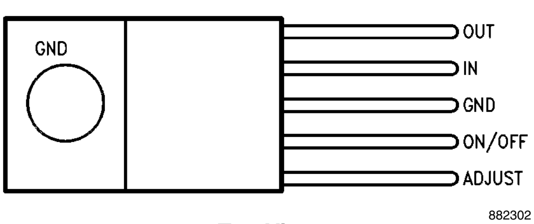
Designed also for vehicular applications, the LM2941 and all regulated circuitry are protected from reverse battery installations or two-battery jumps. During line transients, such as load dump when the input voltage can momentarily exceed the specified maximum operating voltage, the regulator will automatically shut down to protect both the internal circuits and the load. Familiar regulator features such as short circuit and thermal overload protection are also provided.

Features

- LLP space saving package
- Output voltage adjustable from 5V to 20V
- Dropout voltage typically 0.5V @ I_O = 1A
- Output current in excess of 1A
- Trimmed reference voltage
- Reverse battery protection
- Internal short circuit current limit
- Mirror image insertion protection
- P+ Product Enhancement tested
- TTL, CMOS compatible ON/OFF switch

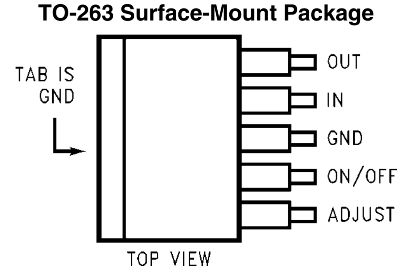
Connection Diagram and Ordering Information

TO-220 Plastic Package



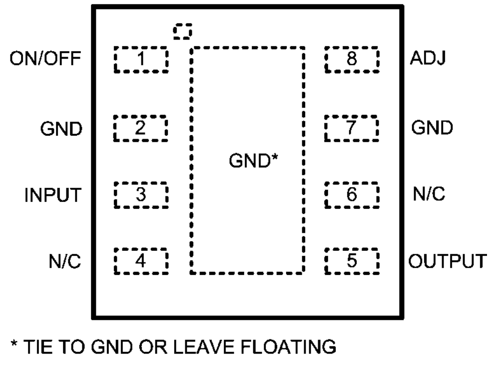
Top View
Order Number LM2941T or LM2941CT
See NS Package Number TO5A

TO-263 Surface-Mount Package



Order Number LM2941S, LM2941SX or LM2941CS, LM2941CSX
See NS Package Number TS5B

8-Lead LLP Surface Mount Package



Top View
Ordering Number LM2941LD, LM2941LDX
See NS Package Number LDC08A

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Input Voltage (Survival Voltage, ≤ 100ms)	
LM2941T, LM2941S, LM2941LD	60V
LM2941CT, LM2941CS	45V
Internal Power Dissipation (Note 4)	Internally Limited
Maximum Junction Temperature	150°C
Storage Temperature Range	$-65°C \leq T_J \leq +150°C$
Soldering Temperature (Note 9)	
TO-220 (T), Wave	260°C, 10s
TO-263 (S)	235°C, 30s
LLP-8 (LD)	235°C, 30s
ESD Rating (Note 2)	±2 kV

Operating Ratings

Maximum Input Voltage	26V
Temperature Range	
LM2941T	$-40°C \leq T_J \leq 125°C$
LM2941CT	$0°C \leq T_J \leq 125°C$
LM2941S	$-40°C \leq T_J \leq 125°C$
LM2941CS	$0°C \leq T_J \leq 125°C$
LM2941LD	$-40°C \leq T_J \leq 125°C$

Electrical Characteristics—LM2941T, LM2941S, LM2941LD

$5V \leq V_O \leq 20V$, $V_{IN} = V_O + 5V$, $C_O = 22\mu F$, unless otherwise specified. Specifications in standard typeface apply for $T_J = 25°C$, while those in **boldface type** apply over the full **Operating Temperature Range.**

Parameter	Conditions	Typ	LM2941T LM2941S LM2941LD Limit	Units (Limits)
Reference Voltage	$5mA \leq I_O \leq 1A$ (Note 7)	1.275	1.237/**1.211**	V(min)
			1.313/**1.339**	V(max)
Line Regulation	$V_O + 2V \leq V_{IN} \leq 26V$, $I_O = 5mA$	4	10/**10**	mV/V(max)
Load Regulation	$50mA \leq I_O \leq 1A$	7	10/**10**	mV/V(max)
Output Impedance	100 mADC and 20 mArms $f_O = 120Hz$	7		mΩ/V
Quiescent Current	$V_O + 2V \leq V_{IN} < 26V$, $I_O = 5mA$	10	15/**20**	mA(max)
	$V_{IN} = V_O + 5V$, $I_O = 1A$	30	45/**60**	mA(max)
RMS Output Noise, % of V_{OUT}	10Hz–100kHz $I_O = 5mA$	0.003		%
Ripple Rejection	$f_O = 120Hz$, 1 Vrms, $I_L = 100mA$	0.005	0.02/**0.04**	%/V(max)
Long Term Stability		0.4		%/1000 Hr
Dropout Voltage	$I_O = 1A$	0.5	0.8/**1.0**	V(max)
	$I_O = 100mA$	110	200/**200**	mV(max)
Short Circuit Current	V_{IN} Max = 26V (Note 8)	1.9	1.6	A(min)
Maximum Line Transient	V_O Max 1V Above Nominal V_O $R_O = 100$, $t \leq 100ms$	75	60/**60**	V(min)
Maximum Operational Input Voltage		31	26/**26**	V_{DC}
Reverse Polarity DC Input Voltage	$R_O = 100$, $V_O \geq -0.6V$	−30	−15/**−15**	V(min)
Reverse Polarity Transient Input Voltage	$t \leq 100ms$, $R_O = 100\Omega$	−75	−50/**−50**	V(min)
ON/OFF Threshold Voltage ON	$I_O \leq 1A$	1.30	0.80/**0.80**	V(max)
ON/OFF Threshold Voltage OFF	$I_O \leq 1A$	1.30	2.00/**2.00**	V(min)
ON/OFF Threshold Current	$V_{ON/OFF} = 2.0V$, $I_O \leq 1A$	50	100/**300**	μA(max)

Electrical Characteristics—LM2941CT, LM2941CS

5V ≤ V_O ≤ 20V, V_{IN} = V_O + 5V, C_O = 22µF, unless otherwise specified. Specifications in standard typeface apply for T_J = 25°C, while those in **boldface type** apply over the full **Operating Temperature Range**.

Parameter	Conditions	Typ	Limit (Note 6)	Units (Limits)
Reference Voltage	5mA ≤ I_O ≤ 1A (Note 7)	1.275	1.237/**1.211**	V(min)
			1.313/**1.339**	V(max)
Line Regulation	V_O + 2V ≤ V_{IN} ≤ 26V, I_O = 5mA	4	10	mV/V(max)
Load Regulation	50mA ≤ I_O ≤ 1A	7	10	mV/V(max)
Output Impedance	100 mADC and 20 mArms f_O = 120Hz	7		mΩ/V
Quiescent Current	V_O + 2V ≤ V_{IN} < 26V, I_O = 5mA	10	15	mA(max)
	V_{IN} = V_O + 5V, I_O = 1A	30	45/**60**	mA(max)
RMS Output Noise, % of V_{OUT}	10Hz–100kHz I_O = 5mA	0.003		%
Ripple Rejection	f_O = 120Hz, 1 Vrms, I_L = 100mA	0.005	0.02	%/V(max)
Long Term Stability		0.4		%/1000 Hr
Dropout Voltage	I_O = 1A	0.5	0.8/**1.0**	V(max)
	I_O = 100mA	110	200/**200**	mV(max)
Short Circuit Current	V_{IN} Max = 26V (Note 8)	1.9	1.6	A(min)
Maximum Line Transient	V_O Max 1V Above Nominal V_O R_O = 100Ω, T ≤ 100ms	55	45	V(min)
Maximum Operational Input Voltage		31	26	V_{DC}
Reverse Polarity DC Input Voltage	R_O = 100Ω, V_O ≥ −0.6V	−30	−15	V(min)
Reverse Polarity Transient Input Voltage	T ≤ 100ms, R_O = 100Ω	−55	−45	V(min)
ON/OFF Threshold Voltage ON	I_O ≤ 1A	1.30	0.80	V(max)
ON/OFF Threshold Voltage OFF	I_O ≤ 1A	1.30	2.00	V(min)
ON/OFF Threshold Current	$V_{ON/OFF}$ = 2.0V, I_O ≤ 1A	50	100	µA(max)

Thermal Performance

Thermal Resistance Junction-to-Case, θ_{JC}	5-Lead TO-220	1		°C/W
	5-Lead TO-263	1		°C/W
	8–Lead LLP	5.3		°C/W
Thermal Resistance Junction-to-Ambient, θ_{JA} (Note 4)	5-Lead TO-220	53		°C/W
	5-Lead TO-263 (See TO-263 MOUNTING)	73		°C/W
	8-Lead LLP (See LLP MOUNTING)	35		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed under these conditions. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The Human Body Model (HBM) is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method is per JESD22–A114.

Note 3: A military RETS specification available upon request. For more information about military-aerospace products, see the Mil-Aero web page at http://www.national.com/appinfo/milaero/index.html.

Note 4: The maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_J(max) – T_A)/θ_{JA}. If this dissipation is exceeded, the die temperature will rise above 150°C and the LM2941 will go into thermal shutdown. If the TO-263 package is used, the thermal resistance can be reduced by increasing the P.C. board copper area thermally connected to the package: Using 0.5 square inches of copper area, θ_{JA} is 50°C/W; with 1 square inch of copper area, θ_{JA} is 37°C/W; and with 1.6 or more square inches of copper area, θ_{JA} is 32°C/W. Thermal performance for the LLP package was obtained using a JESD51-7 board with six vias, using no airflow and an ambient temperature of 22°C. The value θ_{JA} for the LLP package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the LLP package, refer to Application Note AN-1187. It is recommended that 6 vias be placed under the center pad to improve thermal performance.

Note 5: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (boldface type). All limits are used to calculate Outgoing Quality Level, and are 100% production tested.

Note 6: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (boldface type). All room temperature limits are 100% production tested. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.

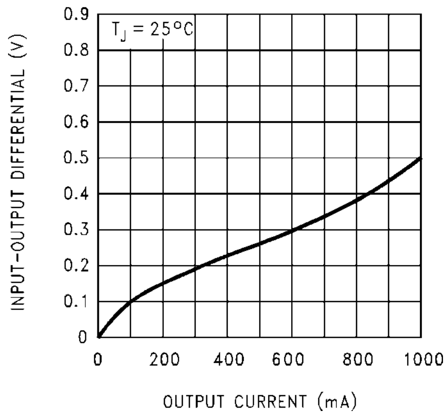
Note 7: The output voltage range is 5V to 20V and is determined by the two external resistors, R1 and R2. See Typical Application Circuit.

Note 8: Output current capability will decrease with increasing temperature, but will not go below 1A at the maximum specified temperatures.

Note 9: Refer to JEDEC J-STD-020C for surface mount device (SMD) package reflow profiles and conditions. Unless otherwise stated, the temperature and time are for Sn-Pb (STD) only.

Typical Performance Characteristics

Dropout Voltage



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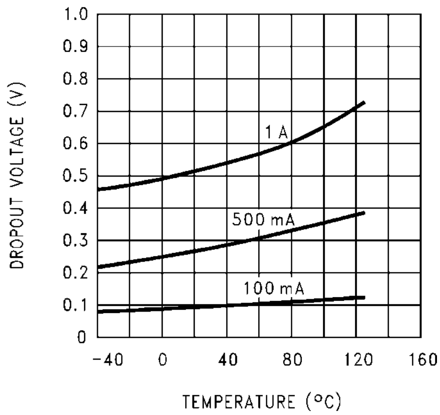
Dropout Voltage vs. Temperature



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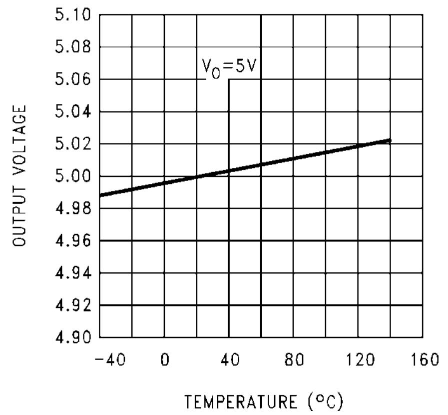
Output Voltage



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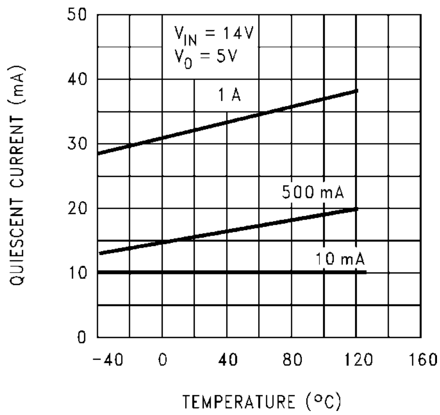
Quiescent Current vs. Temperature



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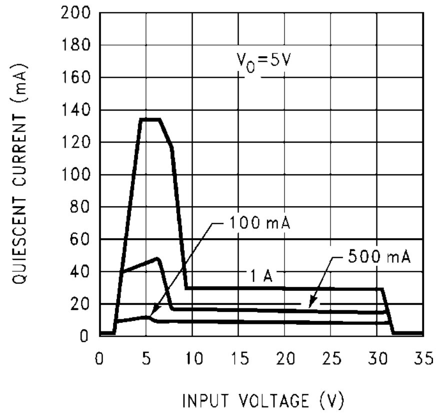
Quiescent Current



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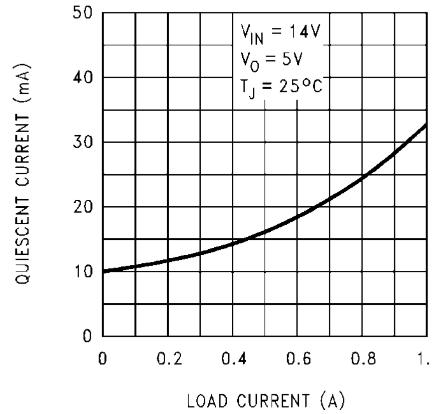
Quiescent Current



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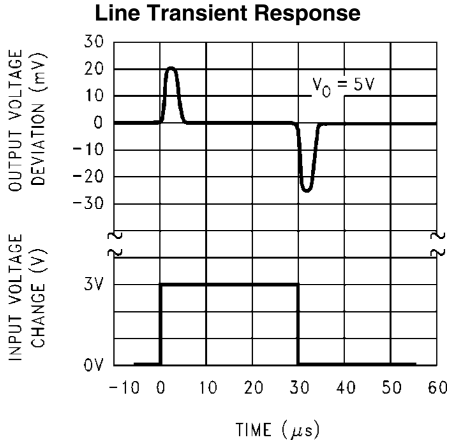
Line Transient Response



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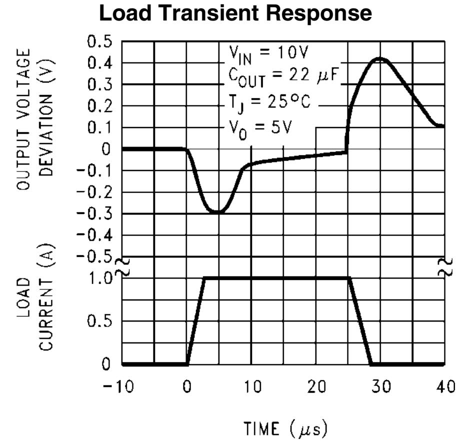
Load Transient Response



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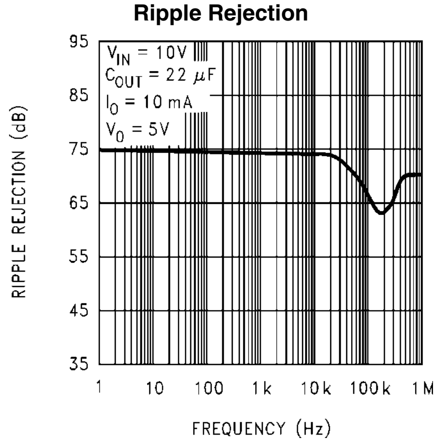
Ripple Rejection



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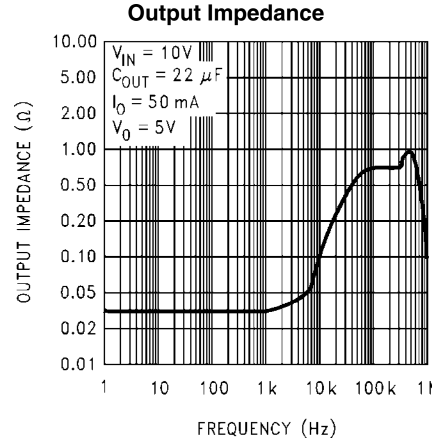
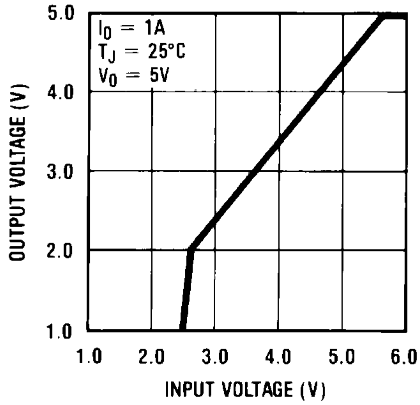
Output Impedance



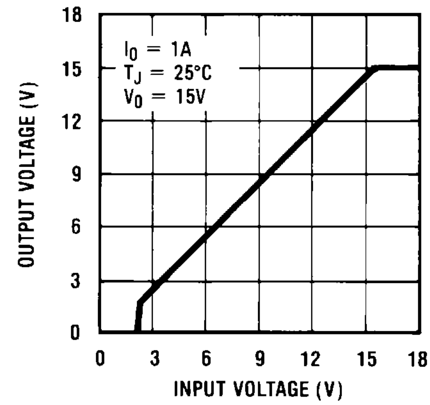
882320

Low Voltage Behavior



882321

Low Voltage Behavior



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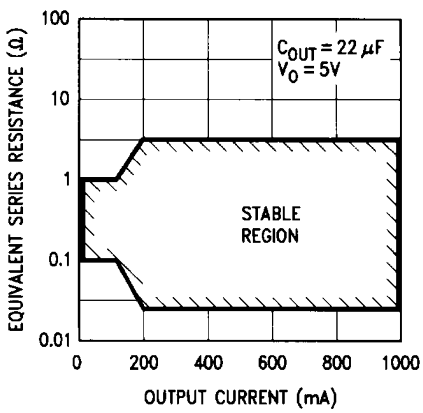
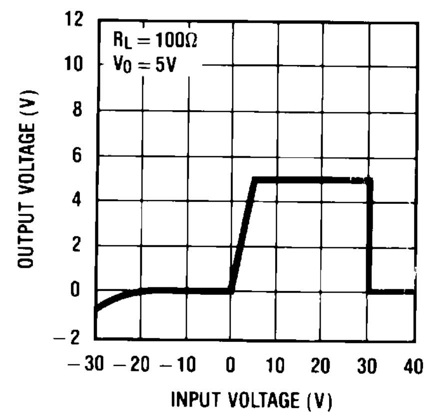
Output Capacitor ESR



882323

Output at Voltage Extremes



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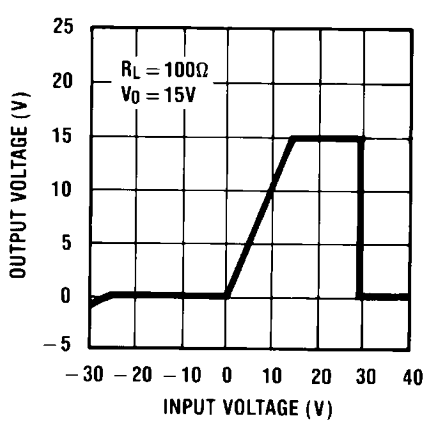
Output at Voltage Extremes



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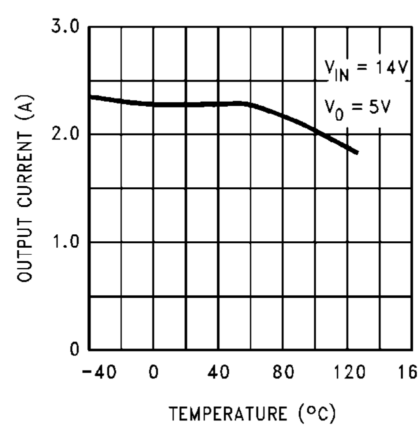
Peak Output Current



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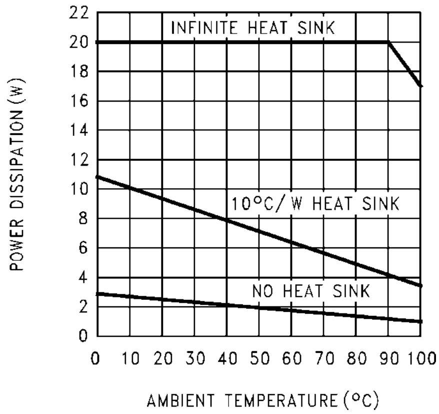
Maximum Power Dissipation (TO-220)



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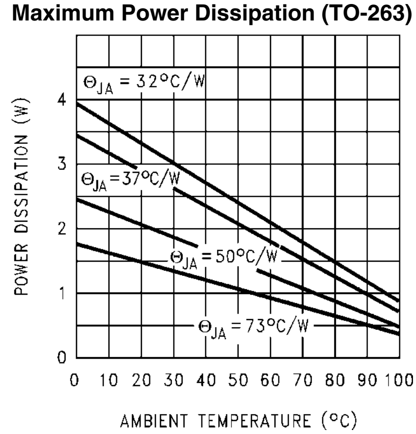
Maximum Power Dissipation (TO-263)



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Definition of Terms

Dropout Voltage: The input-voltage differential at which the circuit ceases to regulate against further reduction in input voltage. Measured when the output voltage has dropped 100mV from the nominal value obtained at (V_{OUT} + 5V) input, dropout voltage is dependent upon load current and junction temperature.

Input Voltage: The DC voltage applied to the input terminals with respect to ground.

Input-Output Differential: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate.

Line Regulation: The change in output voltage for a change in the input voltage. The measurement is made under conditions of low dissipation or by using pulse techniques such that the average chip temperature is not significantly affected.

Load Regulation: The change in output voltage for a change in load current at constant chip temperature.

Long Term Stability: Output voltage stability under accelerated life-test conditions after 1000 hours with maximum rated voltage and junction temperature.

Output Noise Voltage: The rms AC voltage at the output, with constant load and no input ripple, measured over a specified frequency range.

Quiescent Current: That part of the positive input current that does not contribute to the positive load current. The regulator ground lead current.

Ripple Rejection: The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

Temperature Stability of V_O: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

Application Hints

OUTPUT CAPACITOR

A Tantalum capacitor with a minimum capacitance value of 22 µF, and ESR in the range of 0.01Ω to 5Ω, is required at the output pin for loop stability. It must be located less than 1 cm from the device. There is no limitation on any additional capacitance.

Alternately, a high quality X5R/X7R 22 µF ceramic capacitor may be used for the output capacitor only if an appropriate value of series resistance is added to simulate the ESR requirement. The ceramic capacitor selection must include an appropriate voltage de-rating of the capacitance value due to the applied output voltage. The series resistor (for ESR simulation) should be in the range of 0.1Ω to 1.0Ω.

SETTING THE OUTPUT VOLTAGE

The output voltage range is 5V to 20V and is set by the two external resistors, R1 and R2. See the *Typical Applications*. The output voltage is given by the formula:

$$V_{OUT} = V_{REF} \times ((R1+R2) / R1)$$

where V_{REF} is typically 1.275V.

Using 1.00 kΩ for R1 will ensure that the bias current error of the adjust pin will be negligible. Using a R1 value higher than 10 kΩ may cause the output voltage to shift across temperature due to variations in the adjust pin bias current.

Calculating the upper resistor (R2) value of the pair when the lower resistor (R1) value is known is accomplished with the following formula:

$$R2 = R1 \times ((V_{OUT} / V_{REF}) - 1)$$

The resistors used for R1 and R2 should be high quality, tight tolerance, and with matching temperature coefficients. It is important to remember that, although the value of V_{REF} is guaranteed, the final value of V_{OUT} is not. The use of low quality resistors for R1 and R2 can easily produce a V_{OUT} value that is unacceptable.

ON/OFF

The ON/OFF pin has no internal pull-up or pull-down to establish a default condition and, as a result, this pin must be terminated externally, either actively or passively.

The ON/OFF pin requires a low level to enable the output, and a high level to disable the output. To ensure reliable operation, the ON/OFF pin voltage must rise above the maximum ON/$OFF_{(OFF)}$ voltage threshold (2.00V) to disable the output, and must fall below the minimum ON/$OFF_{(ON)}$ voltage threshold (0.80V) to enable the output. If the ON/OFF function is not needed this pin can be connected directly to Ground.

If the ON/OFF pin is being pulled to a high state through a series resistor, an allowance must be made for the ON/OFF pin current that will cause a voltage drop across the pull-up resistor.

THERMAL OVERLOAD PROTECTION

The LM2941 incorporates a linear form of thermal protection that limits the junction temperature (T_J) to typically 155°C.

Should the LM2941 see a fault condition that results in excessive power dissipation and the junction temperature approaches 155°C, the device will respond by reducing the output current (which reduces the power dissipation) to hold the junction temperature at 155°C.

Thermal Overload protection is not a guaranteed operating condition. Operating at, or near to, the Thermal Overload condition for any extended period of time is not encouraged, or recommended, as this may shorten the lifetime of the device.

POWER DISSIPATION

Consideration should be given to the maximum power dissipation ($P_{D(MAX)}$) which is limited by the maximum operating junction temperature ($T_{J(MAX)}$) of 125°C, the maximum operating ambient temperature ($T_{A(MAX)}$) of the application, and the thermal resistance (θ_{JA}) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the Operating Ratings. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND})$$

where I_{GND} is the operating ground pin current of the device (specified under Electrical Characteristics).

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)}$$

The maximum allowable value for junction to ambient Thermal Resistance, θ_{JA}, required to keep the junction temperature, T_J, from exceeding maximum allowed can be calculated using the formula:

$$\theta_{JA} = \Delta T_J / P_{D(MAX)}$$

The maximum allowable power dissipation, $P_{D(MAX)}$, required allowed for a specific ambient temperature can be calculated using the formula:

$$P_{D(MAX)} = \Delta T_J / \theta_{JA}$$

Additional information for thermal performance of surface mount packages can be found in *AN-1520: A Guide to Board Layout for Best Thermal Resistance for Exposed Packages*, *AN-1187: Leadless Leadframe Package (LLP)*, and *AN-2020: Thermal Design By Insight, Not Hindsight* .

TO-263 MOUNTING

The thermal dissipation of the TO-263 package is directly related to the printed circuit board construction and the amount of additional copper area connected to the TAB.

The TAB on the bottom of the TO-263 package is connected to the die substrate via a conductive die attach adhesive, and to device pin 3. As such, it is strongly recommend that the TAB area be connected to copper area directly under the TAB that is extended into the ground plane via multiple thermal vias. Alternately, but not recommended, the TAB may be left floating (i.e. no direct electrical connection). The TAB must not be connected to any potential other than ground.

For the LM2941S in the TS5B TO-263 package, the junction-to-case thermal rating, θ_{JC}, is 1°C/W, where the CASE is defined as the bottom of the package at the center of the TAB area. The junction-to-ambient thermal performance for the LM2941S in the TO-263 package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	**Thermal Vias**	θ_{JC}	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	1°C/W	73°C/W
JEDEC 4-Layer JESD 51-7	1	1°C/W	35°C/W
	2	1°C/W	30°C/W
	4	1°C/W	26°C/W
	8	1°C/W	24°C/W

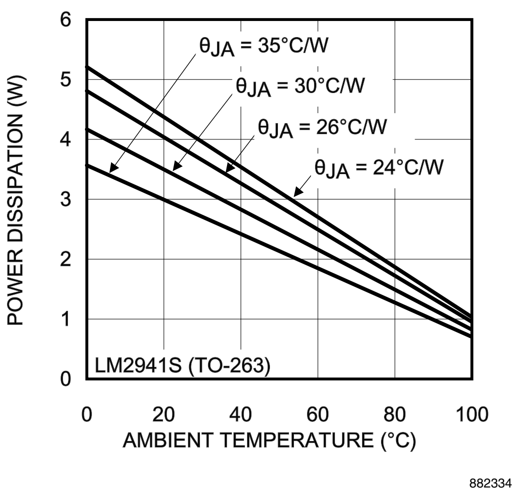


FIGURE 1. $P_{D(MAX)}$ vs T_A for LM2941S (TO-263)

LLP MOUNTING

The LDC08A (Pullback) 8-Lead LLP package requires specific mounting techniques which are detailed in Application Note # 1187. Referring to the section **PCB Design Recommendations** in AN-1187 (Page 5), it should be noted that the pad style which should be used with the LLP package is the NSMD (non-solder mask defined) type.

The thermal dissipation of the LLP package is directly related to the printed circuit board construction and the amount of additional copper area connected to the DAP.

The DAP (exposed pad) on the bottom of the LLP package is connected to the die substrate via a conductive die attach adhesive, and to device pin 2 and pin 7. As such, it is strongly recommend that the DAP area be connected copper area directly under the DAP that is extended into the ground plane via multiple thermal vias. Alternately, but not recommended, the DAP area may be left floating (i.e. no direct electrical connection). The DAP area must not be connected to any potential other than ground.

For the LM2941LD in the LDC08A 8-Lead LLP package, the junction-to-case thermal rating, θ_{JC}, is 5.3°C/W, where the CASE is defined as the bottom of the package at the center of the DAP area. The junction-to-ambient thermal performance for the LM2941LD in the LDC08A 8-Lead LLP package, using the JEDEC JESD51 standards is summarized in the following table:

Board Type	**Thermal Vias**	θ_{JC}	θ_{JA}
JEDEC 2-Layer JESD 51-3	None	5.3°C/W	181°C/W
JEDEC 4-Layer JESD 51-7	1	5.3°C/W	58°C/W
	2	5.3°C/W	49°C/W
	4	5.3°C/W	40°C/W
	6	5.3°C/W	35°C/W

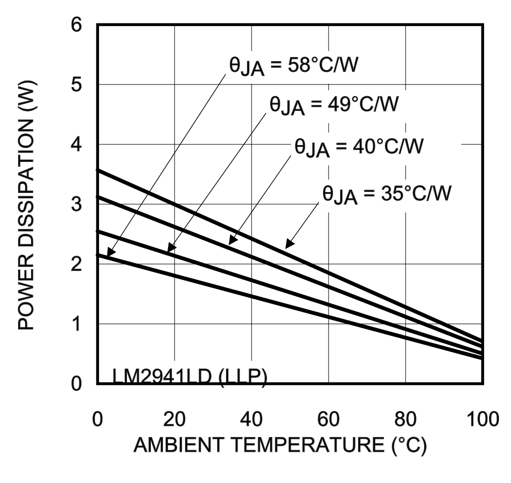
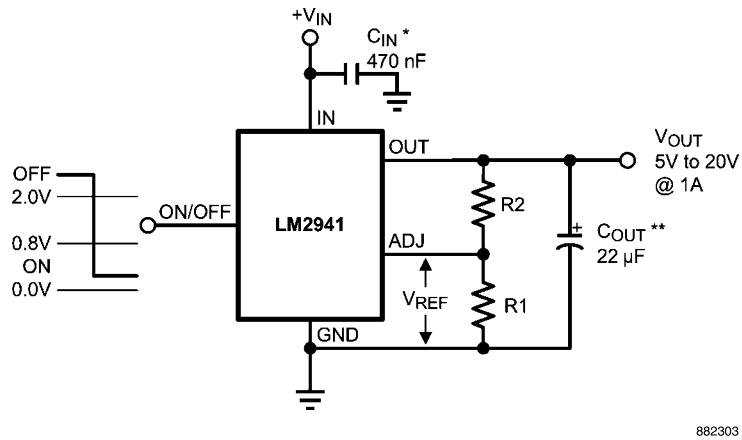


FIGURE 2. $PD_{(MAX)}$ vs T_A for LM2941LD (LLP)

Typical Applications

5V to 20V Adjustable Regulator



$$V_{OUT} = \text{Reference voltage} \times \frac{R1 + R2}{R1} \text{ where } V_{REF} = 1.275 \text{ typical}$$

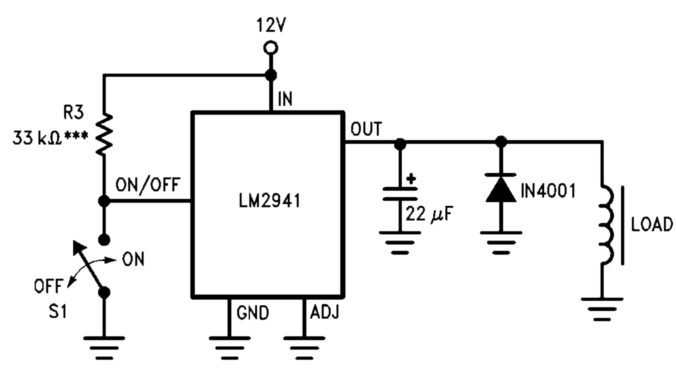
$$\text{Solving for R2: } R2 = R1 \left(\frac{V_O}{V_{REF}} - 1 \right)$$

Note: Using 1k for R1 will ensure that the bias current error from the adjust pin will be negligible. Do not bypass R1 or R2. This will lead to instabilities.

* Required if regulator is located far from power supply filter.

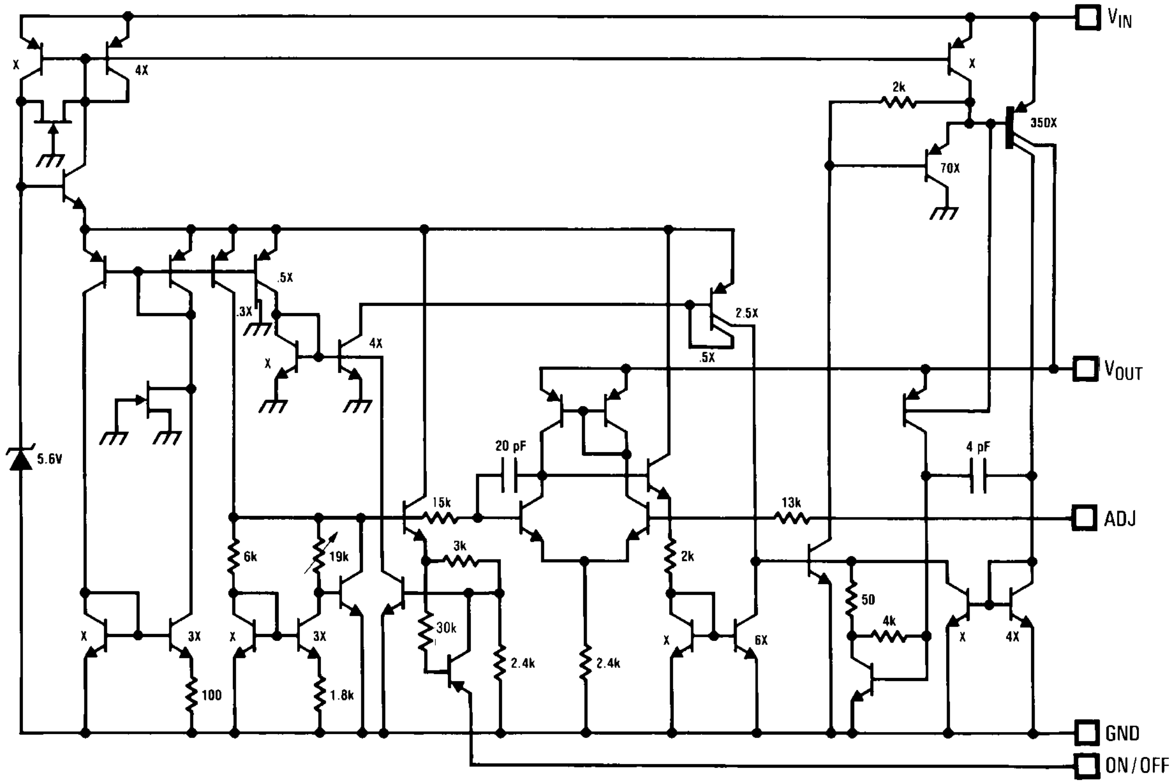
** C_{OUT} must be at least 22µF to maintain stability. May be increased without bound to maintain regulation during transients. Locate as close as possible to the regulator. This capacitor must be rated over the same operating temperature range as the regulator and the ESR is critical; see curve.

1A Switch



*** To assure shutdown, select Resistor R3 to guarantee at least 300µA of pull-up current when S1 is open. (Assume 2V at the ON/OFF pin.)

Equivalent Schematic Diagram



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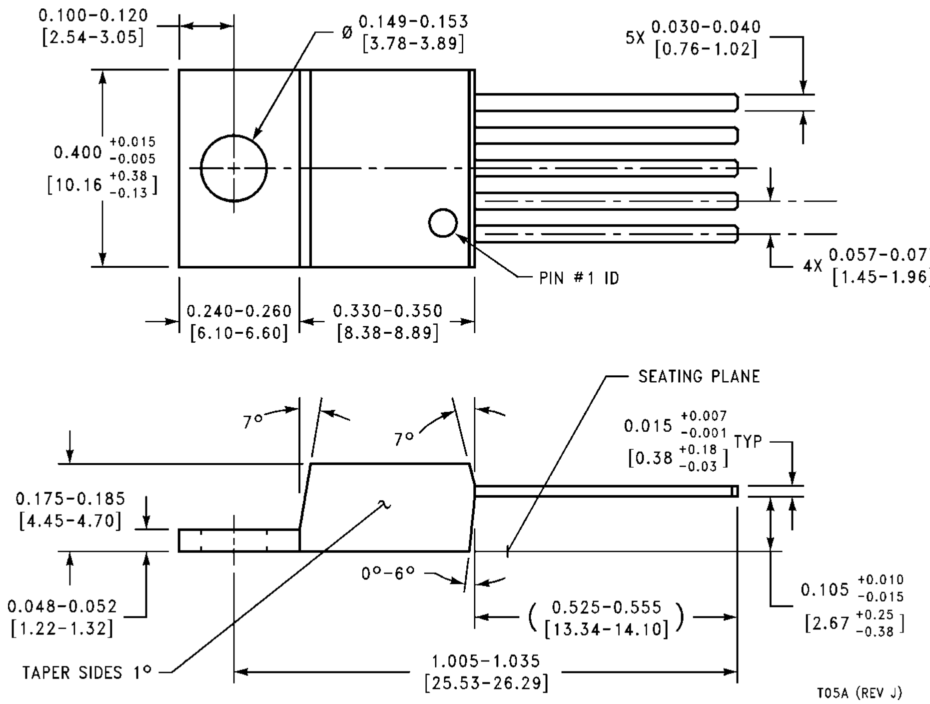
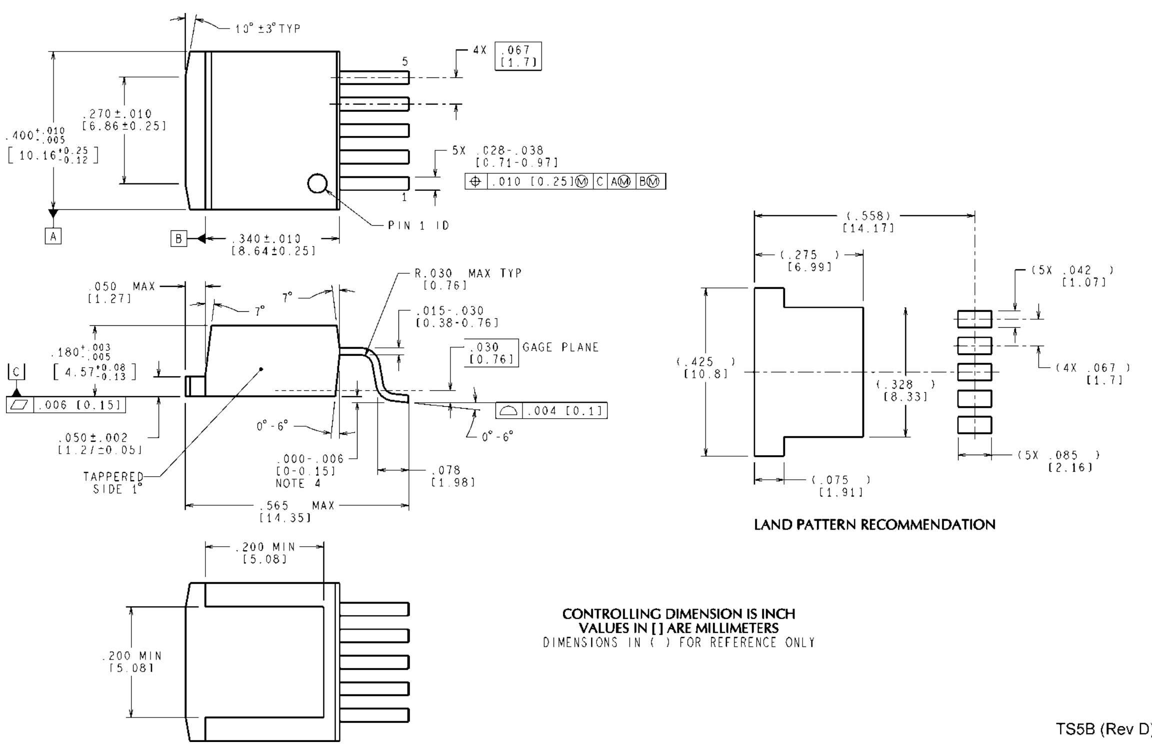
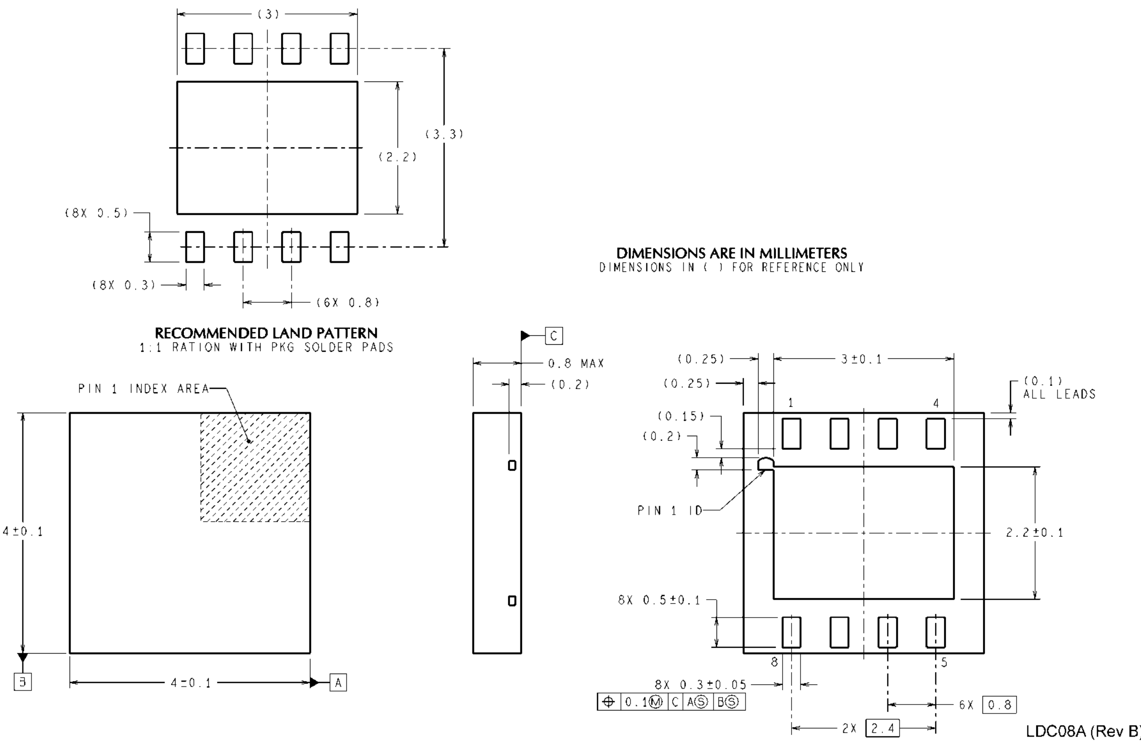
Physical Dimensions inches (millimeters) unless otherwise noted



Order Number LM2941T or LM2941CT
NS Package Number T05A



TO-263 5-Lead Plastic Surface Mount Package
Order Number LM2941S, LM2941SX, LM2941CS or LM2941CSX
NS Package Number TS5B



8-Lead LLP Surface Mount Package
Order Number LM2941LD, LM2941LDX
NS Package Number LDC08A

Notes