



Is Now Part of



**ON Semiconductor®**

To learn more about ON Semiconductor, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

# KA3842B/KA3843B/KA3844B/ KA3845B

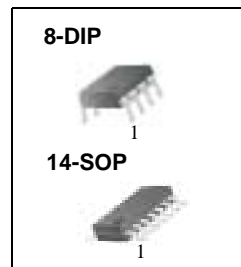
## SMPS Controller

### Features

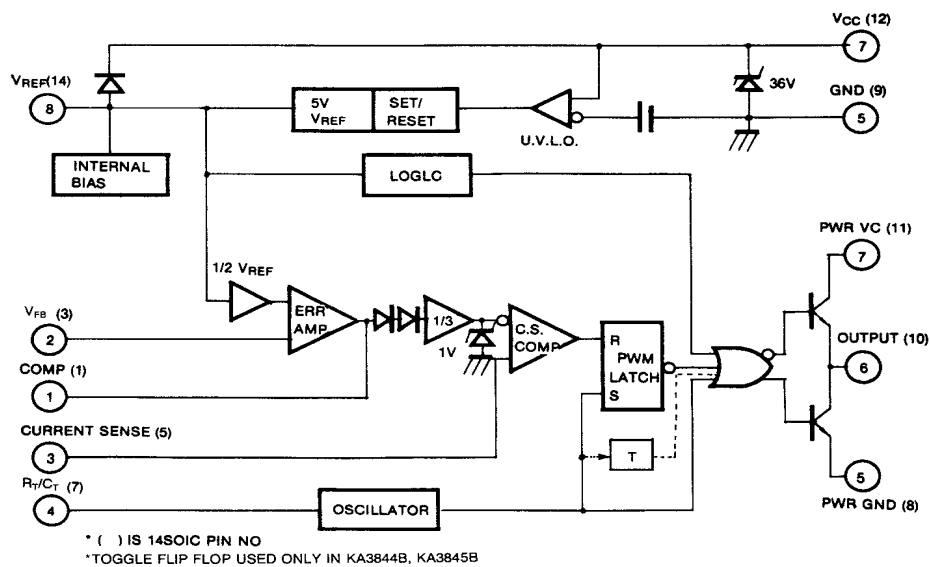
- Low Start up Current
- Maximum Duty Clamp
- UVLO With Hysteresis
- Operating Frequency up to 500KHz

### Description

The KA3842B/KA3843B/KA3844B/KA3845B are fixed frequency current-mode PWM controller. They are specially designed for Off - Line and DC-to-DC converter applications with minimum external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator and a high current totempole output for driving a power MOSFET. The KA3842B and KA3844B have UVLO thresholds of 16V (on) and 10V (off). The KA3843B and KA3845B are 8.5V (on) and 7.9V (off). The KA3842B and KA3843B can operate within 100% duty cycle. The KA3844B and KA3845B can operate with 50% duty cycle.



### Internal Block Diagram



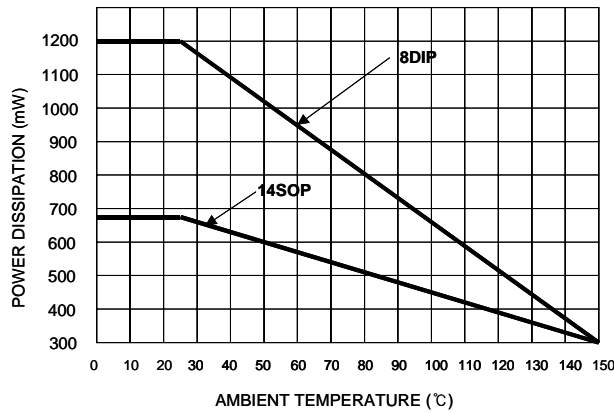
## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	30	V
Output Current	I <sub>O</sub>	±1	A
Analog Inputs (Pin 2,3)	V(ANA)	-0.3 to 6.3	V
Error Amp Output Sink Current	I <sub>SINK (E.A)</sub>	10	mA
Power Dissipation at T <sub>A</sub> ≤25°C (8DIP)	P <sub>D</sub> (Note1,2)	1200	mW
Power Dissipation at T <sub>A</sub> ≤25°C (14SOP)	P <sub>D</sub> (Note1,2)	680	mW
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C
Lead Temperature (Soldering, 10sec)	T <sub>LEAD</sub>	+300	°C

**Note:**

1. Board Thickness 1.6mm, Board Dimension 76.2mm ×114.3mm, (Reference EIA / JSED51-3, 51-7)
2. Do not exceed P<sub>D</sub> and SOA (Safe Operation Area)

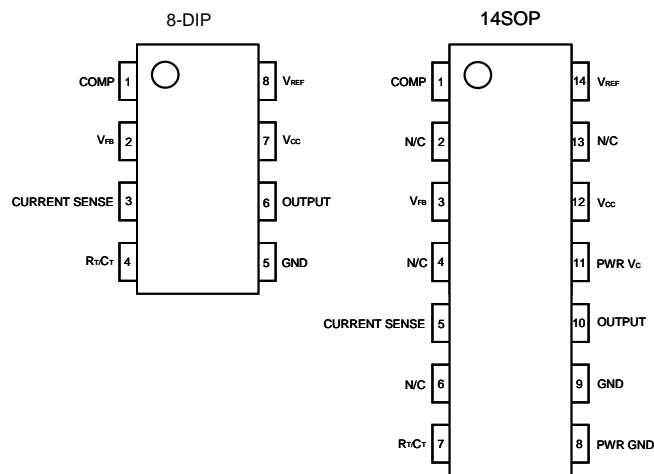
## Power Dissipation Curve



## Thermal Data

Characteristic	Symbol	8-DIP	14-SOP	Unit
Thermal Resistance Junction-ambient	R <sub>thj-amb</sub> (MAX)	100	180	°C/W

## Pin Array



## Electrical Characteristics

( $V_{CC}=15V$ ,  $R_T=10K\Omega$ ,  $C_T=3.3nF$ ,  $T_A=0^\circ C$  to  $+70^\circ C$ , unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>REFERENCE SECTION</b>						
Reference Output Voltage	VREF	$T_J = 25^\circ C$ , $I_{REF} = 1mA$	4.90	5.00	5.10	V
Line Regulation	$\Delta V_{REF}$	$12V \leq V_{CC} \leq 25V$	-	6	20	mV
Load Regulation	$\Delta V_{REF}$	$1mA \leq I_{REF} \leq 20mA$	-	6	25	mV
Short Circuit Output Current	ISC	$T_A = 25^\circ C$	-	-100	-180	mA
<b>OSCILLATOR SECTION</b>						
Oscillation Frequency	f	$T_J = 25^\circ C$	47	52	57	KHz
Frequency Change with Voltage	$\Delta f/\Delta V_{CC}$	$12V \leq V_{CC} \leq 25V$	-	0.05	1	%
Oscillator Amplitude	VOSC	-	-	1.6	-	VP-P
<b>ERROR AMPLIFIER SECTION</b>						
Input Bias Current	I <sub>BIAS</sub>	-	-	-0.1	-2	$\mu A$
Input Voltage	$V_{I(E>A)}$	$V_{pin1} = 2.5V$	2.42	2.50	2.58	V
Open Loop Voltage Gain	G <sub>VO</sub>	$2V \leq V_O \leq 4V$ (Note3)	65	90	-	dB
Power Supply Rejection Ratio	PSRR	$12V \leq V_{CC} \leq 25V$ (Note3)	60	70	-	dB
Output Sink Current	I <sub>SINK</sub>	$V_{pin2} = 2.7V$ , $V_{pin1} = 1.1V$	2	7	-	mA
Output Source Current	I <sub>SOURCE</sub>	$V_{pin2} = 2.3V$ , $V_{pin1} = 5V$	-0.6	-1.0	-	mA
High Output Voltage	V <sub>OH</sub>	$V_{pin2} = 2.3V$ , $R_L = 15K\Omega$ to GND	5	6	-	V
Low Output Voltage	V <sub>OL</sub>	$V_{pin2} = 2.7V$ , $R_L = 15K\Omega$ to Pin 8	-	0.8	1.1	V
<b>CURRENT SENSE SECTION</b>						
Gain	G <sub>V</sub>	(Note 1 & 2)	2.85	3	3.15	V/V
Maximum Input Signal	$V_{I(MAX)}$	$V_{pin1} = 5V$ (Note 1)	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$12V \leq V_{CC} \leq 25V$ (Note1,3)	-	70	-	dB
Input Bias Current	I <sub>BIAS</sub>	-	-	-3	-10	$\mu A$
<b>OUTPUT SECTION</b>						
Low Output Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 20mA	-	0.08	0.4	V
		I <sub>SINK</sub> = 200mA	-	1.4	2.2	V
High Output Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 20mA	13	13.5	-	V
		I <sub>SOURCE</sub> = 200mA	12	13.0	-	V
Rise Time	t <sub>R</sub>	$T_J = 25^\circ C$ , $C_L = 1nF$ (Note 3)	-	45	150	ns
Fall Time	t <sub>F</sub>	$T_J = 25^\circ C$ , $C_L = 1nF$ (Note 3)	-	35	150	ns
<b>UNDER-VOLTAGE LOCKOUT SECTION</b>						
Start Threshold	V <sub>TH(ST)</sub>	KA3842B/KA3844B	14.5	16.0	17.5	V
		KA3843B/KA3845B	7.8	8.4	9.0	V
Min. Operating Voltage (After Turn On)	V <sub>OPR(MIN)</sub>	KA3842B/KA3844B	8.5	10.0	11.5	V
		KA3843B/KA3845B	7.0	7.6	8.2	V

### Electrical Characteristics (Continued)

(VCC=15V, RT=10KΩ, CT=3.3nF, TA= 0°C to +70°C unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>PWM SECTION</b>						
Max. Duty Cycle	D(Max)	KA3842B/KA3843B	95	97	100	%
	D(MAX)	KA3844B/KA3845B	47	48	50	%
Min. Duty Cycle	D(MIN)	-	-	-	0	%
<b>TOTAL STANDBY CURRENT</b>						
Start-Up Current	IST	-	-	0.45	1	mA
Operating Supply Current	ICC(OPR)	Vpin3=Vpin2=ON	-	14	17	mA
Zener Voltage	VZ	ICC = 25mA	30	38	-	V

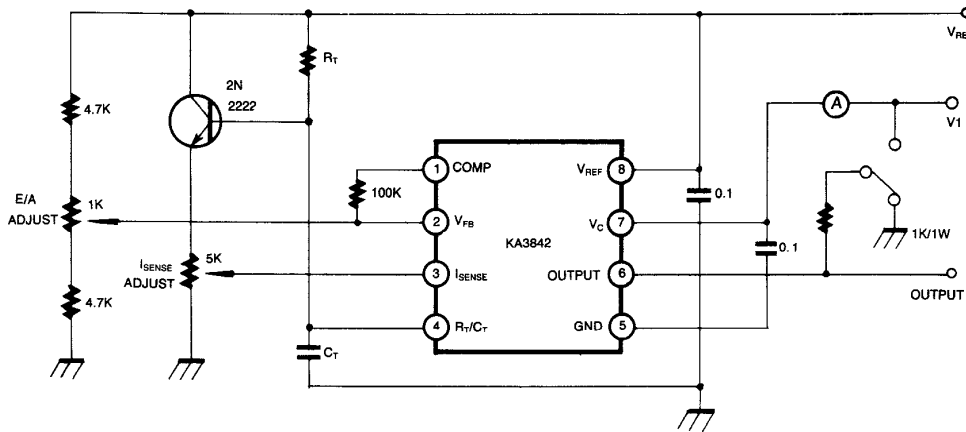
Adjust VCC above the start threshold before setting at 15V

**Note:**

1. Parameter measured at trip point of latch
2. Gain defined as:

$$A = \frac{\Delta V_{pin1}}{\Delta V_{pin3}}, 0 \leq V_{pin3} \leq 0.8V$$

3. These parameters, although guaranteed, are not 100 tested in production.



**Figure 1. Open Loop Test Circuit**

High peak currents associated with capacitive loads necessitate careful grounding techniques. Timing and bypass capacitors should be connected close to pin 5 in a single point ground. The transistor and 5KΩ potentiometer are used to sample the oscillator waveform and apply an adjustable ramp to pin 3.

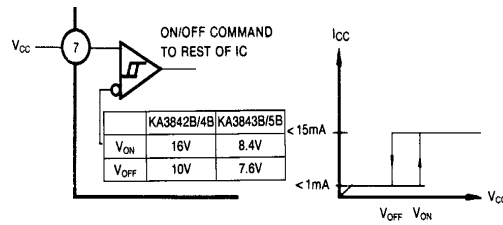


Figure 2. Under Voltage Lockout

During Under-Voltage Lock-Out, the output driver is biased to a high impedance state. Pin 6 should be shunted to ground with a bleeder resistor to prevent activating the power switch with output leakage current.

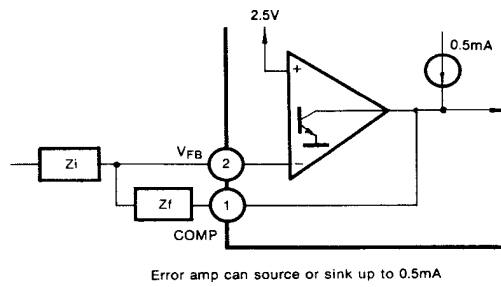


Figure 3. Error Amp Configuration

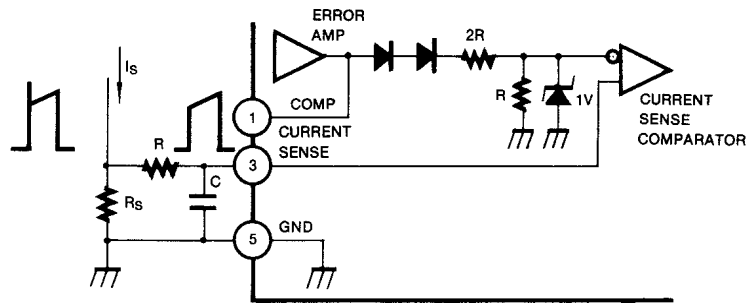


Figure 4. Current Sense Circuit

Peak current ( $I_S$ ) is determined by the formula:

$$I_S(\text{MAX}) = \frac{1.0V}{R_S}$$

A small RC filter may be required to suppress switch transients.

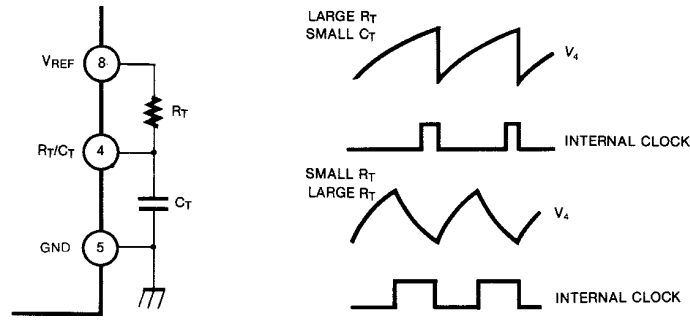


Figure 5. Oscillator Waveforms and Maximum Duty Cycle

Oscillator timing capacitor,  $C_T$ , is charged by  $V_{REF}$  through  $R_T$  and discharged by an internal current source. During the discharge time, the internal clock signal blanks the output to the low state. Selection of  $R_T$  and  $C_T$  therefore determines both oscillator frequency and maximum duty cycle. Charge and discharge times are determined by the formulas:

$$t_c = 0.55 R_T C_T$$

$$t_D = R_T C_T I_n \left( \frac{0.0063 R_T - 2.7}{0.0063 R_T - 4} \right)$$

Frequency, then, is:  $f = (t_c + t_d)^{-1}$

$$\text{For } R_T > 5k\Omega, f = \frac{1.8}{R_T C_T}$$

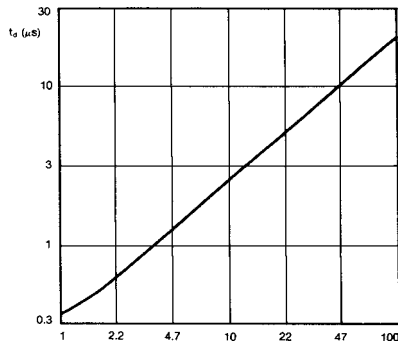


Figure 6. Oscillator Dead Time & Frequency  
(Deadtime vs  $C_T$   $R_T > 5k\Omega$ )

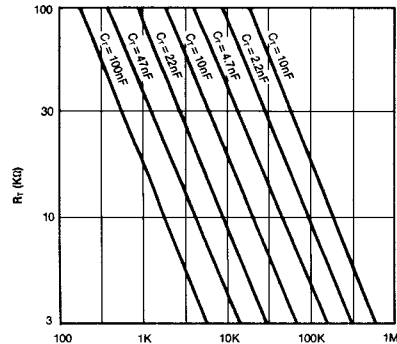


Figure 7. Timing Resistance vs Frequency

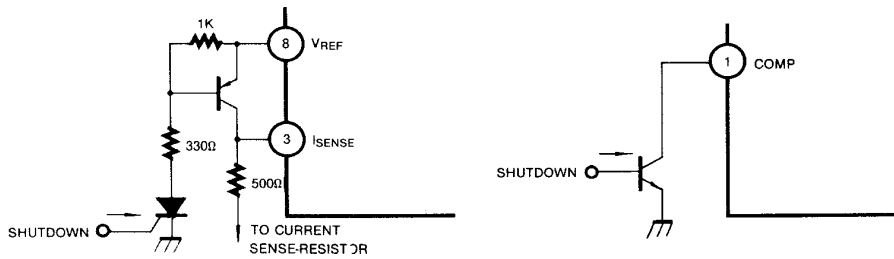


Figure 8. Shutdown Techniques

Shutdown of the KA3842B can be accomplished by two methods; either raise pin 3 above 1V or pull pin 1 below a voltage two diode drops above ground. Either method causes the output of the PWM comparator to be high (refer to block diagram). The PWM latch is reset dominant so that the output will remain low until the next clock cycle after the shutdown condition at pins 1 and/or 3 is removed. In one example, an externally latched shutdown may be accomplished by adding an SOR which will be reset by cycling VCC below the lower UVLO threshold. At this point the reference turns off, allowing the SCR to reset.

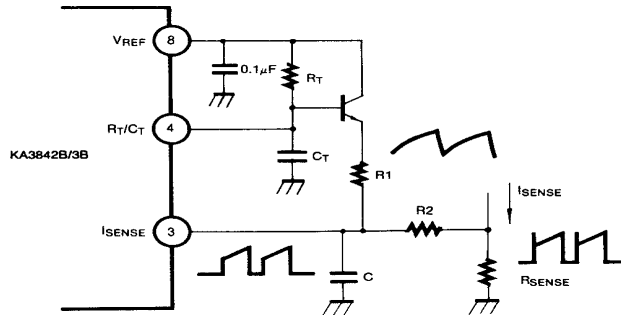


Figure 9. Slope Compensation

A fraction of the oscillator ramp can be resistively summed with the current sense signal to provide slope compensation for converters requiring duty cycles over 50%. Note that capacitor, CT, forms a filter with R2 to suppress the leading edge switch spikes.

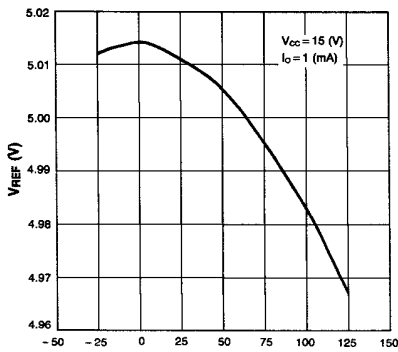


Figure 10. Temperature Drift (Vref)

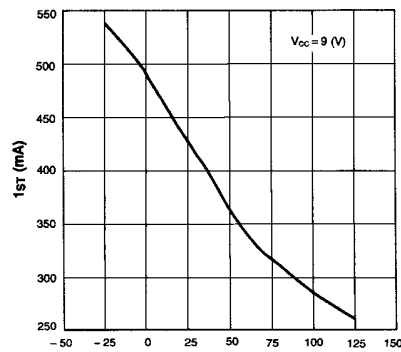


Figure 11. Temperature Drift (Ist)

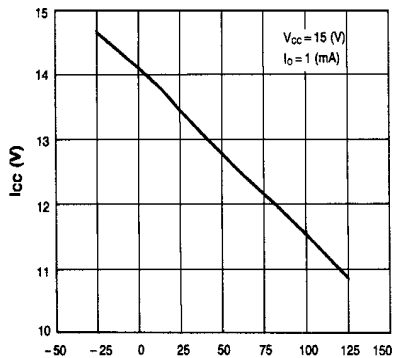


Figure 12. Temperature Drift (Icc)

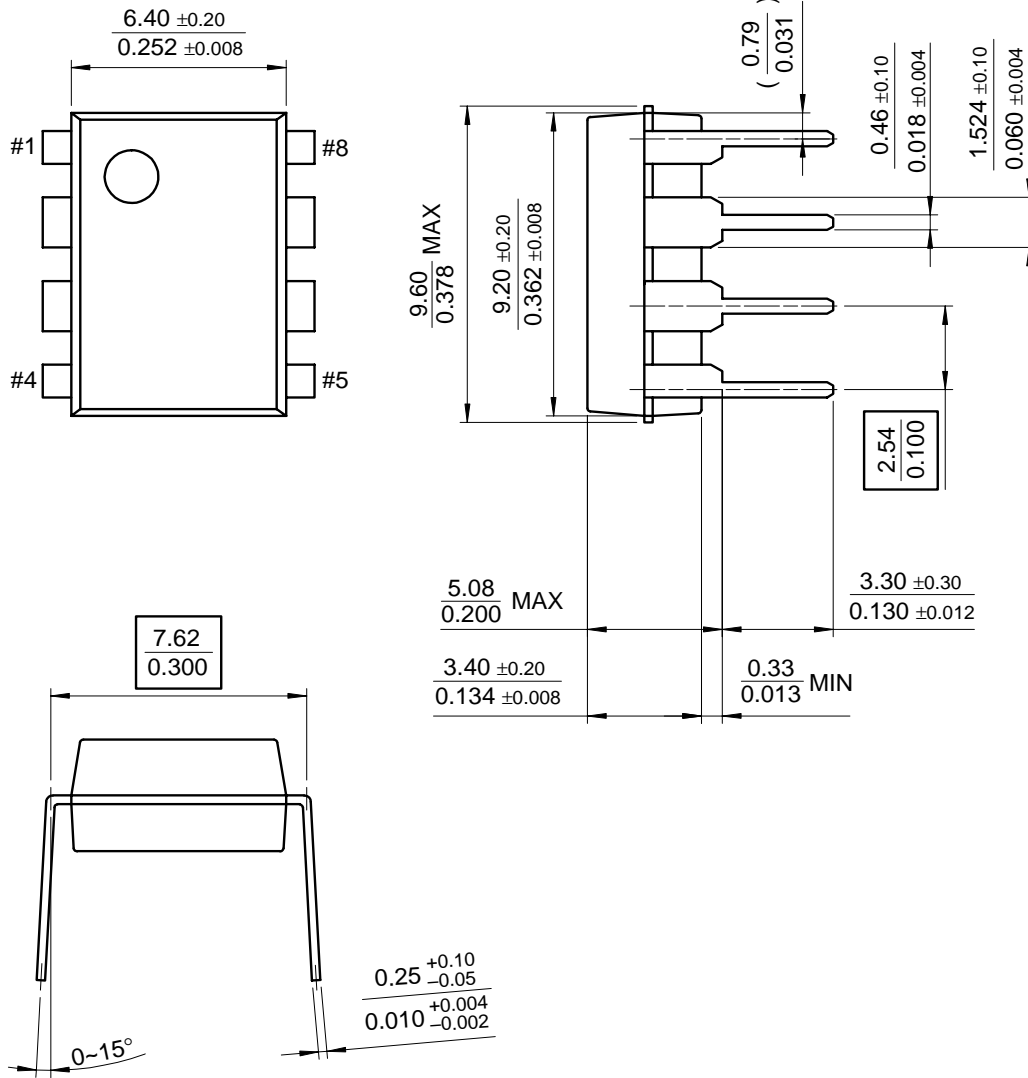


# Mechanical Dimensions

## Package

Dimensions in millimeters

### 8-DIP

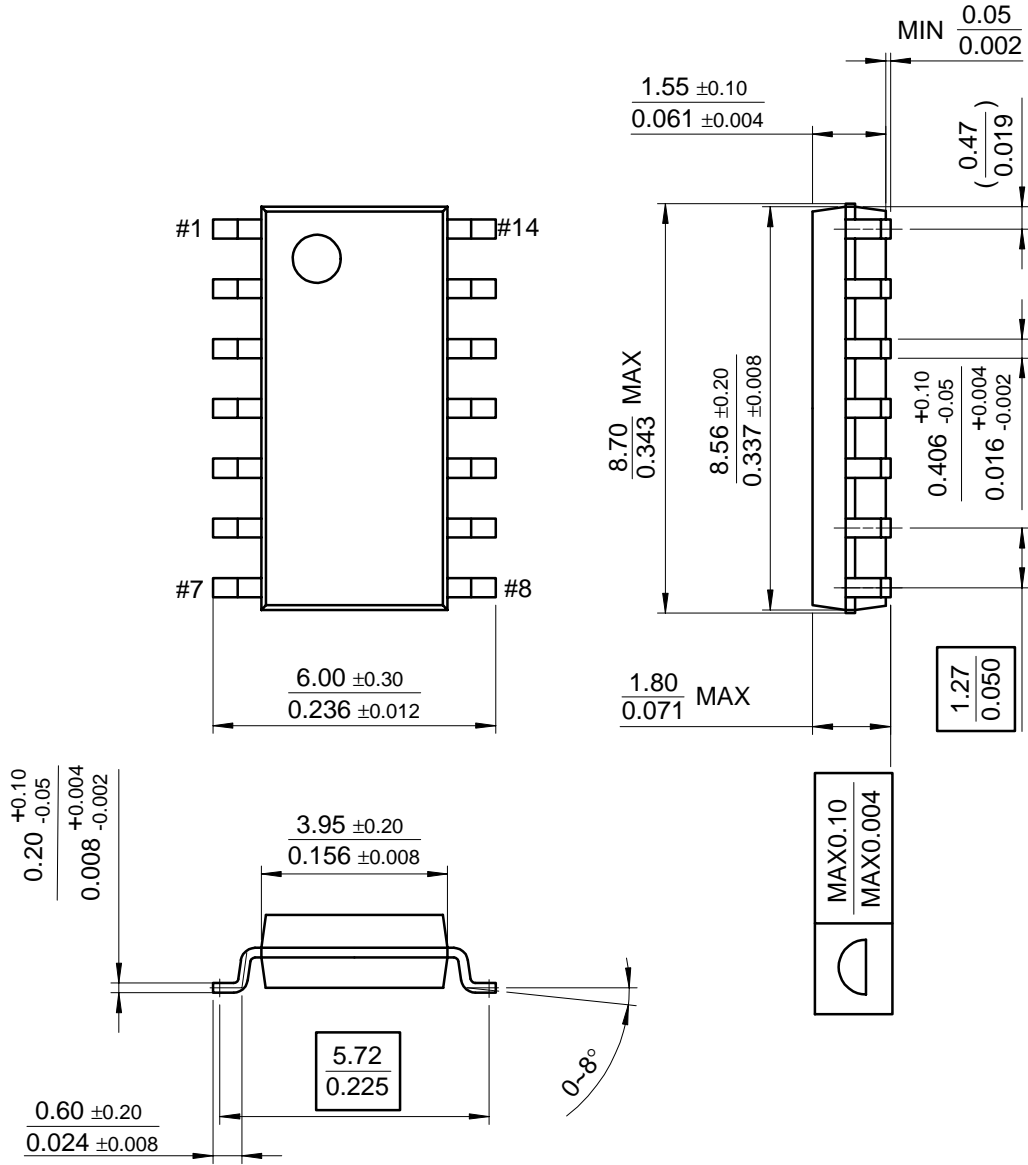


**Mechanical Dimensions** (Continued)

Package

Dimensions in millimeters

**14-SOP**



## Ordering Information

Product Number	Package	Operating Temperature
KA3842B	8-DIP	0 ~ + 70°C
KA3843B		
KA3844B		
KA3845B		
KA3842BD	14-SOP	
KA3843BD		
KA3844BD		
KA3845BD		

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.