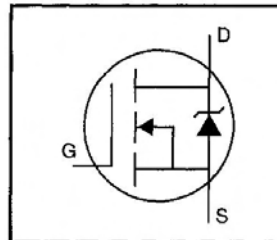


# IRLD120PbF

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Logic-Level Gate Drive
- R<sub>DS(on)</sub> Specified at V<sub>GS</sub>=4V & 5V
- 175°C Operating Temperature
- Lead-Free



$$V_{DSS} = 100V$$

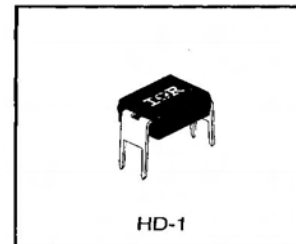
$$R_{DS(on)} = 0.27\Omega$$

$$I_D = 1.3A$$

## Description

Third Generation HEXFETs from International Rectifier provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The 4-pin DIP package is a low cost machine-insertable case style which can be stacked in multiple combinations on standard 0.1 inch pin centers. The dual drain serves as a thermal link to the mounting surface for power dissipation levels up to 1 watt.



## Absolute Maximum Ratings

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 5.0 V	1.3	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 5.0 V	0.94	
I <sub>DM</sub>	Pulsed Drain Current ①	10	
P <sub>O</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	1.3	W
	Linear Derating Factor	0.0083	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±10	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	690	mJ
I <sub>AR</sub>	Avalanche Current ①	1.3	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	0.13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
R <sub>θJA</sub>	Junction-to-Ambient	—	—	120	°C/W

# IRLD120PbF

International  
IR Rectifier

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS}=0V, I_D=250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.27	$\Omega$	$V_{GS}=5.0V, I_D=0.78A$ ④
		—	—	0.38		$V_{GS}=4.0V, I_D=0.65A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	$V_{DS}=V_{GS}, I_D=250\mu A$
$g_{fs}$	Forward Transconductance	1.9	—	—	S	$V_{DS}=50V, I_D=0.78A$ ④
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	$\mu A$	$V_{DS}=100V, V_{GS}=0V$
		—	—	250		$V_{DS}=80V, V_{GS}=0V, T_J=150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS}=10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS}=-10V$
$Q_g$	Total Gate Charge	—	—	12	nC	$I_D=9.2A$
$Q_{gs}$	Gate-to-Source Charge	—	—	3.0		$V_{DS}=80V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	7.1		$V_{GS}=5.0V$ See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	9.8	—	ns	$V_{DD}=50V$
$t_r$	Rise Time	—	64	—		$I_D=9.2A$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G=9.0\Omega$
$t_f$	Fall Time	—	27	—		$R_D=5.2\Omega$ See Figure 10 ④
$L_D$	Internal Drain Inductance	—	4.0	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	6.0	—		
$C_{iss}$	Input Capacitance	—	490	—	pF	$V_{GS}=0V$
$C_{oss}$	Output Capacitance	—	150	—		$V_{DS}=25V$
$C_{rss}$	Reverse Transfer Capacitance	—	30	—		$f=1.0\text{MHz}$ See Figure 5

## Source-Drain Ratings and Characteristics

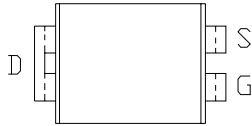
	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	1.3	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	10		
$V_{SD}$	Diode Forward Voltage	—	—	2.5	V	$T_J=25^\circ\text{C}, I_S=1.3A, V_{GS}=0V$ ④
$t_{rr}$	Reverse Recovery Time	—	130	140	ns	$T_J=25^\circ\text{C}, I_F=9.2A$
$Q_{rr}$	Reverse Recovery Charge	—	0.83	1.0	$\mu C$	$di/dt=100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)
- ②  $V_{DD}=25V$ , starting  $T_J=25^\circ\text{C}$ ,  $L=153\text{mH}$ ,  $R_G=25\Omega$ ,  $I_S=2.6A$  (See Figure 12)
- ③  $I_{SD}\leq 9.2A$ ,  $di/dt\leq 110A/\mu s$ ,  $V_{DD}\leq V_{(BR)DSS}$ ,  $T_J\leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

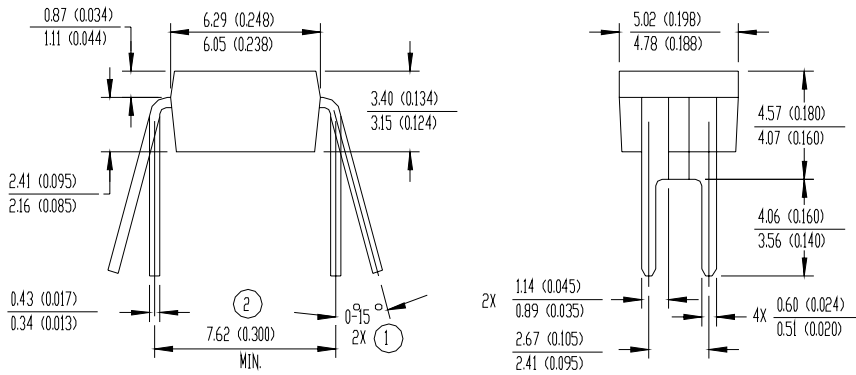
# IRLD120PbF

## Hexdip Package Outline



NOTES:

- ① APPLIES TO SPREAD OF LEADS PRIOR TO INSTALLATION
- ② APPLIES TO INSTALLED LEAD CENTERS
- 3 CONTROLLING DIMENSION: INCH
- 4 DIMENSIONS ARE SHOWN MILLIMETERS (INCHES)
- 5 CASE STYLE HD-1 (SIMILAR TO JEDEC OUTLINE MO-001AN)
- 6 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP  
SOLDER DIP MAX. + 0.16 (0.006)



## Hexdip Part Marking Information

EXAMPLE: THIS IS AN IRFD120

