

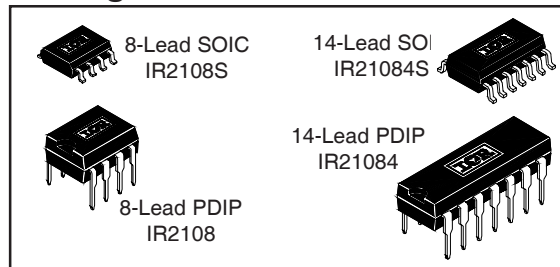
## IR2108(4) (S) & (PbF)

### HALF-BRIDGE DRIVER

#### Features

- Floating channel designed for bootstrap operation Fully operational to +600V Tolerant to negative transient voltage dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- 3.3V, 5V and 15V input logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- High side output in phase with HIN input
- Low side output out of phase with LIN input
- Logic and power ground +/- 5V offset.
- Internal 540ns dead-time, and programmable up to 5us with one external R<sub>DT</sub> resistor (IR21084)
- Lower di/dt gate driver for better noise immunity
- Available in Lead-Free

#### Packages



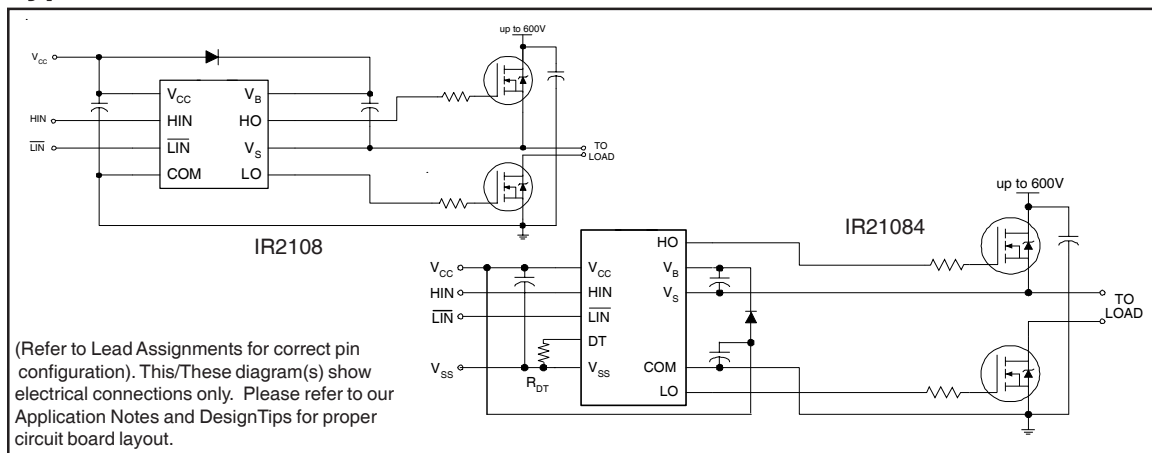
#### 2106/2301//2108//2109/2302/2304 Feature Comparison

Part	Input logic	Cross-conduction prevention logic	Dead-Time	Ground Pins
2106/2301	HIN/LIN	no	none	COM
21064				VSS/COM
2108	HIN/LIN	yes	Internal 540ns	COM
21084				VSS/COM
2109/2302	IN/SD	yes	Internal 540ns	COM
21094				VSS/COM
2304	HIN/LIN	yes	Internal 100ns	COM

#### Description

The IR2108(4)(S) are high voltage, high speed power MOSFET and IGBT drivers with dependent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 volts.

#### Typical Connection



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## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating absolute voltage	-0.3	625	V	
V <sub>S</sub>	High side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
DT	Programmable dead-time pin voltage (IR21084 only)	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage (HIN & LIN)	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3		
V <sub>SS</sub>	Logic ground (IR21084 only)	V <sub>CC</sub> - 25	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
		(14 lead PDIP)	—	1.6	
		(14 lead SOIC)	—	1.0	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
		(14 lead PDIP)	—	75	
		(14 lead SOIC)	—	120	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-50	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> and V<sub>SS</sub> offset rating are tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V	
V <sub>S</sub>	High side floating supply offset voltage	Note 1	600		
V <sub>HO</sub>	High side floating output voltage	V <sub>S</sub>	V <sub>B</sub>		
V <sub>CC</sub>	Low side and logic fixed supply voltage	10	20		
V <sub>LO</sub>	Low side output voltage	0	V <sub>CC</sub>		
V <sub>IN</sub>	Logic input voltage	IR2108	COM		V <sub>CC</sub>
		IR21084	V <sub>SS</sub>		V <sub>CC</sub>
DT	Programmable dead-time pin voltage (IR21084 only)	V <sub>SS</sub>	V <sub>CC</sub>	°C	
V <sub>SS</sub>	Logic ground (IR21084 only)	-5	5		
T <sub>A</sub>	Ambient temperature	-40	125		

Note 1: Logic operational for V<sub>S</sub> of -5 to +600V. Logic state held for V<sub>S</sub> of -5V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

### Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$ ,  $V_{SS} = COM$ ,  $C_L = 1000 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ ,  $DT = V_{SS}$  unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	220	300	nsec	$V_S = 0V$
$t_{off}$	Turn-off propagation delay	—	200	280		$V_S = 0V \text{ or } 600V$
MT	Delay matching $  t_{on} - t_{off}  $	—	0	30		
$t_r$	Turn-on rise time	—	150	220		$V_S = 0V$
$t_f$	Turn-off fall time	—	50	80		$V_S = 0V$
DT	Deadtime: LO turn-off to HO turn-on(DT <sub>LO-HO</sub> ) & HO turn-off to LO turn-on (DT <sub>HO-LO</sub> )	400	540	680		usec
		4	5	6	RDT = 200k (IR21084)	
MDT	Deadtime matching = $  DT_{LO-HO} - DT_{HO-LO}  $	—	0	60	nsec	RDT=0
		—	0	600		RDT = 200k (IR21084)

### Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$ ,  $V_{SS} = COM$ ,  $DT = V_{SS}$  and  $T_A = 25^\circ\text{C}$  unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}/COM$  and are applicable to the respective input leads: HIN and LIN. The  $V_O$ ,  $I_O$  and  $R_{on}$  parameters are referenced to COM and are applicable to the respective output leads: HO and LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage for HIN & logic "0" for $\overline{LIN}$	2.9	—	—	V	$V_{CC} = 10V \text{ to } 20V$
$V_{IL}$	Logic "0" input voltage for HIN & logic "1" for $\overline{LIN}$	—	—	0.8		$V_{CC} = 10V \text{ to } 20V$
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.8	1.4		$I_O = 20 \text{ mA}$
$V_{OL}$	Low level output voltage, $V_O$	—	0.3	0.6		$I_O = 20 \text{ mA}$
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu\text{A}$	$V_B = V_S = 600V$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	20	75	130	$\mu\text{A}$	$V_{IN} = 0V \text{ or } 5V$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	0.4	1.0	1.6	mA	$V_{IN} = 0V \text{ or } 5V$ RDT=0
$I_{IN+}$	Logic "1" input bias current	—	5	20	$\mu\text{A}$	$HIN = 5V, \overline{LIN} = 0V$
$I_{IN-}$	Logic "0" input bias current	—	—	2		$HIN = 0V, \overline{LIN} = 5V$
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold	8.0	8.9	9.8	V	
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9.0		
$V_{CCUVH}$ $V_{BSUVH}$	Hysteresis	0.3	0.7	—		
$I_{O+}$	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V,$ $PW \leq 10 \mu\text{s}$
$I_{O-}$	Output low short circuit pulsed current	250	350	—		$V_O = 15V,$ $PW \leq 10 \mu\text{s}$