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May 2016

# FDMD8560L

## Dual N-Channel PowerTrench® MOSFET

### Q1: 60 V, 22 A, 3.2 mΩ  Q2: 60 V, 22 A, 3.2 mΩ

### Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 3.2 mΩ at $V_{GS}$ = 10 V, $I_D$ = 22 A
- Max $r_{DS(on)}$ = 5.4 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 18 A

Q2: N-Channel

- Max $r_{DS(on)}$ = 3.2 mΩ at $V_{GS}$ = 10 V, $I_D$ = 22 A
- Max $r_{DS(on)}$ = 5.4 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 18 A
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- RoHS Compliant

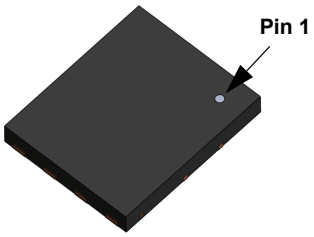
### General Description

This device includes two 60V N-Channel MOSFETs in a dual power (5 mm X 6 mm) package. HS source and LS drain internally connected for half/full bridge, low source inductance package, low $r_{DS(on)}$/Qg FOM silicon.

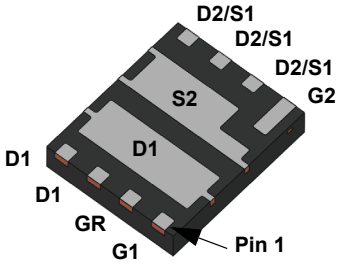
### Applications

- Synchronous Buck: Primary Switch of Half / Full Bridge Converter for Telecom
- Motor Bridge: Primary Switch of Half / Full Bridge Converter for BLDC Motor
- MV POL: 48V Synchronous Buck Switch
- Half/Full Bridge Secondary Synchronous Rectification

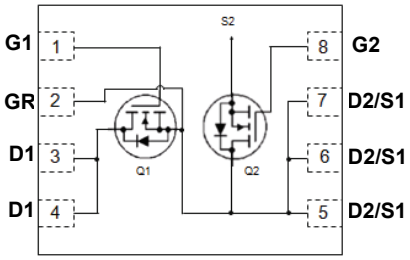
**Top**




**Bottom**




**Power 5 x 6**




## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted.

| Symbol | Parameter | | | Q1 | Q2 | Units |
|---|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 60 | 60 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | ±20 | V |
| $I_D$ | Drain Current -Continuous | $T_C$ = 25 °C | (Note 5) | 93 | 93 | A |
| | -Continuous | $T_C$ = 100 °C | (Note 5) | 59 | 59 | |
| | Drain Current -Continuous | $T_A$ = 25 °C | | 22[1a] | 22[1b] | |
| | -Pulsed | | (Note 4) | 550 | 550 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 384 | 384 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 48 | 48 | W |
| | Power Dissipation | $T_A$ = 25 °C | | 2.2[1a] | 2.2[1b] | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 2.6 | 2.6 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | 55[1a] | 55 [1b] | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMD8560L | FDMD8560L | Power 5 x 6 | 13 ” | 12 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted.

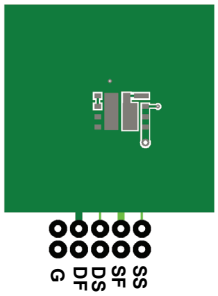
| Symbol | Parameter | Test Conditions | Type | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | Q1<br>Q2 | 60<br>60 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | Q1<br>Q2 | | 32<br>32 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V | Q1<br>Q2 | | | 1<br>1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | Q1<br>Q2 | | | ±100<br>±100 | nA |
| **On Characteristics** | | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | Q1<br>Q2 | 1.0<br>1.0 | 1.6<br>1.6 | 3.0<br>3.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | Q1<br>Q2 | | -7<br>-7 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 22 A | Q1 | | 2.5 | 3.2 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 18A | | | 4.1 | 5.4 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 22 A, $T_J$ = 125 °C | | | 3.9 | 5.0 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 22 A | Q2 | | 2.5 | 3.2 | |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 18 A | | | 4.1 | 5.4 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 22 A, $T_J$ = 125 °C | | | 3.9 | 5.0 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = 5 V, $I_D$ = 22 A | Q1<br>Q2 | | 98<br>98 | | S |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V<br>f = 1 MHz | Q1<br>Q2 | | 7420<br>7420 | 11130<br>11130 | pF |
| $C_{oss}$ | Output Capacitance | | Q1<br>Q2 | | 1110<br>1110 | 1665<br>1665 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | | 38<br>38 | 60<br>60 | pF |
| $R_g$ | Gate Resistance | | Q1<br>Q2 | 0.1<br>0.1 | 1.5<br>1.5 | 3.0<br>3.0 | Ω |
| **Switching Characteristics** | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 22 A<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 20<br>20 | 35<br>35 | ns |
| $t_r$ | Rise Time | | Q1<br>Q2 | | 15<br>15 | 26<br>26 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q1<br>Q2 | | 57<br>57 | 90<br>90 | ns |
| $t_f$ | Fall Time | | Q1<br>Q2 | | 11<br>11 | 20<br>20 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 30 V, $I_D$ =22 A | Q1<br>Q2 | | 92<br>92 | 128<br>128 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V; $V_{DD}$ = 30 V, $I_D$ =22 A | Q1<br>Q2 | | 42<br>42 | 59<br>59 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 30 V, $I_D$ =22 A | Q1<br>Q2 | | 19<br>19 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 30 V, $I_D$ =22 A | Q1<br>Q2 | | 7<br>7 | | nC |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted.

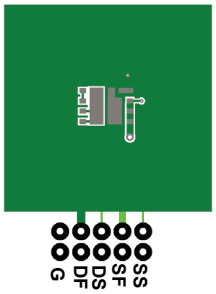
| Symbol | Parameter | Test Conditions | Type | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Drain-Source Diode Characteristics** | | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 22 A (Note 2) | Q1<br>Q2 | | 0.8<br>0.8 | 1.3<br>1.3 | V |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2 A (Note 2) | Q1<br>Q2 | | 0.7<br>0.7 | 1.2<br>1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 22 A, di/dt = 100 A/μs | Q1<br>Q2 | | 53<br>53 | 84<br>84 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | Q1<br>Q2 | | 44<br>44 | 70<br>70 | nC |

NOTES:

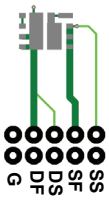
1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



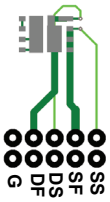

a. 55 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper




b. 55 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper




c. 155 °C/W when mounted on a minimum pad of 2 oz copper




d. 155 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Q1: $E_{AS}$ of 384 mJ is based on starting $T_J$ = 25 °C, L = 3 mH, $I_{AS}$ = 16 A, $V_{DD}$ = 60 V, $V_{GS}$ = 10 V. 100% tested at L = 0.1 mH, $I_{AS}$ = 51 A.
   Q2: $E_{AS}$ of 384 mJ is based on starting $T_J$ = 25 °C, L = 3 mH, $I_{AS}$ = 16 A, $V_{DD}$ = 60 V, $V_{GS}$ = 10 V. 100% tested at L = 0.1 mH, $I_{AS}$ = 51 A.
4. Pulsed Id please refer to Fig 11 and Fig 24 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25°C unless otherwise noted.

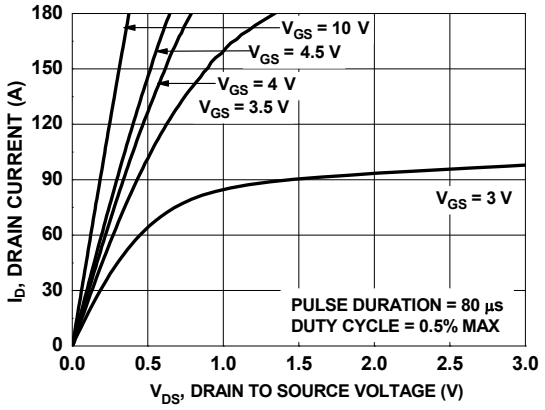



**Figure 1. On Region Characteristics**

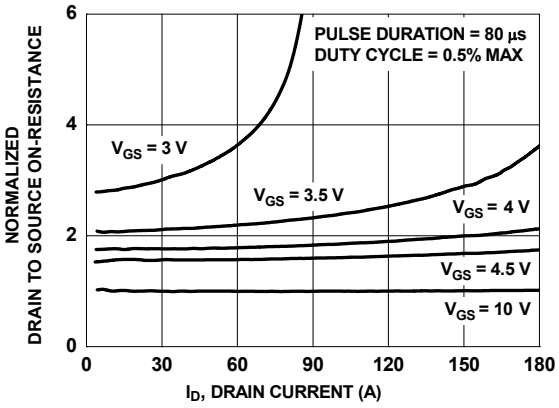



**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**

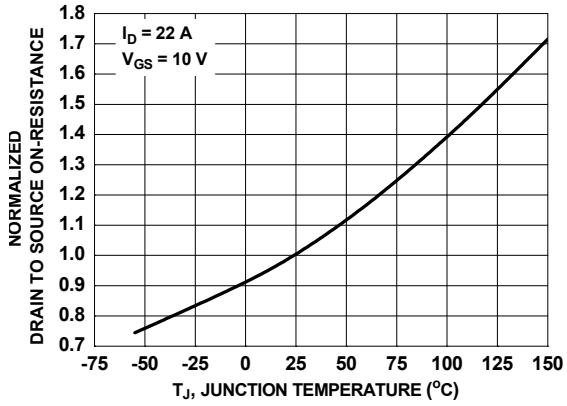



**Figure 3. Normalized On Resistance vs. Junction Temperature**

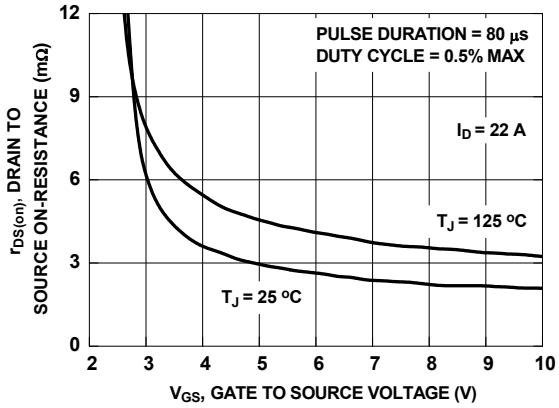



**Figure 4. On-Resistance vs. Gate to Source Voltage**

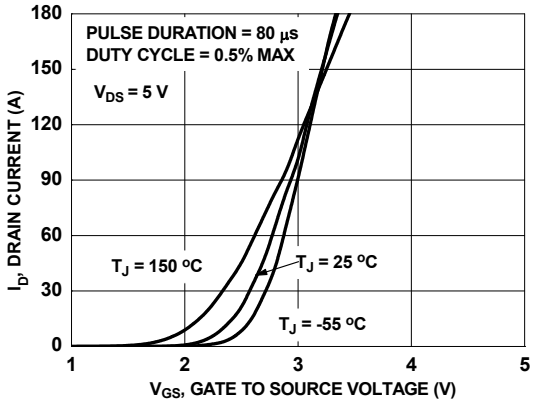



**Figure 5. Transfer Characteristics**

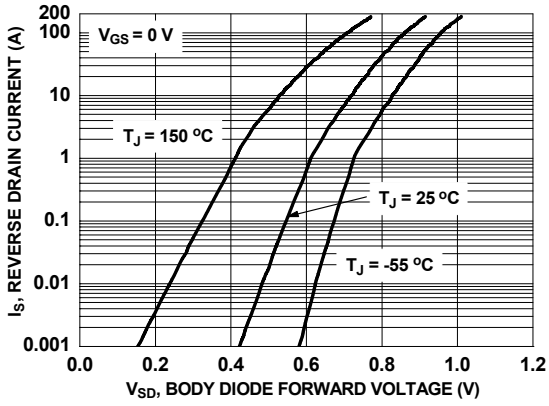



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25°C unless otherwise noted.

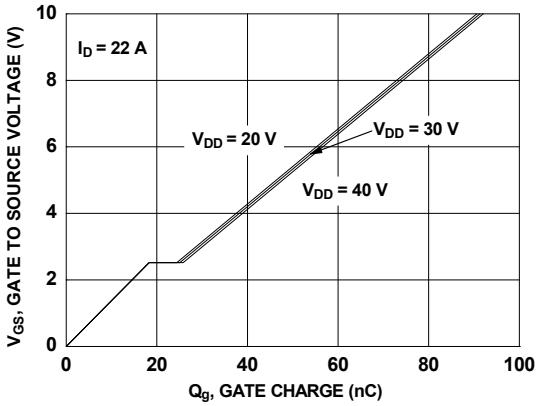



**Figure 7. Gate Charge Characteristics**

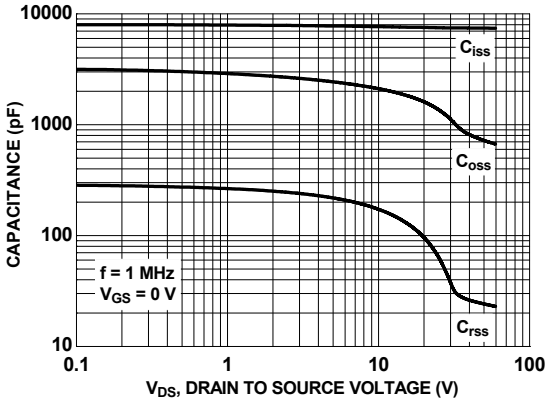



**Figure 8. Capacitance vs. Drain to Source Voltage**

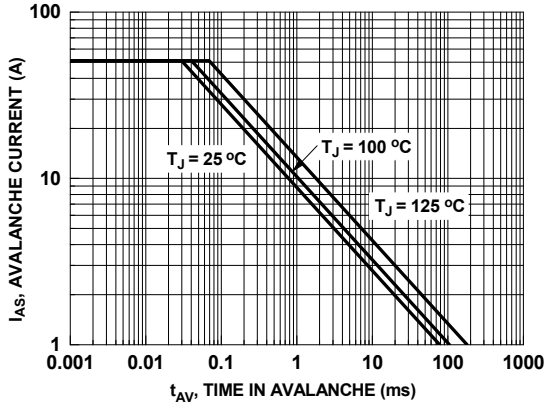



**Figure 9. Unclamped Inductive Switching Capability**

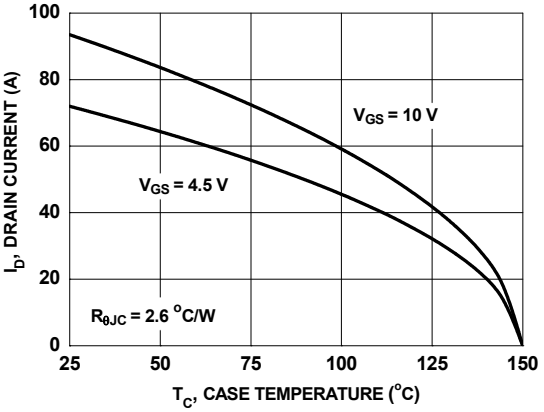



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

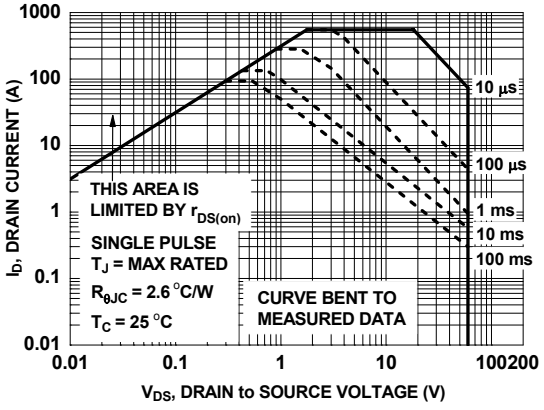



**Figure 11. Forward Bias Safe Operating Area**

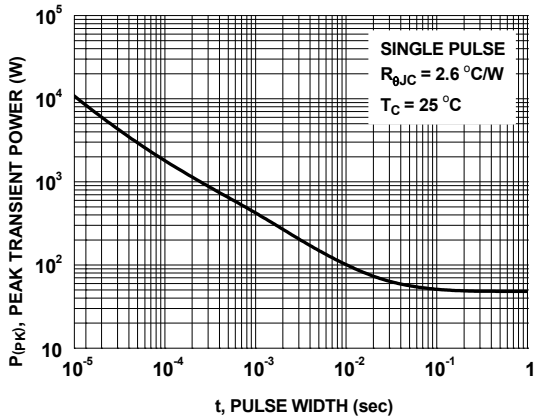



**Figure 12. Single Pulse Maximum Power Dissipation**

## Typical Characteristics (Q1 N-Channel) $T_J$ = 25°C unless otherwise noted.

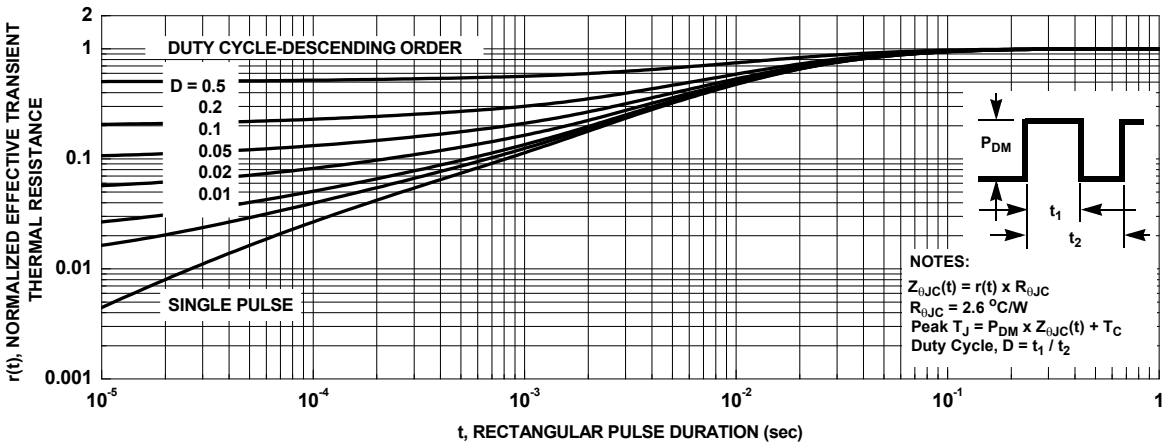



**Figure 13. Junction-to-Case Transient Thermal Response Curve**

## Typical Characteristics (Q2 N-Channel) $T_J$ = 25 °C unless otherwise noted.

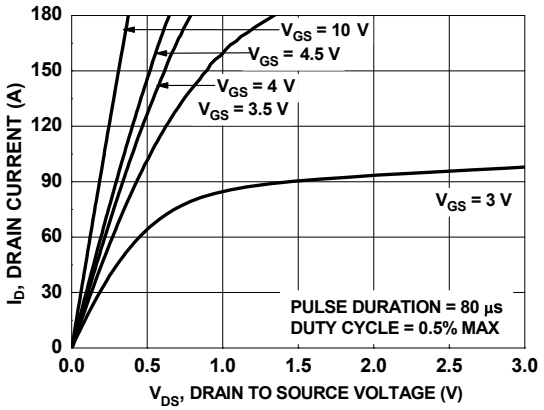



**Figure 14. On- Region Characteristics**

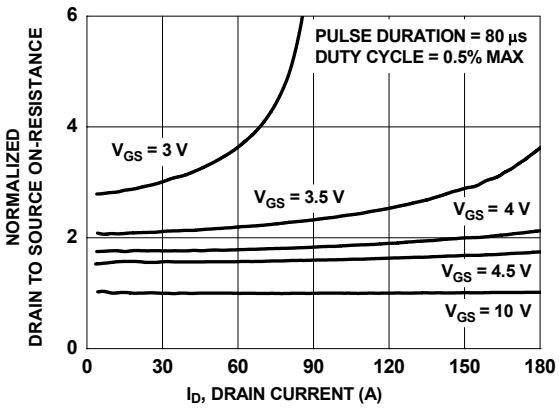



**Figure 15. Normalized on-Resistance vs. Drain Current and Gate Voltage**

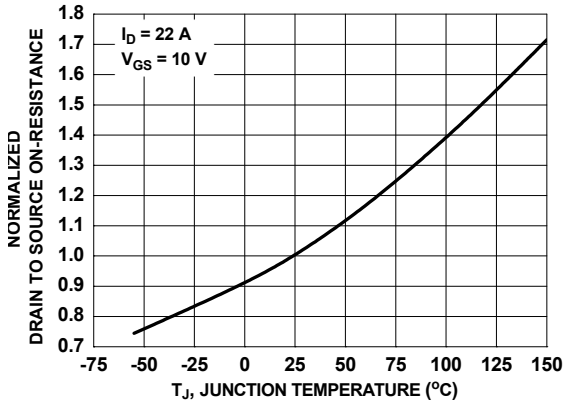



**Figure 16. Normalized On-Resistance vs. Junction Temperature**

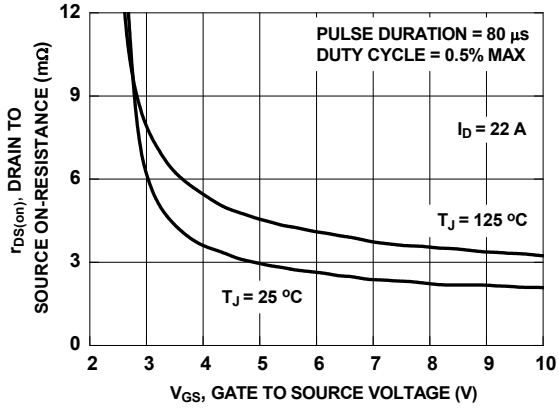



**Figure 17. On-Resistance vs. Gate to Source Voltage**

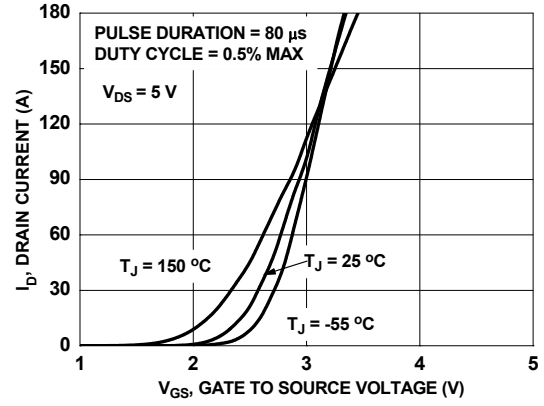



**Figure 18. Transfer Characteristics**

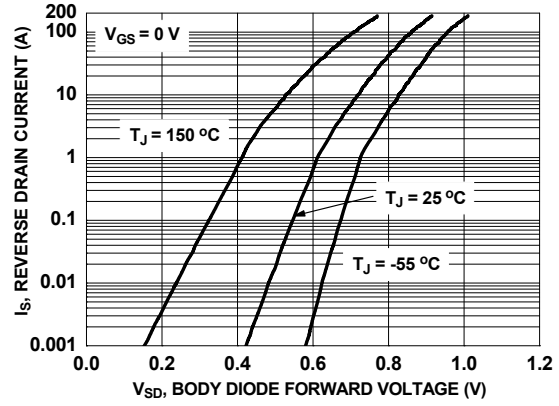



**Figure 19. Source to Drain Diode Forward Voltage vs. Source Current**

## Typical Characteristics (Q2 N-Channel) $T_J$ = 25°C unless otherwise noted.

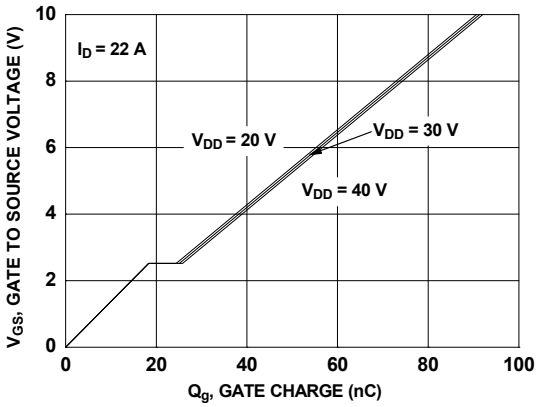



**Figure 20. Gate Charge Characteristics**

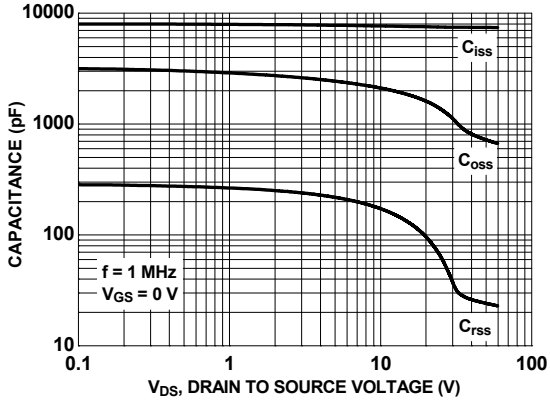



**Figure 21. Capacitance vs. Drain to Source Voltage**

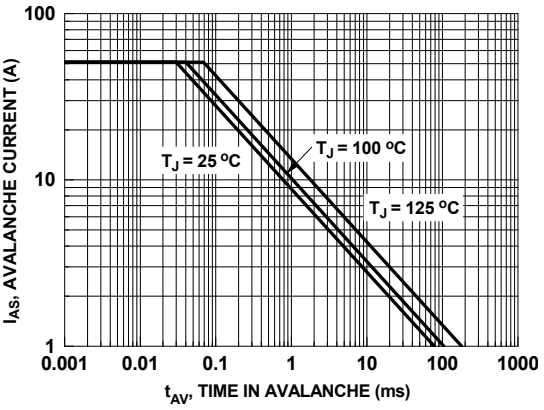



**Figure 22. Unclamped Inductive Switching Capability**

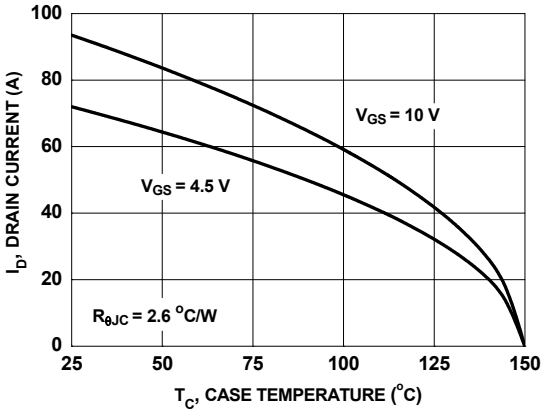



**Figure 23. Maximum Continuous Drain Current vs. Case Temperature**

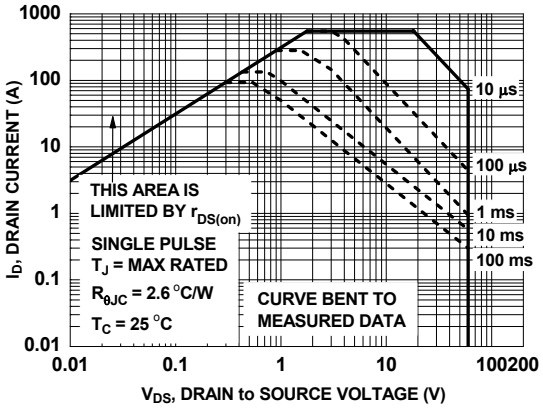



**Figure 24. Forward Bias Safe Operating Area**

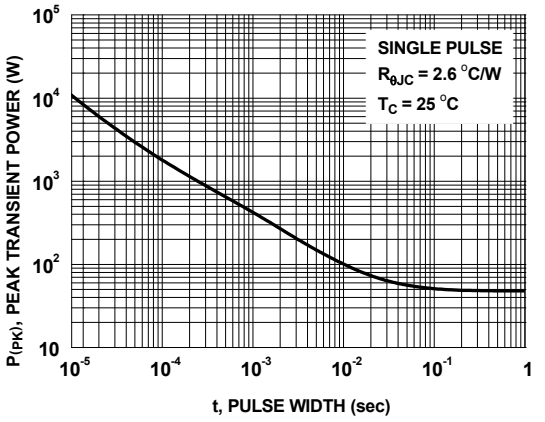



**Figure 25. Single Pulse Maximum Power Dissipation**

## Typical Characteristics (Q2 N-Channel) $T_J$ = 25 °C unless otherwise noted.

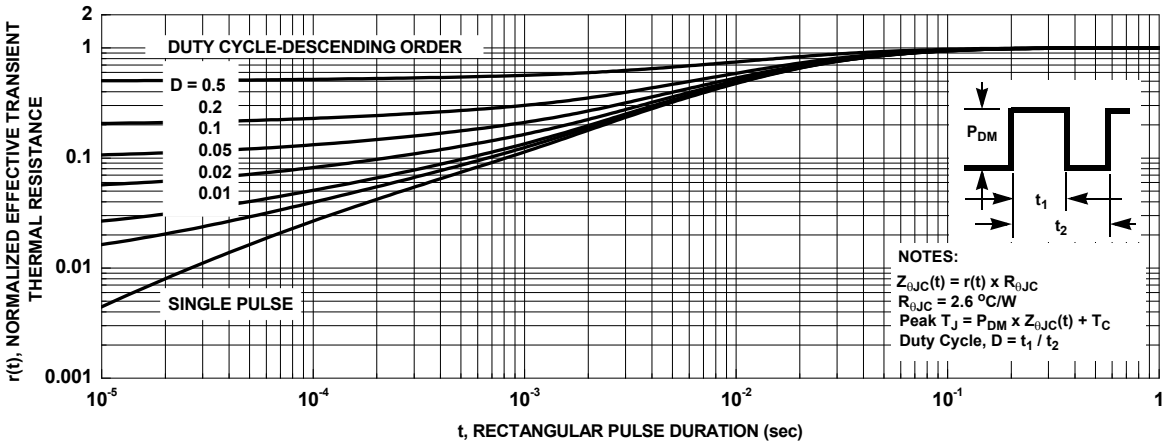
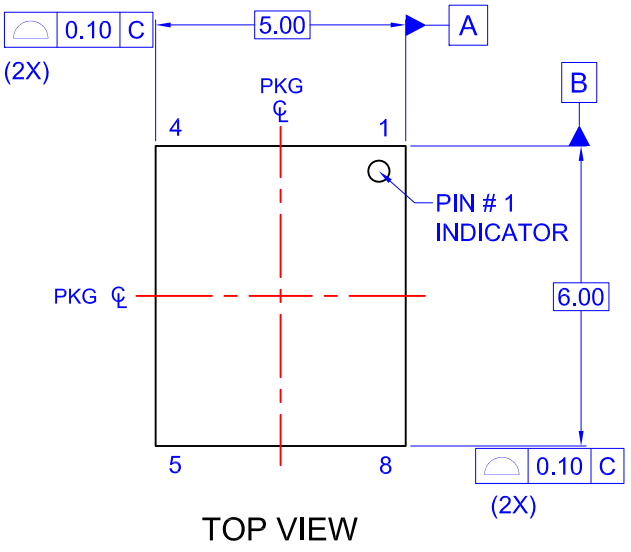
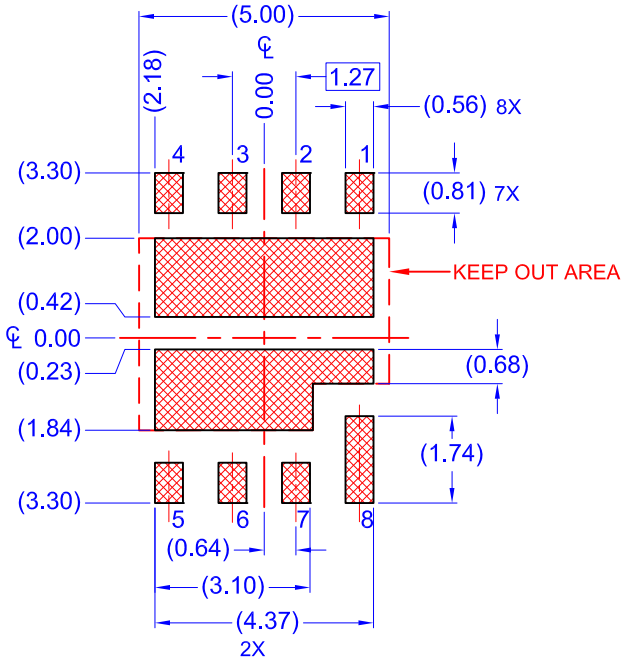


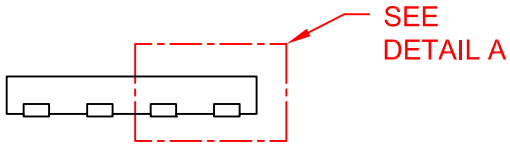

**Figure 26. Junction-to-Case Transient Thermal Response Curve**



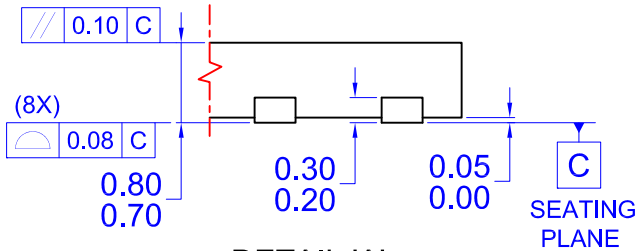

TOP VIEW



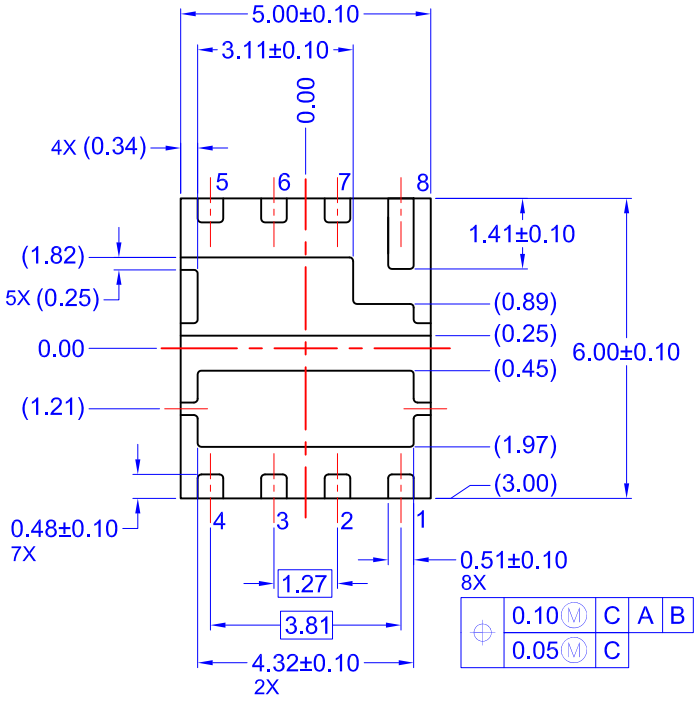

RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL 'A'
(SCALE: 2X)




BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC REGISTRATION, MO-240, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

F) DRAWING FILE NAME: MKT-PQFN08QREV2

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