



August 2015

FDC658AP

Single P-Channel Logic Level PowerTrench[®] MOSFET

-30V, -4A, 50mΩ

General Description

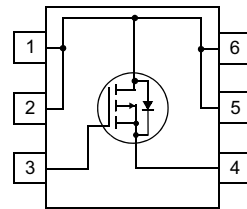
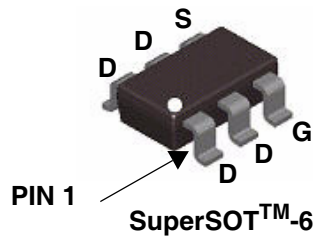
This P-Channel Logic Level MOSFET is produced using Fairchild's advanced PowerTrench process. It has been optimized for battery power management applications.

Applications

- Battery management
- Load switch
- Battery protection
- DC/DC conversion

Features

- Max $r_{DS(on)}$ = 50 mΩ @ $V_{GS} = -10$ V, $I_D = -4$ A
- Max $r_{DS(on)}$ = 75 mΩ @ $V_{GS} = -4.5$ V, $I_D = -3.4$ A
- Low Gate Charge
- High performance trench technology for extremely low $r_{DS(on)}$
- RoHS Compliant



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Drain Current - Continuous (Note 1a)	-4	A
	- Pulsed	-20	
P_D	Maximum Power dissipation (Note 1a)	1.6	W
	(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	30	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.58A	FDC658AP	7inch	8mm	3000 units

FDC658AP Single P-Channel Logic Level PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, Referenced to 25°C		-22		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{V}, V_{DS} = -24\text{V}$			-1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, Referenced to 25°C		4		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain-Source On-Resistance	$I_D = -4\text{A}, V_{GS} = -10\text{V}$		44	50	m Ω
		$I_D = -3.4\text{A}, V_{GS} = -4.5\text{V}$		67	75	
		$I_D = -4\text{A}, V_{GS} = -10\text{V}$, $T_J = 125^\circ\text{C}$		60	70	
$I_{D(ON)}$	On-State Drain Current	$V_{GS} = -10\text{V}, V_{DS} = -5\text{V}$	-20			A
g_{FS}	Forward Transconductance	$I_D = -4\text{A}, V_{DS} = -5\text{V}$		8.4		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$, $f = 1\text{MHz}$		470	660	pF
C_{oss}	Output Capacitance			126	180	pF
C_{rss}	Reverse Transfer Capacitance			61	85	pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{V}, I_D = -1\text{A}$, $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		7	14	ns
t_r	Turn-On Rise Time			12	22	ns
$t_{d(off)}$	Turn-Off Delay Time			16	29	ns
t_f	Turn-Off Fall Time			6	12	ns
Q_g	Total Gate Charge			6	8.1	nC
Q_{gs}	Gate-Source Charge	$V_{DS} = -15\text{V}, I_D = -4\text{A}$, $V_{GS} = -5\text{V}$		2.1		nC
Q_{gd}	Gate-Drain Charge			2		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current			-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -1.3\text{A}$ (Note 2)	-0.77	-1.2	V

Notes:

1: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 156°C/W when mounted on a minimum pad of 2 oz copper

Scale 1: 1 on letter size paper

2: Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

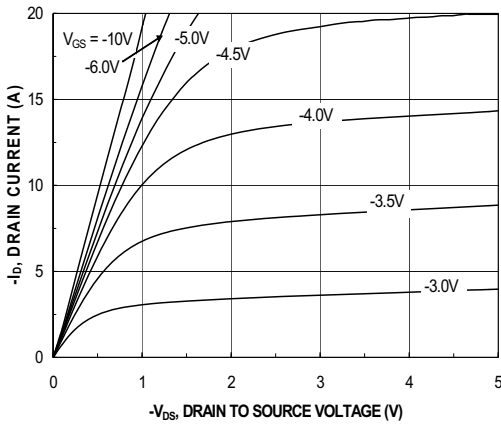


Figure 1. On-Region Characteristics

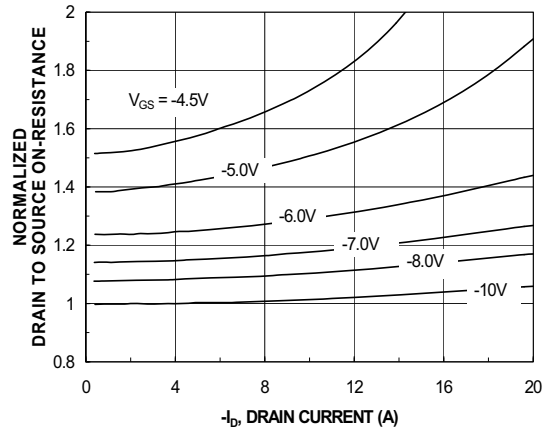


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

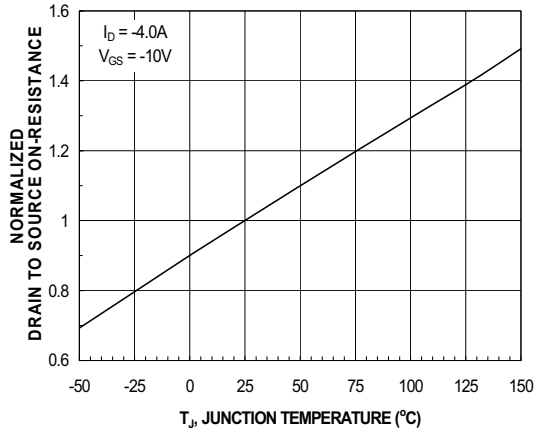


Figure 3. Normalized On-Resistance vs Junction Temperature

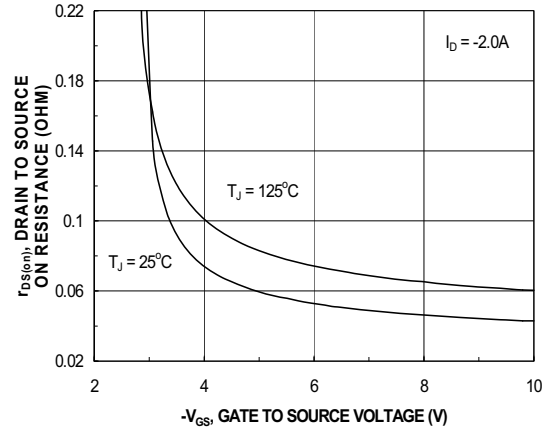


Figure 4. On-Resistance vs Gate to Source Voltage

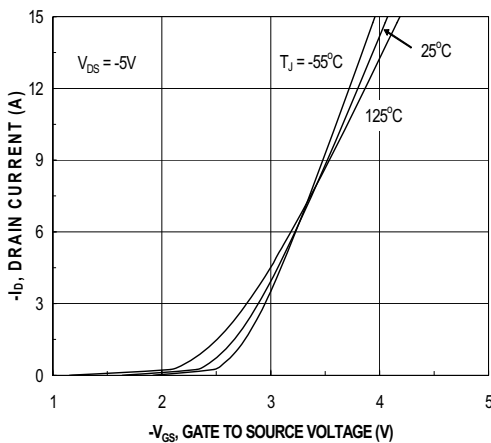


Figure 5. Transfer Characteristics

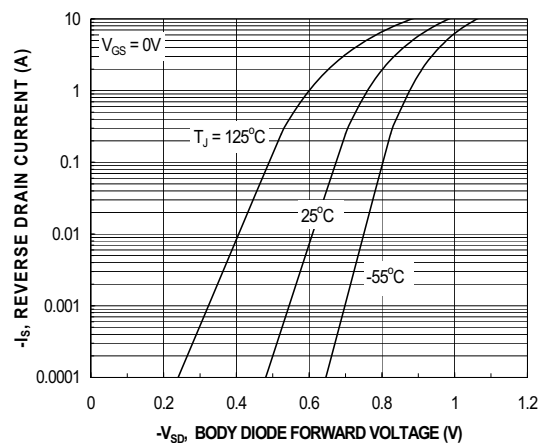


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

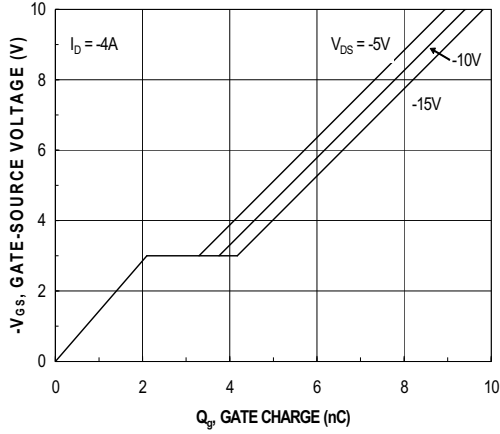


Figure 7. Gate Charge Characteristics

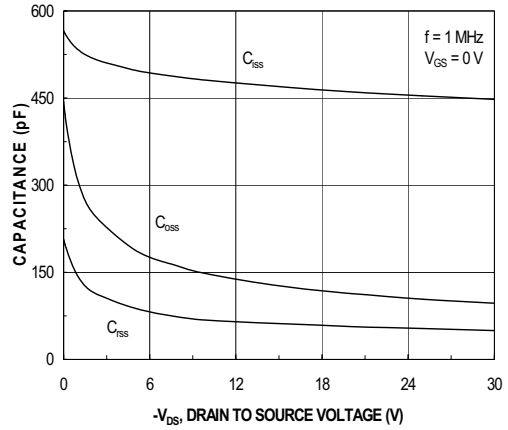


Figure 8. Capacitance vs Drain to Source Voltage

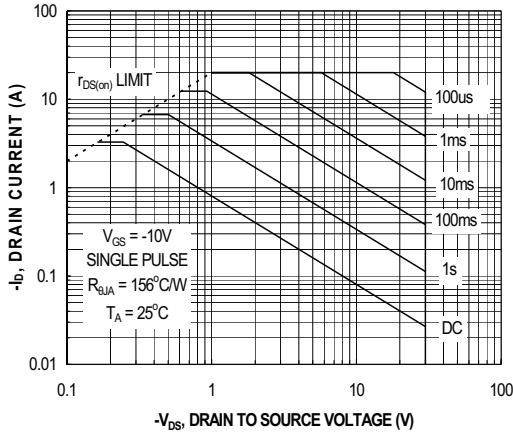


Figure 9. Forward Bias Safe Operating Area

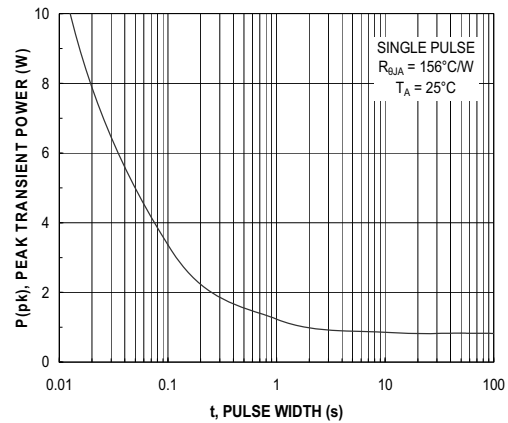


Figure 10. Single Pulse Maximum Power Dissipation

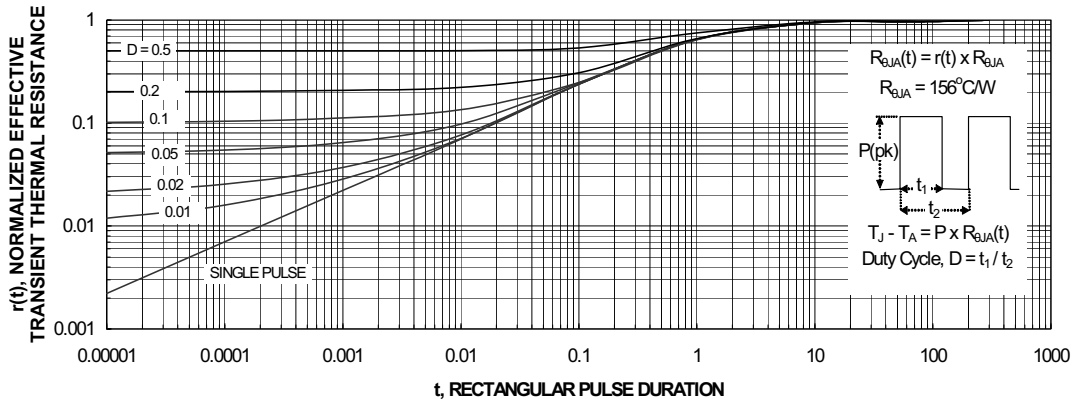
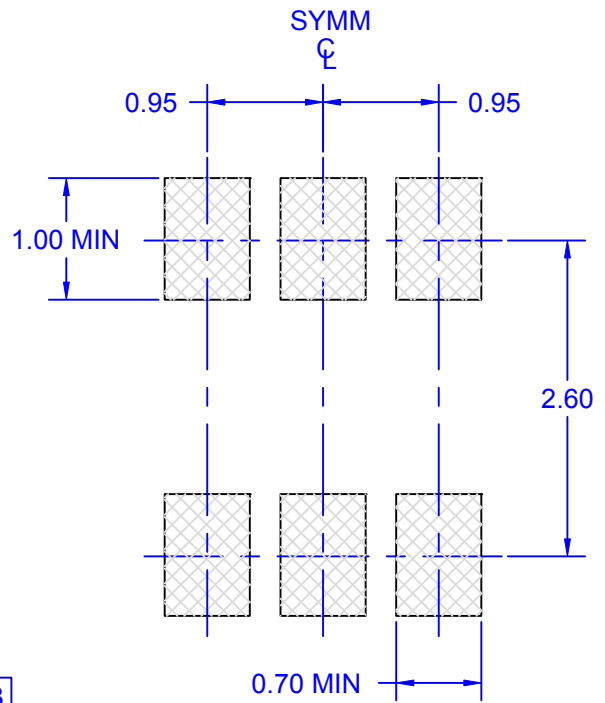
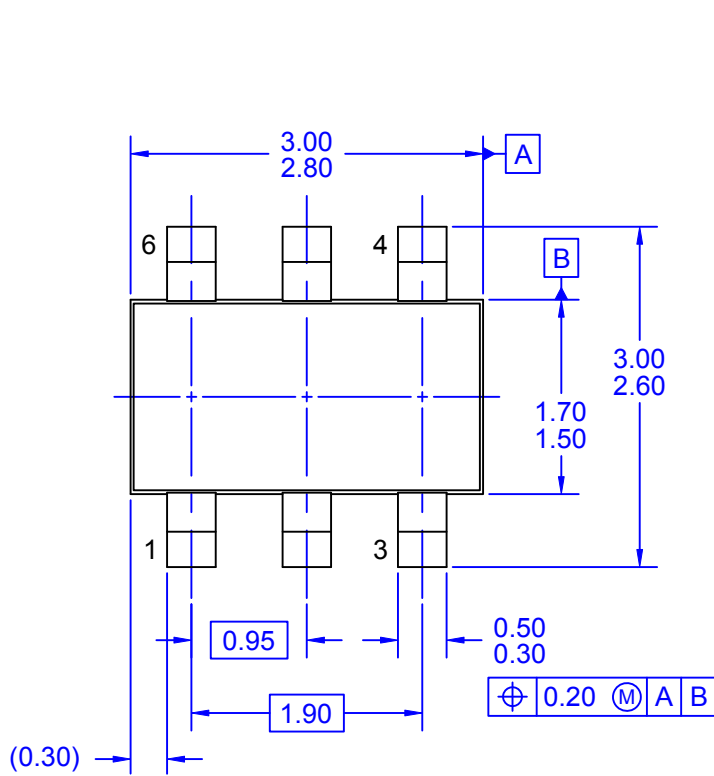
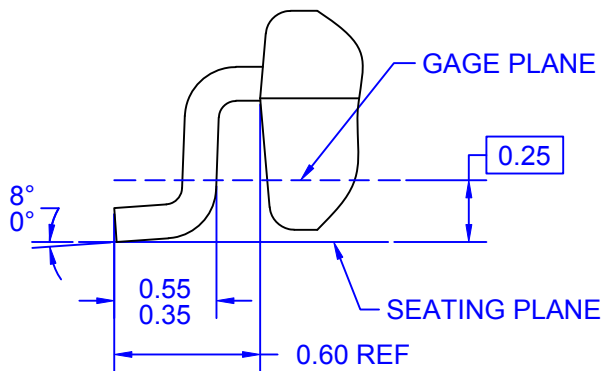
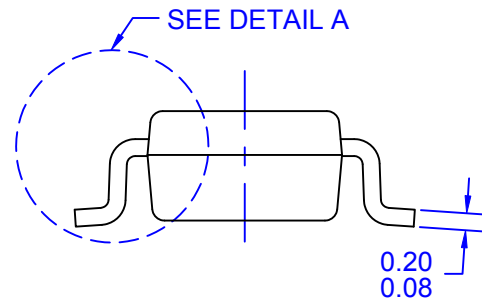
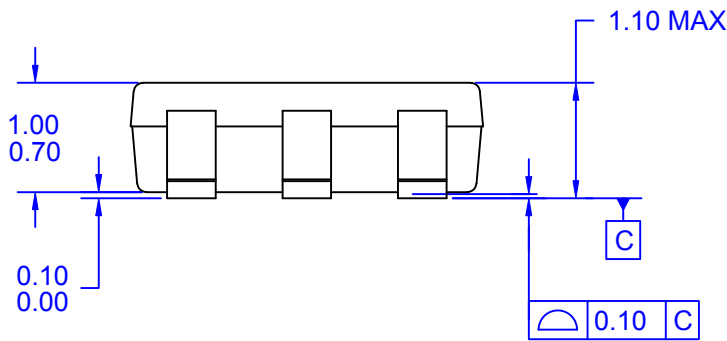


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



LAND PATTERN RECOMMENDATION



DETAIL A
SCALE: 50X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MO-193. VAR. AA, ISSUE C, DATED JANUARY 2000.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
 - D) DRAWING FILE NAME: MKT-MA06AREV5





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