1. Stratix III Device Family Overview

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Introduction

The Stratix® III family provides the most architecturally advanced, high performance, low power FPGAs in the marketplace.

Stratix III FPGAs lower power consumption through Altera's innovative Programmable Power Technology, which provides the ability to turn on the performance where needed and turn down the power consumption for blocks not in use. Selectable Core Voltage and the latest in silicon process optimizations are also employed to deliver the industry's lowest power, high performance FPGAs.

Specifically designed for ease of use and rapid system integration, the Stratix III FPGA family offers two family variants optimized to meet different application needs:

- The Stratix III *L* family provides balanced logic, memory, and multiplier ratios for mainstream applications.
- The Stratix III *E* family is memory and multiplier rich for data-centric applications.

Modular I/O banks with a common bank structure for vertical migration lend efficiency and flexibility to the high speed I/O. Package and die enhancements with dynamic on-chip termination, output delay, and current strength control provide best-in-class signal integrity.

Based on a 1.1-V, 65-nm all-layer copper SRAM process, the Stratix III family is a programmable alternative to custom ASICs and programmable processors for high performance logic, digital signal processing (DSP), and embedded designs.

Stratix III devices include optional configuration bit stream security through volatile or non-volatile 256-bit Advanced Encryption Standard (AES) encryption. Where ultra-high reliability is required, Stratix III devices include automatic error detection circuitry to detect data corruption by soft errors in the configuration random-access memory (CRAM) and user memory cells.

Features

Stratix III devices offer the following features:

- 48,000 to 338,000 equivalent logic elements (LEs); see Table 1–1
- 2,430 to 20,497 Kbits of enhanced TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of 9×9, 12×12, 18×18, and 36×36 multipliers (at up to 550 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- I/O:GND:PWR ratio of 8:1:1 along with on-die and on-package decoupling for robust signal integrity

- Programmable Power Technology, which minimizes power while maximizing device performance
- Selectable Core Voltage, available in low-voltage devices (L ordering code suffix), enables selection of lowest power or highest performance operation
- Up to 16 global clocks, 88 regional clocks, and 116 peripheral clocks per device
- Up to 12 phase-locked loops (PLLs) per device that support PLL reconfiguration, clock switchover, programmable bandwidth, clock synthesis, and dynamic phase shifting
- Memory interface support with dedicated DQS logic on all I/O banks
- Support for high-speed external memory interfaces including DDR, DDR2, DDR3 SDRAM, RLDRAM II, QDR II, and QDR II+ SRAM on up to 24 modular I/O banks
- Up to 1,104 user I/O pins arranged in 24 modular I/O banks that support a wide range of industry I/O standards
- Dynamic On-Chip Termination (OCT) with auto calibration support on all I/O banks
- High-speed differential I/O support with serializer/deserializer (SERDES) and dynamic phase alignment (DPA) circuitry for 1.25 Gbps performance
- Support for high-speed networking and communications bus standards including SPI-4.2, SFI-4, SGMII, Utopia IV, 10 Gigabit Ethernet XSBI, Rapid I/O and NPSI
- The only high-density, high-performance FPGA with support for 256-bit (AES) volatile and non-volatile security key to protect designs
- Robust on-chip hot socketing and power sequencing support
- Integrated cyclical redundancy check (CRC) for configuration memory error detection with critical error determination for high availability systems support
- Built-in error correction coding (ECC) circuitry to detect and correct data errors in M144K TriMatrix memory blocks
- Nios® II embedded processor support
- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP)

Table 1–1 lists the Stratix III FPGA family features.

Table 1–1. Stratix III FPGA Family Features

	Device/ Feature	ALMs	LEs	M9K Blocks	M144K Blocks	MLAB Blocks	Total Embedded RAM Kbits	MLAB RAM Kbits *(2)*	Total RAM Kbits *(3)*	18×18-bit Multipliers (FIR Mode)	PLLs *(4)*
Stratix III Logic Family	EP3SL50	19K	47.5K	108	6	950	1,836	297	2,133	216	4
	EP3SL70	27K	67.5K	150	6	1,350	2,214	422	2,636	288	4
	EP3SL110	43K	107.5K	275	12	2,150	4,203	672	4,875	288	8
	EP3SL150	57K	142.5K	355	16	2,850	5,499	891	6,390	384	8
	EP3SL200	80K	200K	468	36	4,000	9,396	1,250	10,646	576	12
	EP3SE260	102K	255K	864	48	5,100	14,688	1,594	16,282	768	12
	EP3SL340	135K	337.5K	1,040	48	6,750	16,272	2,109	18,381	576	12
Stratix III Enhanced Family	EP3SE50	19K	47.5K	400	12	950	5,328	297	5,625	384	4
	EP3SE80	32K	80K	495	12	1,600	6,183	500	6,683	672	8
	EP3SE110	43K	107.5K	639	16	2,150	8,055	672	8,727	896	8
	EP3SE260 *(1)*	102K	255K	864	48	5,100	14,688	1,594	16,282	768	12

Notes to Table 1–1:

(1) The EP3SE260 device is rich in LE, memory, and multiplier resources. Therefore, it aligns with both logic (*L*) and enhanced (*E*) variants.

(2) MLAB ROM mode support twice of MLAB RAM Kbits.

(3) For total ROM Kbits, please use this equation to calculate:
Total ROM Kbits = Total Embedded RAM Kbits + [(# of MLAB blocks × 640)/1024]

(4) The availability of the PLL shown in this column is based on the device with the largest package. Refer to *Clock Networks and PLLs in Stratix III Device* chapter in volume 1 of the Stratix III Device Handbook for the availability of the PLL for each device.

The Stratix III logic family (*L*) offers balanced logic, memory, and multipliers to address a wide range of applications, while the enhanced family (*E*) offers more memory and multipliers per logic and is ideal for wireless, medical imaging, and military applications.

Stratix III devices are available in space-saving FineLine BGA packages (see Table 1–2 and Table 1–3).

Table 1–2 lists the Stratix III FPGA package options and I/O pin counts.

Table 1–2. Package Options and I/O Pin Counts *(Note 1)* (Part 1 of 2)

Device	484-Pin FineLine BGA *(2)*	780-Pin FineLine BGA *(2)*	1152-Pin FineLine BGA *(2)*	1517-Pin FineLine BGA *(3)*	1760-Pin FineLine BGA *(3)*
EP3SL50	296	488	—	—	—
EP3SL70	296	488	—	—	—
EP3SL110	—	488	744	—	—
EP3SL150	—	488	744	—	—
EP3SL200	—	488 *(5)*	744	976	—
EP3SL340	—	—	744 *(4)*	976	1,120
EP3SE50	296	488	—	—	—
EP3SE80	—	488	744	—	—

Table 1–2. Package Options and I/O Pin Counts *(Note 1)* (Part 2 of 2)

Device	484-Pin FineLine BGA *(2)*	780-Pin FineLine BGA *(2)*	1152-Pin FineLine BGA *(2)*	1517-Pin FineLine BGA *(3)*	1760-Pin FineLine BGA *(3)*
EP3SE110	—	488	744	—	—
EP3SE260	—	488 *(5)*	744	976	—

Notes to Table 1–2:

(1) The arrows indicate vertical migration.

(2) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p` and `CLK10n`) that can be used for data inputs.

(3) All I/O pin counts include eight dedicated clock inputs (`CLK1p`, `CLK1n`, `CLK3p`, `CLK3n`, `CLK8p`, `CLK8n`, `CLK10p`, and `CLK10n`) and eight dedicated corner PLL clock inputs (`PLL_L1_CLKp`, `PLL_L1_CLKn`, `PLL_L4_CLKp`, `PLL_L4_CLKn`, `PLL_R4_CLKp`, `PLL_R4_CLKn`, `PLL_R1_CLKp`, and `PLL_R1_CLKn`) that can be used for data inputs.

(4) The EP3SL340 FPGA is offered only in the H1152 package, but not offered in the F1152 package.

(5) The EP3SE260 and EP3SL200 FPGAs are offered only in the H780 package, but not offered in the F780 package.

All Stratix III devices support vertical migration within the same package (for example, you can migrate between the EP3SL50 and EP3SL70 devices in the 780-pin FineLine BGA package). Vertical migration allows you to migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus® II software (Assignments menu > Device > Migration Devices). You can migrate from the *L* family to the *E* family without increasing the number of LEs available. This minimizes the cost of vertical migration.

Table 1–3 lists the Stratix III FBGA package sizes.

Table 1–3. FineLine BGA Package Sizes

Dimension	484 Pin	780 Pin	1152 Pin	1517 Pin	1760 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00
Area (mm^2)	529	841	1,225	1,600	1,849
Length/Width (mm/mm)	23/23	29/29	35/35	40/40	43/43

Table 1–4 lists the Stratix III HBGA package sizes.

Table 1–4. Hybrid FineLine BGA Package Sizes

Dimension	780 Pin	1152 Pin
Pitch (mm)	1.00	1.00
Area (mm^2)	1,089	1,600
Length/Width (mm/mm)	33/33	40/40

Stratix III devices are available in up to three speed grades: –2, –3, and –4, with –2 being the fastest. Stratix III devices are offered in both commercial and industrial temperature range ratings with leaded and lead-free packages. Selectable Core Voltage is available in specially marked low-voltage devices (*L* ordering code suffix).

Table 1–5 lists the Stratix III device speed grades.

Table 1–5. Stratix III Device Speed Grades

Device	Temperature Grade	484 -Pin FineLine BGA	780-Pin FineLine BGA	780-Pin Hybrid FineLine BGA	1152-Pin FineLine BGA	1152-Pin Hybrid FineLine BGA	1517-Pin FineLine BGA	1760-Pin FineLine BGA
EP3SL50	Commercial	–2, –3, –4, –4L	–2, –3,–4, –4L	—	—	—	—	—
	Industrial	–3, –4, –4L	–3, –4, –4L	—	—	—	—	—
EP3SL70	Commercial	–2, –3, –4, –4L	–2, –3, –4, –4L	—	—	—	—	—
	Industrial	–3, –4, –4L	–3, –4, –4L	—	—	—	—	—
EP3SL110	Commercial	—	–2, –3, –4, –4L	—	–2, –3, –4, –4L	—	—	—
	Industrial	—	–3, –4, –4L	—	–3, –4, –4L	—	—	—
EP3SL150	Commercial	—	–2,–3, –4, –4L	—	–2, –3, –4, –4L	—	—	—
	Industrial	—	–3, –4, –4L	—	–3, –4, –4L	—	—	—
EP3SL200	Commercial	—	—	–2,–3, –4, –4L	–2,–3, –4, –4L	—	–2,–3, –4, –4L	—
	Industrial *(1)*	—	—	–3, –4, –4L	–3, –4, –4L	—	–3, –4, –4L	—
EP3SL340	Commercial	—	—	—	—	–2, –3, –4	–2, –3, –4	–2, –3, –4
	Industrial *(1)*	—	—	—	—	–3, –4, –4L	–3, –4, –4L	–3, –4, –4L
EP3SE50	Commercial	–2, –3, –4, –4L	–2, –3, –4, –4L	—	—	—	—	—
	Industrial	–3, –4, –4L	–3, –4, –4L	—	—	—	—	—
EP3SE80	Commercial	—	–2, –3, –4, –4L	—	–2, –3, –4, –4L	—	—	—
	Industrial	—	–3, –4, –4L	—	–3, –4, –4L	—	—	—
EP3SE110	Commercial	—	–2,–3, –4, –4L	—	–2, –3, –4, –4L	—	—	—
	Industrial	—	–3, –4, –4L	—	–3, –4, –4L	—	—	—
EP3SE260	Commercial	—	—	–2, –3, –4, –4L	–2,– 3, –4, –4L	—	–2, –3, –4, –4L	—
	Industrial *(1)*	—	—	–3, –4, –4L	–3, –4, –4L	—	–3, –4,–4L	—

Note to Table 1–5:

(1) For EP3SL340, EP3SL200, and EP3SE260, the industrial junction temperature range for –4L is 0–100°C, regardless of supply voltage.

Architecture Features

The following section briefly describes the various features of the Stratix III family of FPGAs.

Logic Array Blocks and Adaptive Logic Modules

The Logic Array Block (LAB) is composed of basic building blocks known as Adaptive Logic Modules (ALMs) that can be configured to implement logic, arithmetic, and register functions. Each LAB consists of ten ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. ALMs are part of a unique, innovative logic structure that delivers faster performance, minimizes area, and reduces power consumption. ALMs expand the traditional 4-input look-up table architecture to 7 inputs, increasing performance by reducing LEs, logic levels, and associated routing. In addition, ALMs maximize DSP performance with dedicated functionality to efficiently implement adder trees and other complex arithmetic functions. The Quartus II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency.

The LAB of Stratix III has a new derivative called Memory LAB (or MLAB), which adds SRAM memory capability to the LAB. MLAB is a superset of the LAB and includes all LAB features. MLABs support a maximum of 320-bits of simple dual-port Static Random Access Memory (SRAM). Each ALM in an MLAB can be configured as a 16×2 block, resulting in a configuration of 16×20 simple dual port SRAM block. MLAB and LAB blocks always co-exist as pairs in all Stratix III families, allowing up to 50% of the logic (LABs) to be traded for memory (MLABs).

For more information about LABs and ALMs, refer to the *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices* chapter in *volume 1* of the *Stratix III Device Handbook*.

For more information about MLAB modes, features and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in *volume 1* of the *Stratix III Device Handbook*.

MultiTrack Interconnect

In the Stratix III architecture, connections between ALMs, TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities. The MultiTrack interconnect provides 1-hop connection to 34 adjacent LABs, 2-hop connections to 96 adjacent LABs and 3-hop connections to 160 adjacent LABs.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the reoptimization cycles that typically follow design changes and additions. The Quartus II Compiler also automatically places critical design paths on faster interconnects to improve design performance.

For more information, refer to the *MultiTrack Interconnect in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

TriMatrix Embedded Memory Blocks

TriMatrix embedded memory blocks provide three different sizes of embedded SRAM to efficiently address the needs of Stratix III FPGA designs. TriMatrix memory includes the following blocks:

- 320-bit MLAB blocks optimized to implement filter delay lines, small FIFO buffers, and shift registers
- 9-Kbit M9K blocks that can be used for general purpose memory applications
- 144-Kbit M144K blocks that are ideal for processor code storage, packet and video frame buffering

Each embedded memory block can be independently configured to be a single- or dual-port RAM, ROM, or shift register via the Quartus II MegaWizard®. Multiple blocks of the same type can also be stitched together to produce larger memories with minimal timing penalty. TriMatrix memory provides up to 16,272 Kbits of embedded SRAM at up to 600 MHz operation.

For more information about TriMatrix memory blocks, modes, features, and design considerations, refer to the *TriMatrix Embedded Memory Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

DSP Blocks

Stratix III devices have dedicated high-performance digital signal processing (DSP) blocks optimized for DSP applications requiring high data throughput. Stratix III devices provide you with the ability to implement various high performance DSP functions easily. Complex systems such as WiMAX, 3GPP WCDMA, CDMA2000, voice over Internet Protocol (VoIP), H.264 video compression, and high-definition television (HDTV) require high performance DSP blocks to process data. These system designs typically use DSP blocks to implement finite impulse response (FIR) filters, complex FIR filters, infinite impulse response (IIR) filters, fast Fourier transform (FFT) functions, and discrete cosine transform (DCT) functions.

Stratix III devices have up to 112 DSP blocks. The architectural highlights of the Stratix III DSP block are the following:

- High performance, power optimized, fully pipelined multiplication operations
- Native support for 9-bit, 12-bit, 18-bit, and 36-bit word lengths
- Native support for 18-bit complex multiplications
- Efficient support for floating point arithmetic formats (24-bit for Single Precision and 53-bit for Double Precision)
- Signed and unsigned input support
- Built-in addition, subtraction, and accumulation units to efficiently combine multiplication results
- Cascading 18-bit input bus to form tap-delay lines

- Cascading 44-bit output bus to propagate output results from one block to the next block
- Rich and flexible arithmetic rounding and saturation units
- Efficient barrel shifter support
- Loopback capability to support adaptive filtering

DSP block multipliers can optionally feed an adder/subtractor or accumulator in the block depending on user configuration. This option saves ALM routing resources and increases performance, because all connections and blocks are inside the DSP block. Additionally, the DSP Block input registers can efficiently implement shift registers for FIR filter applications, and the Stratix III DSP blocks support rounding and saturation. The Quartus II software includes megafunctions that control the mode of operation of the DSP blocks based on user parameter settings.

For more information, refer to the *DSP Blocks in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Clock Networks and PLLs

Stratix III devices provide dedicated Global Clock Networks (GCLKs), Regional Clock Networks (RCLKs), and Periphery Clock Networks (PCLKs). These clocks are organized into a hierarchical clock structure that provides up to 104 unique clock domains (16 GCLK + 88 RCLK) within the Stratix III device and allows for up to 38 (16 GCLK + 22 RCLK) unique GCLK/RCLK clock sources per device quadrant.

Stratix III delivers abundant PLL resources with up to 12 PLLs per device and up to 10 outputs per PLL. Every output can be independently programmed, creating a unique, customizable clock frequency with no fixed relation to any other input or output clock. Inherent jitter filtration and fine granularity control over multiply, divide ratios, and dynamic phase-shift reconfiguration provide the high-performance precision required in today's high-speed applications. Stratix III device PLLs are feature rich, supporting advanced capabilities such as clock switchover, reconfigurable phase shift, PLL reconfiguration, and reconfigurable bandwidth. PLLs can be used for general-purpose clock management supporting multiplication, phase shifting, and programmable duty cycle. Stratix III PLLs also support external feedback mode, spread-spectrum input clock tracking, and post-scale counter cascading.

For more information, refer to the *Clock Networks and PLLs in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

I/O Banks and I/O Structure

Stratix III devices contain up to 24 modular I/O banks, each of which contains 24, 32, 36, 40, or 48 I/Os. This modular bank structure improves pin efficiency and eases device migration. The I/O banks contain circuitry to support external memory interfaces at speeds up to 533 MHz and high-speed differential I/O interfaces meeting up to 1.25 Gbps performance. It also supports high-speed differential inputs and outputs running at speeds up to 800 MHz and 500 MHz, respectively.

Stratix III devices support a wide range of industry I/O standards, including single-ended, voltage referenced single-ended, and differential I/O standards. The Stratix III I/O supports programmable bus hold, programmable pull-up resistor, programmable slew rate, programmable drive strength, programmable output delay control, and open-drain output. Stratix III devices also support on-chip series (R_S) and on-chip parallel (R_T) termination with auto calibration for single-ended I/O standards and on-chip differential termination (R_D) for LVDS I/O standards on Left/Right I/O banks. Dynamic OCT is also supported on bi-directional I/O pins in all I/O banks.

For more information, refer to the *Stratix III Device I/O Features* chapter in volume 1 of the *Stratix III Device Handbook*.

External Memory Interfaces

The Stratix III I/O structure has been completely redesigned from the ground up to provide flexibility and enable high-performance support for existing and emerging external memory standards such as DDR, DDR2, DDR3, QDRII, QDRII+, and RLDRAMII at frequencies of up to 533 MHz.

Packed with features such as dynamic on-chip termination, trace mismatch compensation, read/write levelling, half-rate registers, and 4-to 36-bit programmable DQ group widths, Stratix III I/Os supply the built-in functionality required for rapid and robust implementation of external memory interfaces. Double data-rate support is found on all sides of the Stratix III device. Stratix III devices provide an efficient architecture to quickly and easily fit wide external memory interfaces exactly where you want them.

A self-calibrating soft IP core (ALTMEMPHY) optimized to take advantage of Stratix III device I/O, along with the new Quartus II timing analysis tool (TimeQuest), provide the total solution for the highest reliable frequency of operation across process voltage and temperature.

For more information about external memory interfaces, refer to the *External Memory Interfaces in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

High Speed Differential I/O Interfaces with DPA

Stratix III devices contain dedicated circuitry for supporting differential standards at speeds up to 1.25 Gbps. The high-speed differential I/O circuitry supports the following high speed I/O interconnect standards and applications: Utopia IV, SPI-4.2, SFI-4, 10 Gigabit Ethernet XSBI, Rapid I/O, and NPSI. Stratix III devices support 2×, 4×, 6×, 7×, 8×, and 10× SERDES modes for high speed differential I/O interfaces and 4×, 6×, 7×, 8×, and 10× SERDES modes when using the dedicated DPA circuitry. DPA minimizes bit errors, simplifies PCB layout and timing management for high-speed data transfer, and eliminates channel-to-channel and channel-to-clock skew in high-speed data transmission systems. Soft CDR can also be implemented, enabling low-cost 1.25-Gbps clock embedded serial links.

Stratix III devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmitter serializer

- Receiver deserializer
- Data realignment
- Dynamic phase aligner (DPA)
- Soft CDR functionality
- Synchronizer (FIFO buffer)
- PLLs

For more information, refer to the *High Speed Differential I/O Interfaces with DPA in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Hot Socketing and Power-On Reset

Stratix III devices are hot-socketing compliant. Hot socketing is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. Robust on-chip hot-socketing and power-sequencing support ensures proper device operation independent of the power-up sequence. You can insert or remove a Stratix III board in a system during system operation without causing undesirable effects to the running system bus or the board that was inserted into the system.

The hot-socketing feature also makes it easier to use Stratix III devices on PCBs that also contain a mixture of 3.3-V, 3.0-V, 2.5-V, 1.8-V, 1.5-V, and 1.2-V devices. With the Stratix III hot socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board.

For more information, refer to the *Hot Socketing and Power-On Reset in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Configuration

Stratix III devices are configured using one of the following four configuration schemes:

- Fast passive parallel (FPP)
- Fast active serial (AS)
- Passive serial (PS)
- Joint Test Action Group (JTAG)

All configuration schemes use either an external controller (for example, a MAX® II device or microprocessor), a configuration device, or a download cable.

Stratix III devices support configuration data decompression, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory and transmit this compressed bitstream to Stratix III devices. During configuration, the Stratix III device decompresses the bitstream in real time and programs its SRAM cells.

Stratix III devices support decompression in the FPP when using a MAX II device/microprocessor + flash, fast AS, and PS configuration schemes. The Stratix III decompression feature is not available in the FPP when using the enhanced configuration device and JTAG configuration schemes.

For more information, refer to the *Configuring Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Remote System Upgrades

Stratix III devices feature remote system upgrade capability, allowing error-free deployment of system upgrades from a remote location securely and reliably. Soft logic (either the Nios embedded processor or user logic) implemented in a Stratix III device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, and can recover from an error condition by reverting back to a safe configuration image, and provides error status information. This dedicated remote system upgrade circuitry is unique to Stratix series FPGAs and helps to avoid system downtime.

For more information, refer to the *Remote System Upgrades with Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

IEEE 1149.1 (JTAG) Boundary Scan Testing

Stratix III devices support the JTAG IEEE Std. 1149.1 specification. The Boundary-Scan Test (BST) architecture offers the capability to test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in the Stratix III device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. In addition to BST, you can use the IEEE Std. 1149.1 controller for Stratix III device in-circuit reconfiguration (ICR).

For more information, refer to the *IEEE 1149.1 (JTAG) Boundary Scan Testing in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Design Security

Stratix III devices are the only high-density, high-performance FPGAs with support for 256-bit volatile and non-volatile security keys to protect designs against copying, reverse engineering, and tampering. Stratix III devices have the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm, an industry standard encryption algorithm that is FIPS-197 certified and requires a 256-bit security key.

The design security feature is available when configuring Stratix III FPGAs using the fast passive parallel (FPP) configuration mode with an external host (such as a MAX II device or microprocessor), or when using fast active serial (AS) or passive serial (PS) configuration schemes.

For more information about the design security feature, refer to the *Design Security in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

SEU Mitigation

Stratix III devices have built-in error detection circuitry to detect data corruption due to soft errors in the configuration random-access memory (CRAM) cells. This feature allows all CRAM contents to be read and verified continuously during user mode operation to match a configuration-computed CRC value. The enhanced CRC circuit and frame-based configuration architecture allows detection and location of multiple, single, and adjacent bit errors which, in conjunction with a soft circuit supplied as a reference design, allows don't-care soft errors in the CRAM to be ignored during device operation. This provides a steep decrease in the effective soft error rate, increasing system reliability.

On-chip memory block SEU mitigation is also offered using the 9th bit and a configurable megafunction in the Quartus II software for MLAB and M9K blocks while the M144K memory blocks have built-in error correction code (ECC) circuitry.

For more information about the dedicated error detection circuitry, refer to the *SEU Mitigation in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*.

Programmable Power

Stratix III delivers Programmable Power, the only FPGA with user programmable power options balancing today's power and performance requirements. Stratix III devices utilize the most advanced power-saving techniques including a variety of process, circuit, and architecture optimizations and innovations. In addition, user controllable power reduction techniques provide an optimal balance of performance and power reduction specific for each design configured into the Stratix III FPGA. The Quartus II software (starting from version 6.1) automatically optimizes designs to meet the performance goals while simultaneously leveraging the programmable power-saving options available in the Stratix III FPGA without the need for any changes to the design flow.

For more information about Programmable Power in Stratix III devices, refer to the following documents:

- *Programmable Power and Temperature Sensing Diode in Stratix III Devices* chapter in volume 1 of the *Stratix III Device Handbook*
- *AN 437: Power Optimization in Stratix III FPGAs*
- *Stratix III Programmable Power White Paper*

Signal Integrity

Stratix III devices simplify the challenge of signal integrity through a number of chip, package, and board level enhancements to enable efficient high speed data transfer into and out of the device. These enhancements include:

- 8:1:1 user I/O/Gnd/V_{cc} ratio to reduce the loop inductance in the package
- Dedicated power supply for each I/O bank, limit of I/Os is 24 to 48 I/Os per bank, to help limit simultaneous switching noise
- Programmable slew-rate support with up to four settings to match desired I/O standard, control noise, and overshoot

- Programmable output-current drive strength support with up to six settings to match desired I/O standard performance
- Programmable output-delay support to control rise/fall times and adjust duty cycle, compensate for skew, and reduce simultaneous switching outputs (SSO) noise
- Dynamic OCT with auto calibration support for series and parallel OCT and differential OCT support for LVDS I/O standard on the left/right banks

For more information about SI support in Quartus II software, refer to the *Quartus II Handbook*.

Reference and Ordering Information

The following section describes Stratix III device software support and ordering information.

Software

Stratix III devices are supported by the Altera Quartus II design software, version 6.1 and later, which provides a comprehensive environment for system-on-a-programmable-chip (SOPC) design. The Quartus II software includes HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, SignalTap® II logic analyzer, and device configuration.

For more information about the Quartus II software features, refer to the *Quartus II Handbook*.

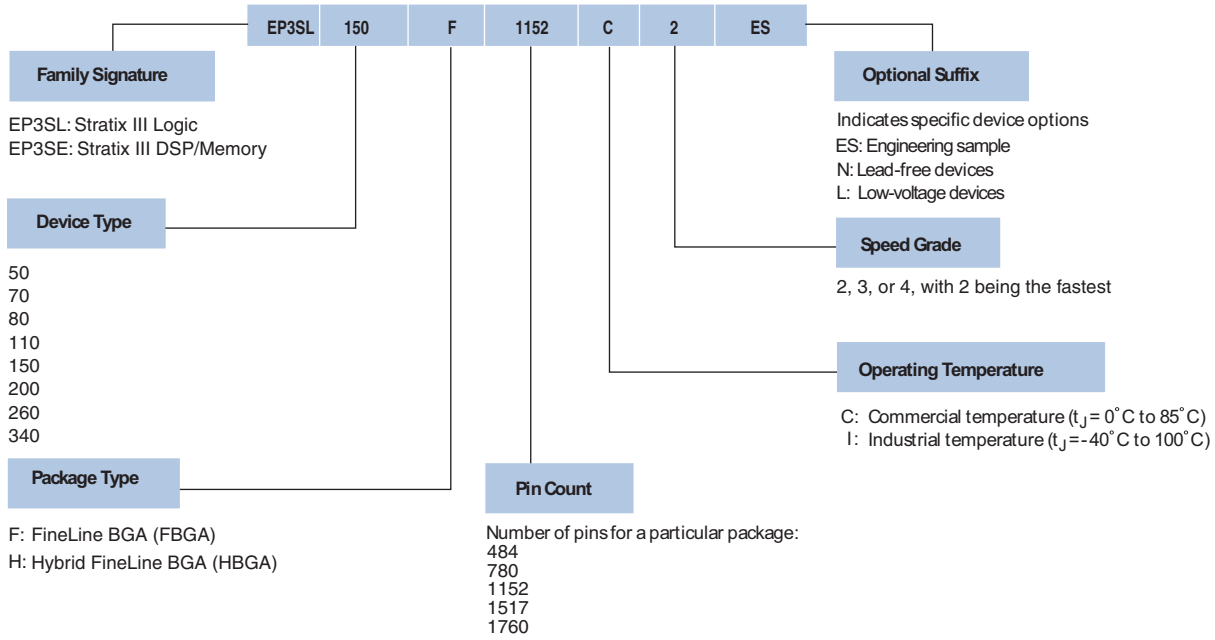
The Quartus II software supports the Windows XP/2000/NT/98, Solaris, and Linux Red Hat/SUSE operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink® interface.

Ordering Information

Figure 1–1 describes the ordering codes for Stratix III devices.

For more information about a specific package, refer to the *Stratix III Device Package Information* chapter of the *Stratix III Device Handbook*.

Figure 1–1. Stratix III Device Packaging Ordering Information



Referenced Documents

This chapter references the following documents:

- *AN 437: Power Optimization in Stratix III FPGAs*
- *Clock Networks and PLLs in Stratix III Devices*
- *Configuring Stratix III Devices*
- *Design Security in Stratix III Devices*
- *DSP Blocks in Stratix III Devices*
- *External Memory Interfaces in Stratix III Devices*
- *High Speed Differential I/O Interfaces with DPA in Stratix III Devices*
- *Hot Socketing and Power-On Reset in Stratix III Devices*
- *IEEE 1149.1 (JTAG) Boundary Scan Testing in Stratix III Devices*
- *Logic Array Blocks and Adaptive Logic Modules in Stratix III Devices*
- *MultiTrack Interconnect in Stratix III Devices*
- *Programmable Power and Temperature Sensing Diode in Stratix III Devices*
- *Quartus II Handbook*

- *Remote System Upgrades with Stratix III Devices*
- *SEU Mitigation in Stratix III Devices*
- *Stratix III Device I/O Features*
- *Stratix III Device Package Information*
- *TriMatrix Embedded Memory Blocks in Stratix III Devices*

Chapter Revision History

Table 1–6 shows the revision history for this chapter.

Table 1–6. Chapter Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.5	■ Updated "Features" section. ■ Updated Table 1–1 and Table 1–5. ■ Updated New Document Format.	—
May 2008, version 1.4	■ Updated "Introduction". ■ Updated Table 1–1. ■ Updated Table 1–2. ■ Added Table 1–5. ■ Updated "Reference and Ordering Information". ■ Updated package type information in Figure 1–1.	—
November 2007, version 1.3	■ Updated Table 1–1. ■ Updated Table 1–2.	—
October 2007, version 1.2	■ Minor typo fixes. ■ Added Table 1–4. ■ Added section "Referenced Documents". ■ Added live links for references.	—
May 2007, version 1.1	■ Minor formatting changes, fixed PLL numbers and ALM, LE and MLAB bit counts in Table 1–1.	—
November 2006, version 1.0	■ Initial Release.	—