



256-Kb I²C CMOS Serial EEPROM



FEATURES

- Supports Standard and Fast I²C Protocol
- 1.8 V to 5.5 V Supply Voltage Range
- 64-Byte Page Write Buffer
- Hardware Write Protection for entire memory
- Schmitt Triggers and Noise Suppression Filters on I²C Bus Inputs (SCL and SDA)
- Low power CMOS technology
- 1,000,000 program/erase cycles
- 100 year data retention
- Industrial and Extended temperature range
- RoHS-compliant 8-pin PDIP, SOIC, TSSOP and 8-pad TDFN packages

DESCRIPTION

The CAT24C256 is a 256-Kb Serial CMOS EEPROM, internally organized as 32,768 words of 8 bits each.

It features a 64-byte page write buffer and supports both the Standard (100 kHz) as well as Fast (400 kHz) I²C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to eight CAT24C256 devices on the same bus.

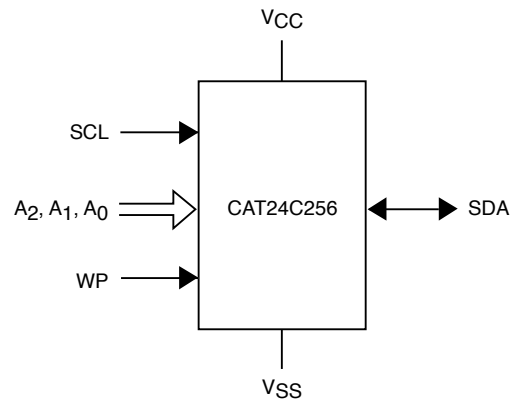
For Ordering Information details, see page 15.

PIN CONFIGURATION

	PDIP (L)	SOIC (W, X)	TSSOP (Y)	TDFN (ZD2)
A ₀	1	8	V _{CC}	
A ₁	2	7	WP	
A ₂	3	6	SCL	
V _{SS}	4	5	SDA	

For the location of Pin 1, please consult the corresponding package drawing.

FUNCTIONAL SYMBOL



PIN FUNCTIONS

Pin Name	Function
A ₀ , A ₁ , A ₂	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V _{CC}	Power Supply
V _{SS}	Ground



* Catalyst carries the I²C protocol under a license from the Philips Corporation.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on any Pin with Respect to Ground ⁽²⁾	-0.5 to +6.5	V

RELIABILITY CHARACTERISTICS ⁽³⁾

Symbol	Parameter	Min	Units
N _{END} ⁽⁴⁾	Endurance	1,000,000	Program/Erase Cycles
T _{DR}	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I _{CCR}	Read Current	Read, f _{SCL} = 400 kHz		1	mA
I _{CC}	Write Current	Write, f _{SCL} = 400 kHz		3	mA
I _{SB}	Standby Current	All I/O Pins at GND or V _{CC}	T _A = -40°C to +85°C	1	µA
			T _A = -40°C to +125°C	2	
I _L	I/O Pin Leakage	Pin at GND or V _{CC}	T _A = -40°C to +85°C	1	µA
			T _A = -40°C to +125°C	2	
V _{IL}	Input Low Voltage		-0.5	V _{CC} x 0.3	V
V _{IH}	Input High Voltage		V _{CC} x 0.7	V _{CC} + 0.5	V
V _{OL1}	Output Low Voltage	V _{CC} ≥ 2.5 V, I _{OL} = 3.0 mA		0.4	V
V _{OL2}	Output Low Voltage	V _{CC} < 2.5 V, I _{OL} = 1.0 mA		0.2	V

PIN IMPEDANCE CHARACTERISTICS

V_{CC} = 1.8 V to 5.5 V, T_A = -40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Conditions	Max	Units
C _{IN} ⁽³⁾	SDA I/O Pin Capacitance	V _{IN} = 0 V	8	pF
C _{IN} ⁽³⁾	Input Capacitance (other pins)	V _{IN} = 0 V	6	pF
I _{WP} ⁽⁵⁾	WP Input Current (Product Revision C and higher)	V _{IN} < V _{IH} , V _{CC} = 5.5 V	130	µA
		V _{IN} < V _{IH} , V _{CC} = 3.3 V	120	
		V _{IN} < V _{IH} , V _{CC} = 1.8 V	80	
		V _{IN} > V _{IH}	1	

Notes:

- (1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.
- (2) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.
- (3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
- (4) Page Mode V_{CC} = 5 V, 25°C
- (5) When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull-down reverts to a weak current source. The variable WP input impedance is available only for Die Rev. C and higher.

A.C. CHARACTERISTICS ⁽¹⁾

$V_{CC} = 1.8\text{ V to }5.5\text{ V}$, $T_A = -40^\circ\text{C to }+125^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Standard $V_{CC} = 1.8\text{ V} - 5.5\text{ V}$		Fast $V_{CC} = 1.8\text{ V} - 5.5\text{ V}$		Fast-Plus ⁽⁴⁾ $V_{CC} = 2.5\text{ V} - 5.5\text{ V}$ $T_A = -40^\circ\text{C to }+85^\circ\text{C}$		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.55		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.25		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
$t_R^{(2)}$	SDA and SCL Rise Time		1,000		300		100	ns
$t_F^{(2)}$	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		μs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.50	μs
t_{DH}	Data Out Hold Time	100		100		50		ns
$T_i^{(2)}$	Noise Pulse Filtered at SCL and SDA Inputs		100		100		100	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		μs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		μs
t_{WR}	Write Cycle Time		5		5		5	ms
$t_{PU}^{(2,3)}$	Power-up to Ready Mode		1		1	0.1	1	ms

A.C. TEST CONDITIONS

Input Levels	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Input Rise and Fall Times	$\leq 50\text{ ns}$
Input Reference Levels	$0.3 \times V_{CC}$, $0.7 \times V_{CC}$
Output Reference Levels	$0.5 \times V_{CC}$
Output Load	Current Source: $I_L = 3\text{ mA}$ ($V_{CC} \geq 2.5\text{ V}$); $I_L = 1\text{ mA}$ ($V_{CC} < 2.5\text{ V}$); $C_L = 100\text{ pF}$

Notes:

- (1) Test conditions according to "A.C. Test Conditions" table.
- (2) Tested initially and after a design or process change that affects this parameter.
- (3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.
- (4) **Fast-Plus (1 MHz) speed class available for product revision "D", identified by letter "D" marked on top of the package.**

POWER-ON RESET (POR)

The CAT24C256 Die Rev. C incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level.

This bi-directional POR behavior protects the device against brown-out failure, following a temporary loss of power.

PIN DESCRIPTION

SCL: The Serial Clock input pin accepts the Serial Clock signal generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A₀, A₁ and A₂: The Address pins accept the device address. These pins have on-chip pull-down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on-chip pull-down resistor.

FUNCTIONAL DESCRIPTION

The CAT24C256 supports the Inter-Integrated Circuit (I²C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C256 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A₀, A₁, and A₂.

I²C BUS PROTOCOL

The I²C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 1).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 2). The next 3 bits, A₂, A₁ and A₀, select one of 8 possible Slave devices. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 3). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 4.

Figure 1: Start/Stop Timing

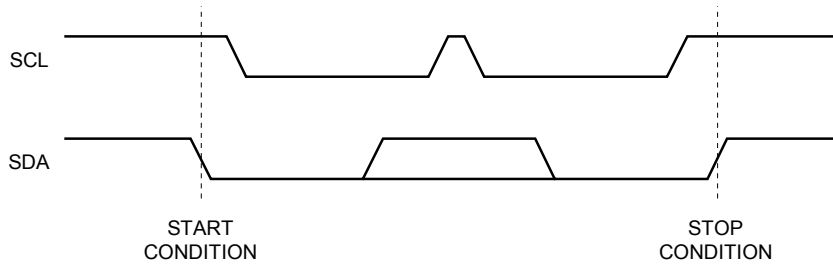


Figure 2: Slave Address Bits

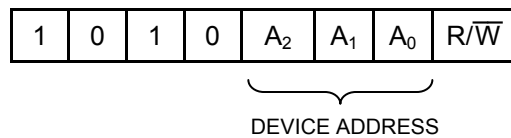


Figure 3: Acknowledge Timing

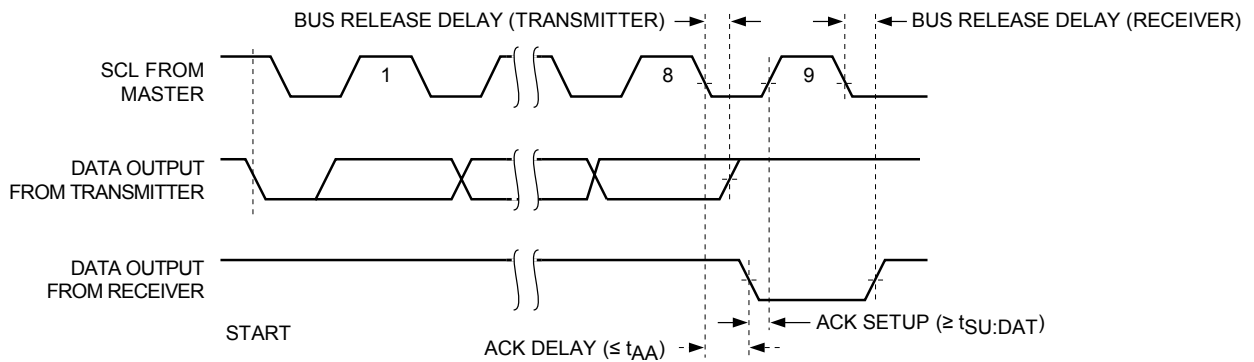
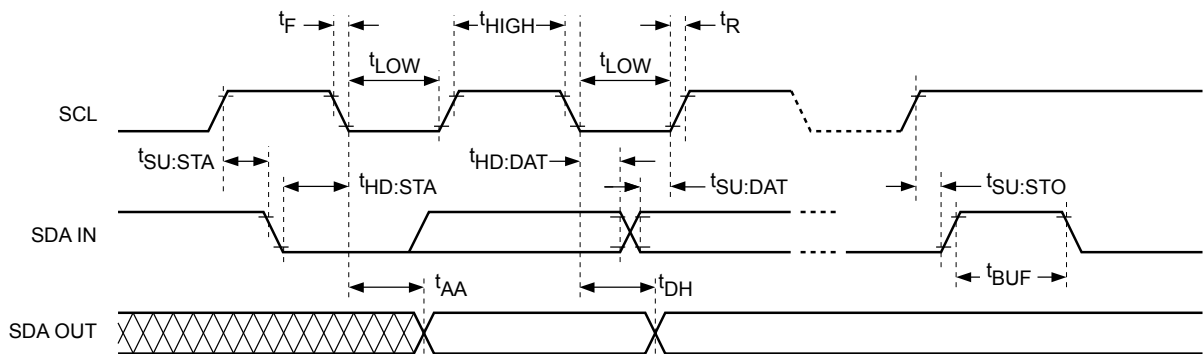


Figure 4: Bus Timing



WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 5). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 6). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The CAT24C256 contains 32,768 bytes of data, arranged in 512 pages of 64 bytes each. A two byte address word, following the Slave address, points to the first byte to be written. The most significant bit of the address word is 'don't care', the next 9 bits identify the page and the last 6 bits identify the byte within the page. Up to 64 bytes can be written in one Write cycle (Figure 7).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 64 data bytes, then earlier bytes will be overwritten by later bytes in a 'wrap-around' fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT24C256 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a 'Selective Read' command (see READ OPERATIONS).

The CAT24C256 will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24C256. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 8). If the WP pin is HIGH during the strobe interval, the CAT24C256 will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24C256 is shipped erased, i.e., all bytes are FFh.

Figure 5: Byte Write Timing

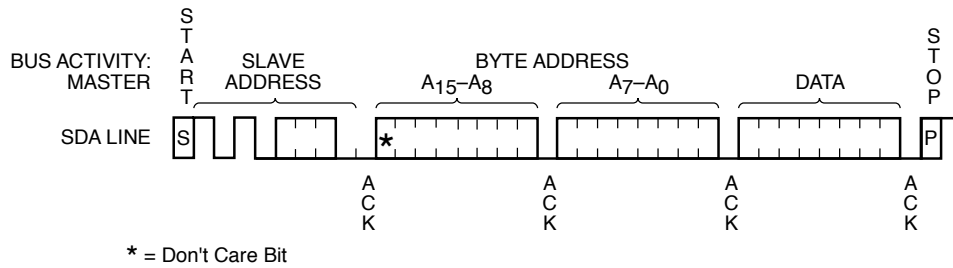


Figure 6: Write Cycle Timing

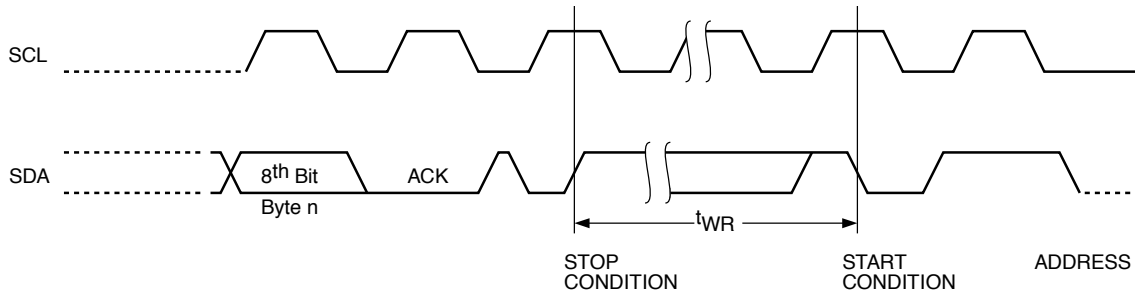


Figure 7: Page Write Timing

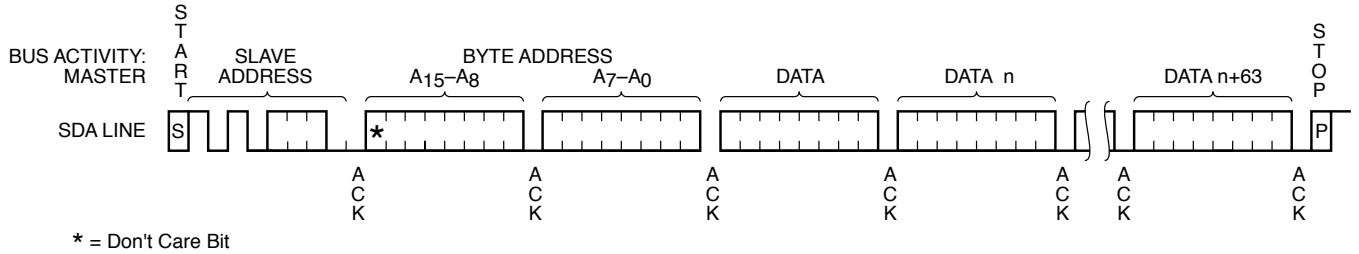
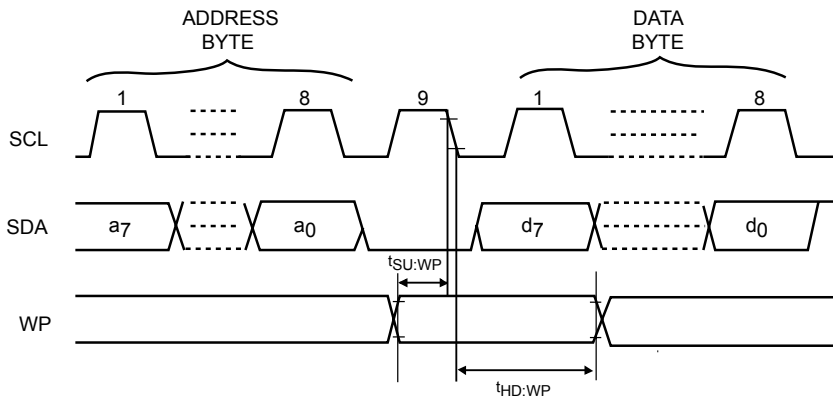


Figure 8: WP Timing



READ OPERATIONS

Immediate Address Read

In standby mode, the CAT24C256 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that 'previous' byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT24C256 is presented with a Slave address containing a '1' in the R/W bit position (Figure 9), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a 'dummy' Write operation (Figure 10). Here the START is followed by the Slave address (with the R/W bit set to '0') and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the 'Immediate Address Read' sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT24C256, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 11). If the end of memory is reached during sequential Read, then the address counter will 'wrap-around' to the beginning of memory, etc. Sequential Read works with either 'Immediate Address Read' or 'Selective Read', the only difference being the starting byte address.

Figure 9: Immediate Address Read Timing

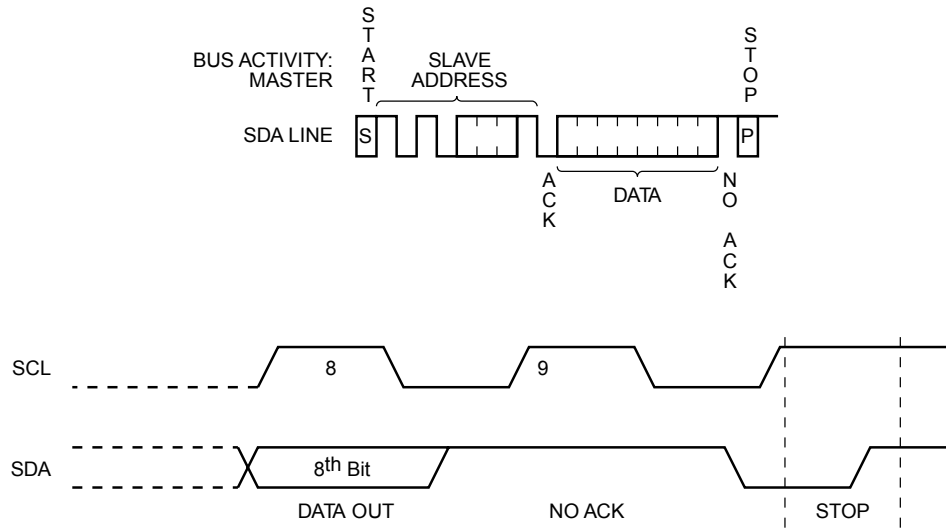


Figure 10: Selective Read Timing

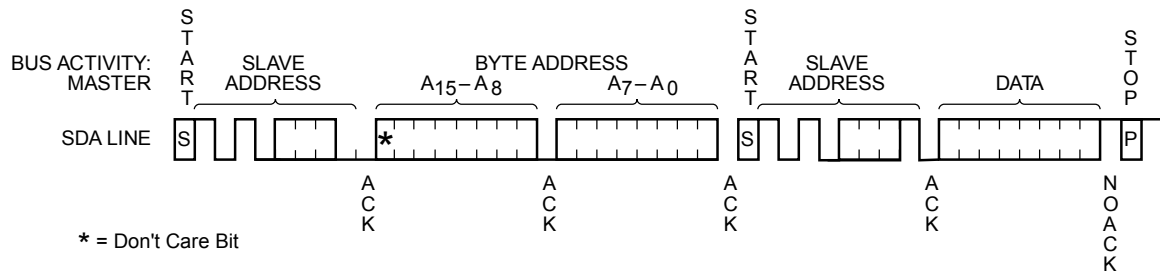
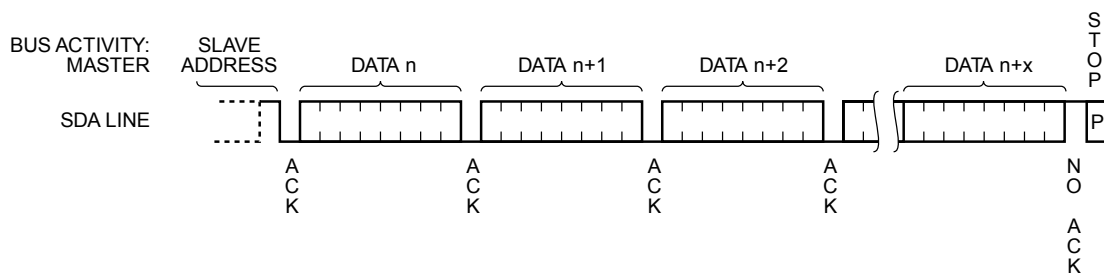
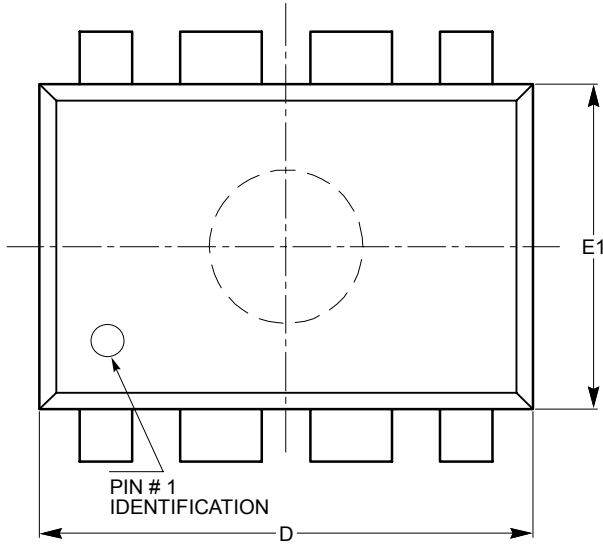


Figure 11: Sequential Read Timing



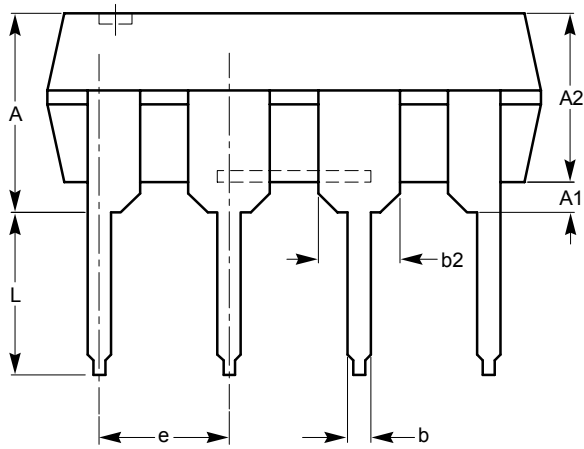
PACKAGE OUTLINE DRAWINGS

PDIP 8-Lead 300 mil (L) ⁽¹⁾⁽²⁾

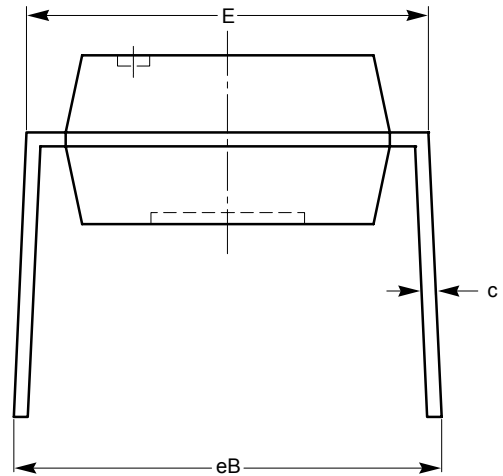


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
e	2.54 BSC		
E1	6.10	6.35	7.11
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW



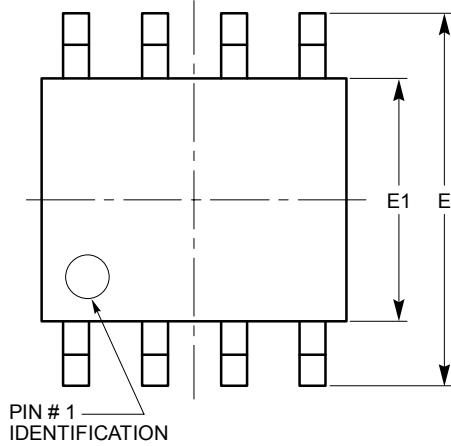
END VIEW

For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

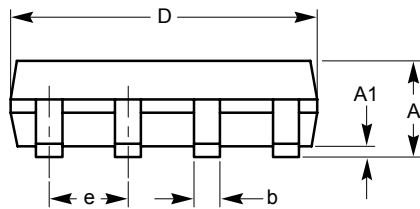
- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MS-001.

SOIC 8-Lead 150 mil (W) ⁽¹⁾⁽²⁾

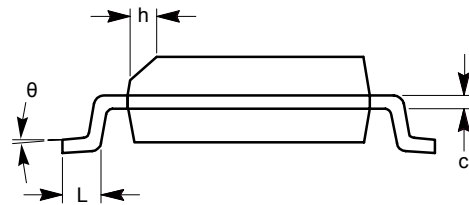


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0°		8°



SIDE VIEW



END VIEW

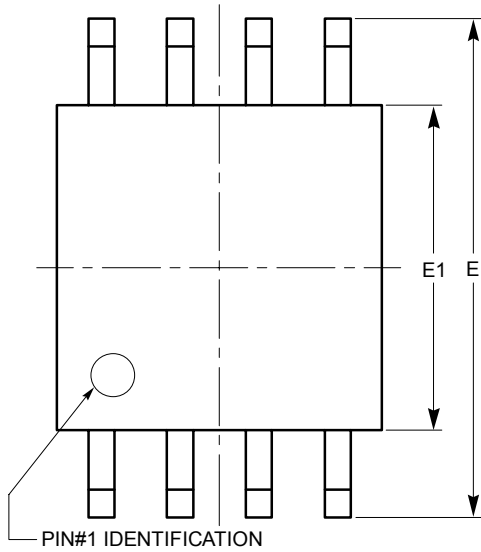
For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MS-012.

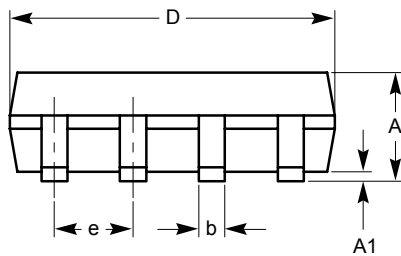
CAT24C256

SOIC 8-Lead 208 mil (X) ⁽¹⁾⁽²⁾

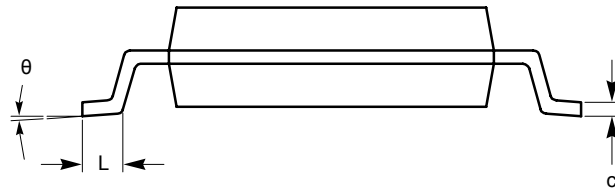


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e	1.27 BSC		
L	0.51		0.76
θ	0°		8°



SIDE VIEW



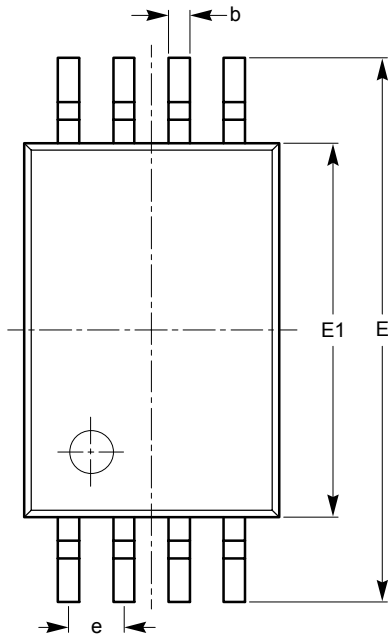
END VIEW

For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

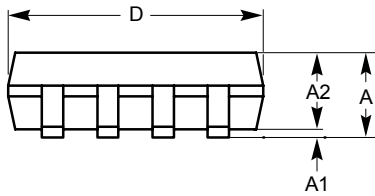
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with EIAJ EDR-7320.

TSSOP 8-Lead 4.4 mm (Y) ⁽¹⁾⁽²⁾

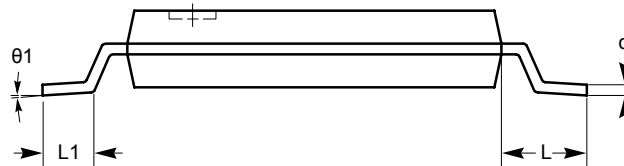


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
$\theta 1$	0°		8°



SIDE VIEW



END VIEW

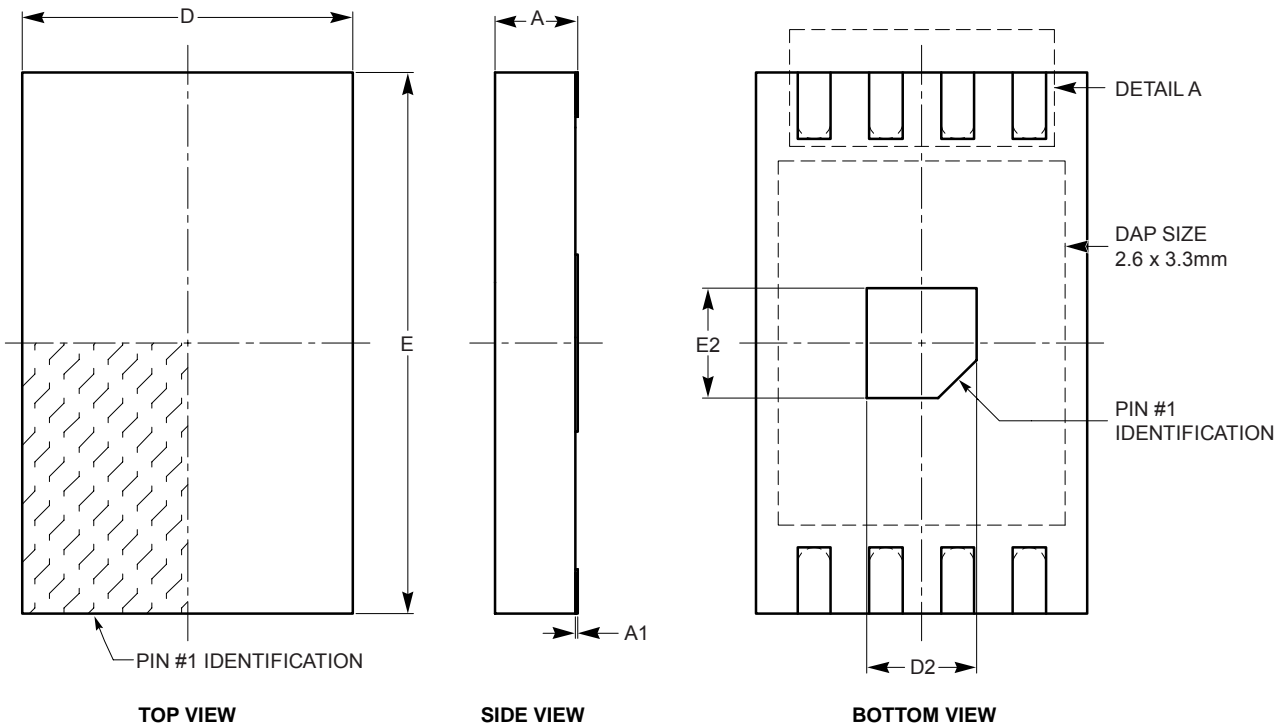
For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>.

Notes:

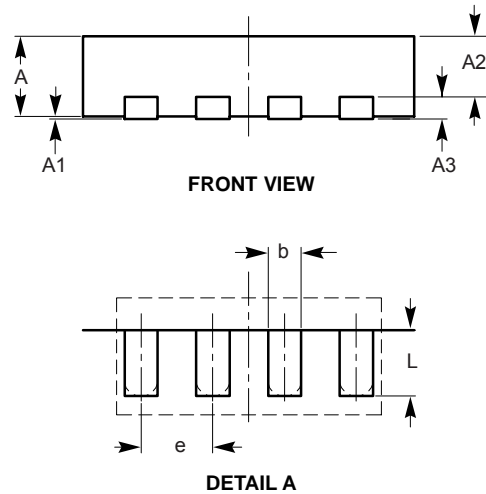
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-153.

CAT24C256

TDFN 8-Pad 3 x 4.9 mm (ZD2) ⁽¹⁾⁽²⁾



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3	0.20 REF		
b	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	0.90	1.00	1.10
E	4.80	4.90	5.00
E2	0.90	1.00	1.10
e	0.65 TYP		
L	0.50	0.60	0.70

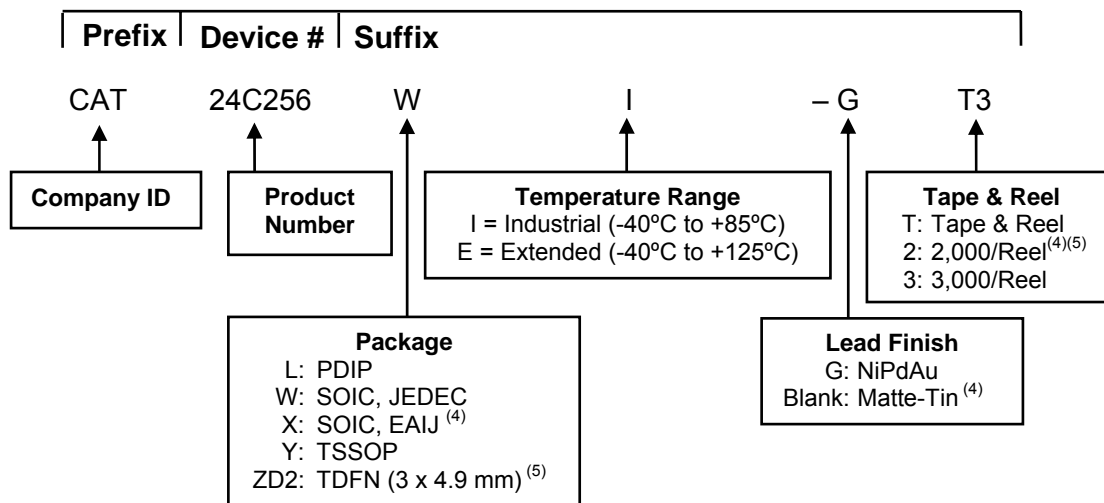


For current Tape and Reel information, download the PDF file from:
<http://www.catsemi.com/documents/tapeandreel.pdf>

Notes:

- (1) All dimensions are in millimeters.
- (2) Complies with JEDEC MO-229.

EXAMPLE OF ORDERING INFORMATION



ORDERING INFORMATION

Orderable Part Numbers	
CAT24C256LI-G	CAT24C256LE-G
CAT24C256WI-GT3	CAT24C256WE-GT3
CAT24C256XI-T2	CAT24C256XE-T2
CAT24C256YI-GT3	CAT24C256YE-GT3
CAT24C256ZD2IGT2*	CAT24C256ZD2EGT2*


* Part number is not exactly the same as the “Example of Ordering Information” shown above. For part numbers marked with * there are NO hyphens in the orderable part numbers.

Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a CAT24C256WI-GT3 (SOIC-JEDEC, Industrial Temperature, NiPdAu, Tape & Reel, 3,000/Reel).
- (4) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2,000 pcs/reel, i.e. CAT24C256XI-T2.
- (5) The TDFN 3 x 4.9 mm (ZD2) package is available in 2000 pcs/reel, i.e., CAT24C256ZD2I-GT2.
- (6) For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.

REVISION HISTORY

Date	Revision	Description
10-Jul-05	A	Initial Issue
16-Nov-05	B	Update Ordering Information Add Tape and Reel Specifications
02-Feb-06	C	Update Ordering Information
12-Jan-07	D	Update Package Outlines. Add SOIC, EIAJ Package Outlines Update A.C. Characteristics. Add A.C. Test Conditions Update Figures 1, 3, and 4 Delete Package Marking. Deleted Tape and Reel Update Ordering Information
08-May-07	E	Update Features/Packages Update Pin Configuration Update Pin Impedance Characteristics Add Power-On Reset (POR) text Update Hardware Write Protection Add WP Timing (Figure 8) (Renumbered Figures 9 & 11) Add 8-Lead TSSOP Package Outline Add 8-pad TDFN 3 x 4.9 mm Package Outline Updated Ordering Information
15-Aug-07	F	Updated PDIP, SOIC, TSSOP, and TDFN Package Outline Drawings
12-Oct-08	G	Updated SOIC 8L, 208 mil, Package Outline Drawing Change logo and fine print to ON Semiconductor
01-Jul-09	H	Update D.C Operating Characteristics and A.C. Characteristics tables Add Extended Temperature range
27-Jul-09	I	Add Ordering Information table

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