

BSS138

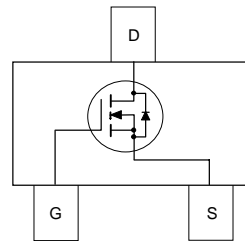
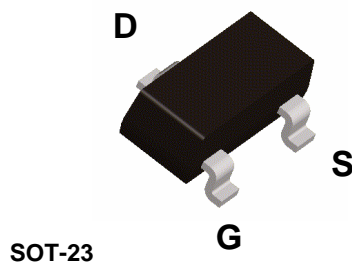
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- 0.22 A, 50 V. $R_{DS(ON)} = 3.5\Omega @ V_{GS} = 10\text{ V}$
 $R_{DS(ON)} = 6.0\Omega @ V_{GS} = 4.5\text{ V}$
- High density cell design for extremely low $R_{DS(ON)}$
- Rugged and Reliable
- Compact industry standard SOT-23 surface mount package



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	50	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current – Continuous (Note 1)	0.22	A
	– Pulsed	0.88	
P _D	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above 25°C	2.8	mW/°C
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C
T _L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1)	350	°C/W
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Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
SS	BSS138	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	50			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		72		$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$			0.5	μA
		$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			5	μA
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			100	nA
I_{GSS}	Gate–Body Leakage.	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	0.8	1.3	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 1\text{ mA}$, Referenced to 25°C		–2		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 10\text{ V}, I_D = 0.22\text{ A}$		0.7	3.5	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 0.22\text{ A}$		1.0	6.0	
		$V_{GS} = 10\text{ V}, I_D = 0.22\text{ A}, T_J = 125^\circ\text{C}$		1.1	5.8	
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	0.2			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 0.22\text{ A}$	0.12	0.5		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		27		pF
C_{oss}	Output Capacitance			13		pF
C_{rss}	Reverse Transfer Capacitance			6		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		9		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 30\text{ V}, I_D = 0.29\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		2.5	5	ns
t_r	Turn–On Rise Time			9	18	ns
$t_{d(off)}$	Turn–Off Delay Time			20	36	ns
t_f	Turn–Off Fall Time			7	14	ns
Q_g	Total Gate Charge	$V_{DS} = 25\text{ V}, I_D = 0.22\text{ A},$ $V_{GS} = 10\text{ V}$		1.7	2.4	nC
Q_{gs}	Gate–Source Charge			0.1		nC
Q_{gd}	Gate–Drain Charge			0.4		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current			0.22		A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 0.44\text{ A}$ (Note 2)		0.8	1.4	V

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- 350°C/W when mounted on a minimum pad..

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

Typical Characteristics

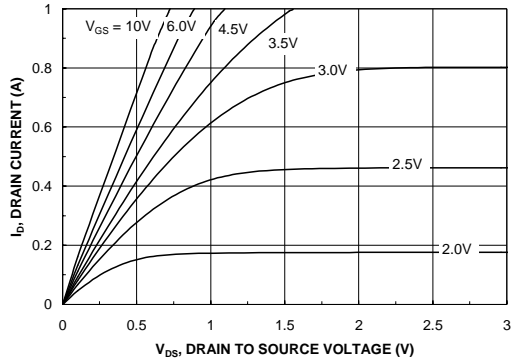


Figure 1. On-Region Characteristics.

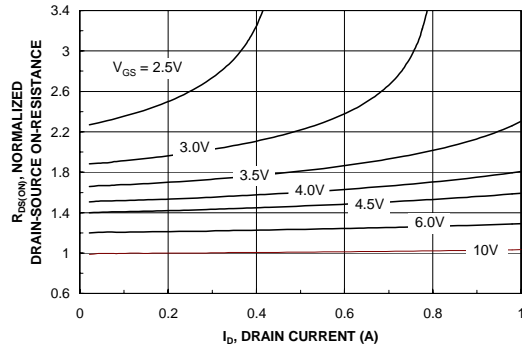


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

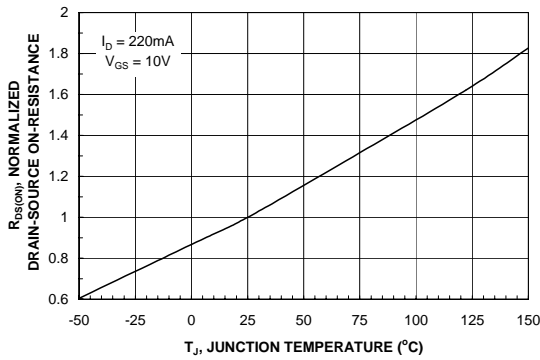


Figure 3. On-Resistance Variation with Temperature.

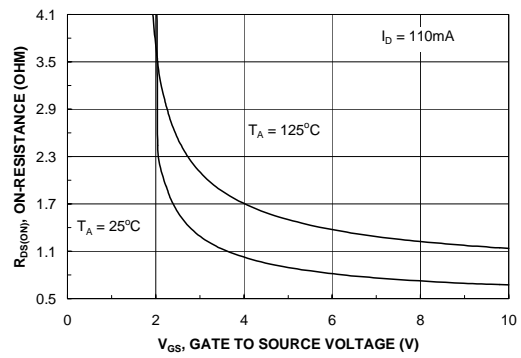


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

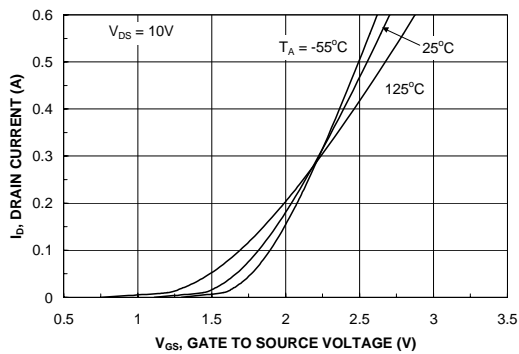


Figure 5. Transfer Characteristics.

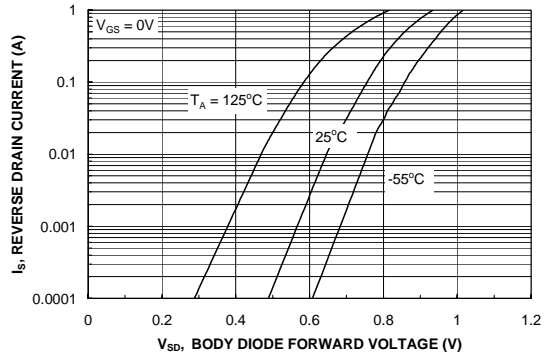


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

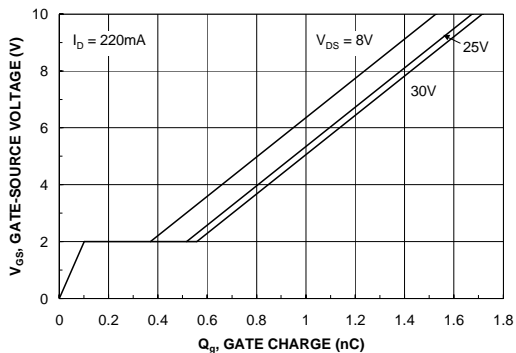


Figure 7. Gate Charge Characteristics.

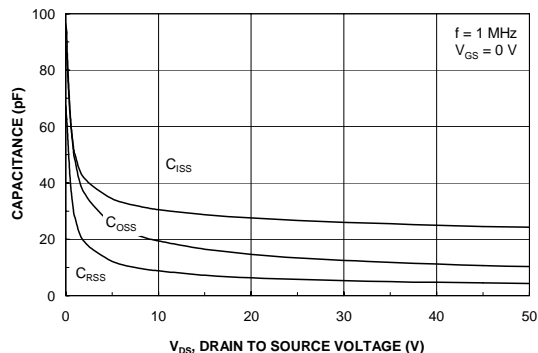


Figure 8. Capacitance Characteristics.

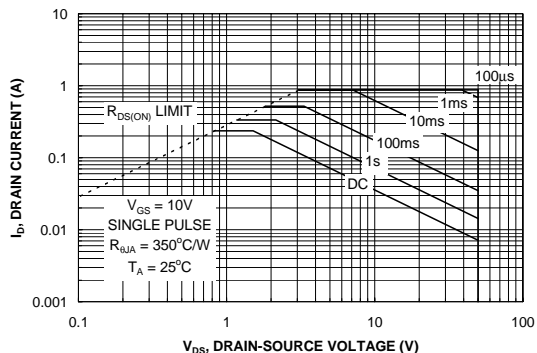


Figure 9. Maximum Safe Operating Area.

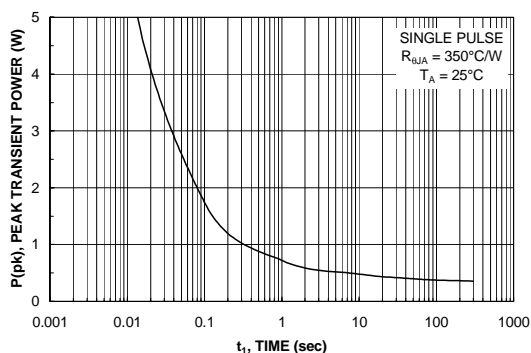


Figure 10. Single Pulse Maximum Power Dissipation.

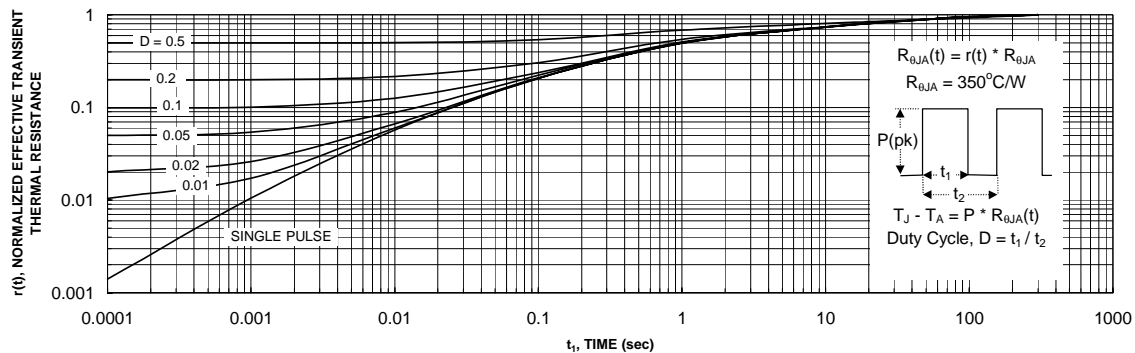
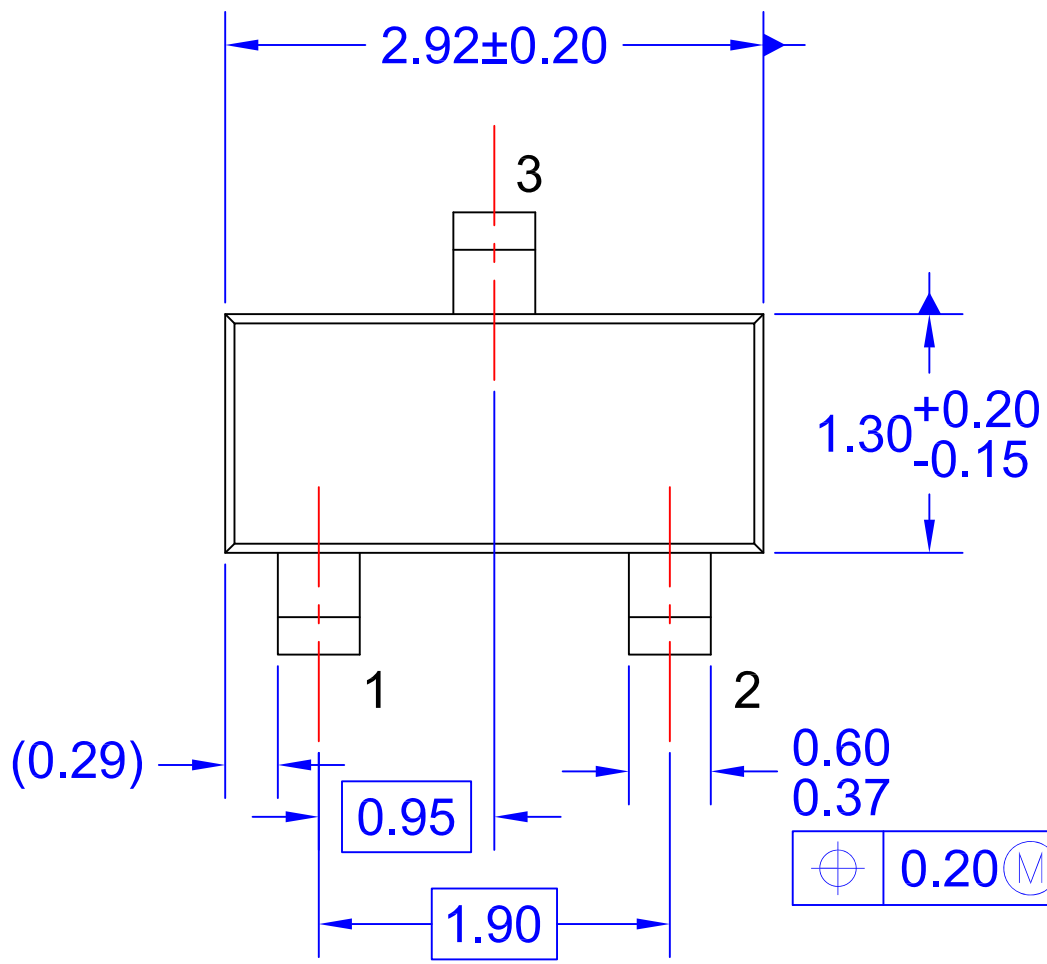
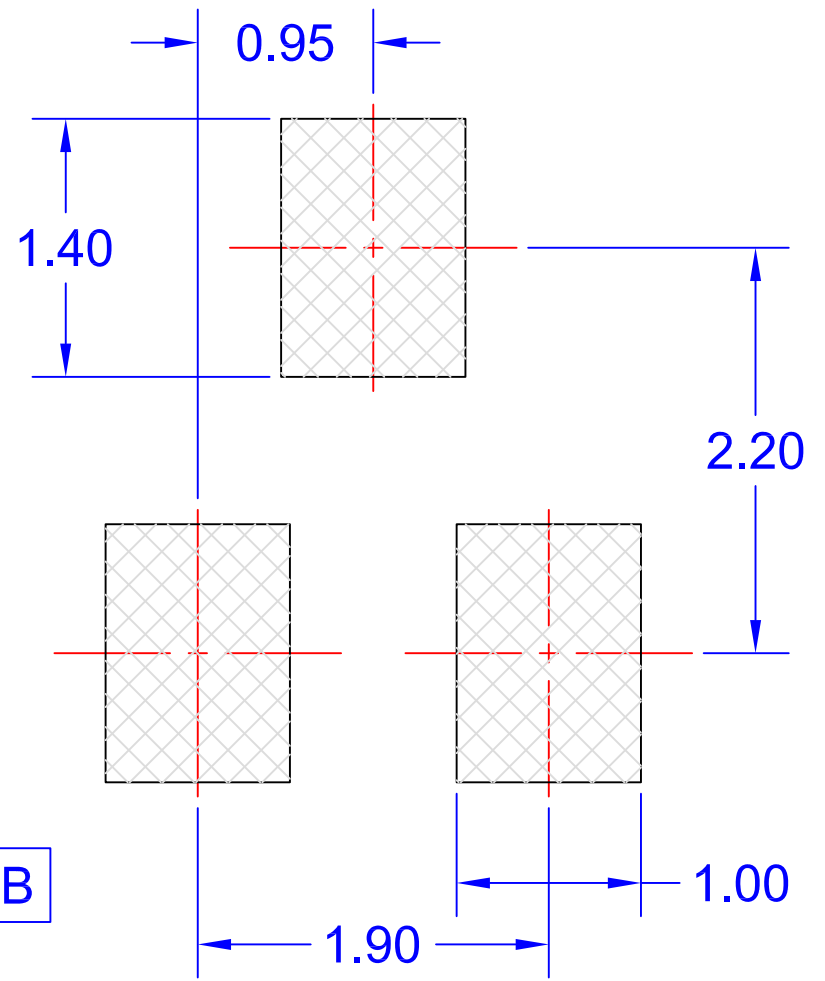


Figure 11. Transient Thermal Response Curve.

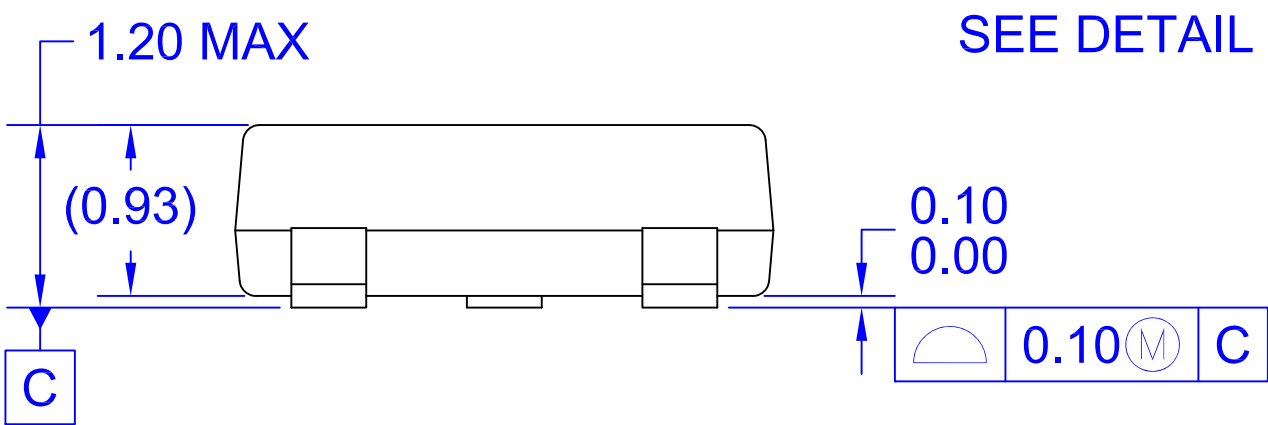
Thermal characterization performed using the conditions described in Note 1a. Transient thermal response will change depending on the circuit board design.



\oplus 0.20 (M) A B

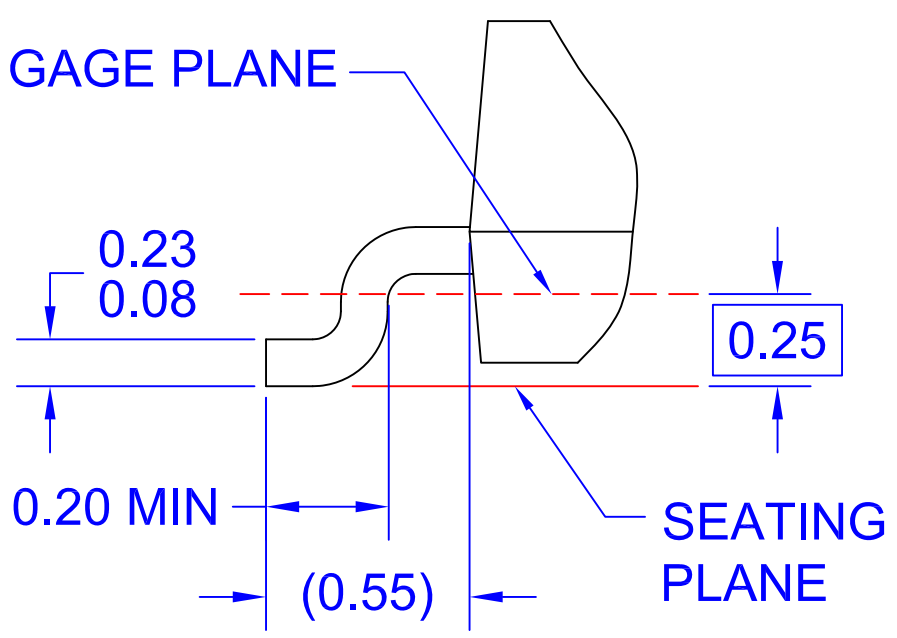
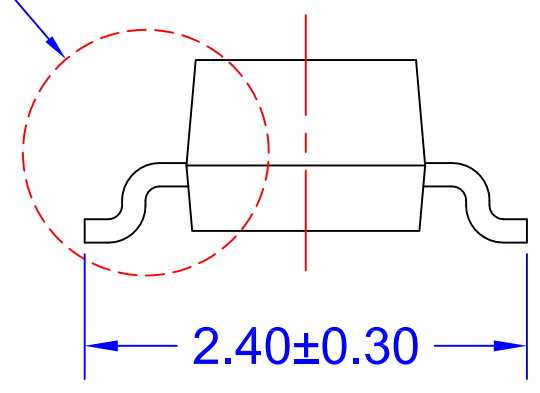


LAND PATTERN RECOMMENDATION



$\frac{1}{4}$ 0.10 (M) C

SEE DETAIL A



DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

- A) REFERENCE JEDEC REGISTRATION TO-236, VARIATION AB, ISSUE H.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE INCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M - 2009.
- E) DRAWING FILE NAME: MA03DREV11





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