Features

- Single 2.7V - 3.6V Supply
- Dual-interface Architecture
  - RapidS™ Serial Interface: 66 MHz Maximum Clock Frequency
    SPI Compatible Modes 0 and 3
  - Rapid8™ 8-bit Interface: 50 MHz Maximum Clock Frequency
- User Configurable Page Size
  - 1024 Bytes per Page
  - 1056 Bytes per Page
  - Page Size Can Be Factory Pre-configured for 1024 Bytes
- Page Program Operation
  - Intelligent Programming Operation
  - 8192 Pages (1024/1056 Bytes/Page) Main Memory
- Flexible Erase Options
  - Page Erase (1 Kbyte)
  - Block Erase (8 Kbytes)
  - Sector Erase (256 Kbytes)
  - Chip Erase (64 Mbits)
- Two SRAM Data Buffers (1024/1056 Bytes)
  - Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 10 mA Active Read Current Typical – Serial Interface
  - 10 mA Active Read Current Typical – 8-bit Interface
  - 25 µA Standby Current Typical
  - 9 µA Deep Power Down Typical
- Hardware and Software Data Protection Features
  - Individual Sector
- Permanent Sector Lockdown for Secure Code and Data Storage
  - Individual Sector
- Security: 128-byte Security Register
  - 64-byte User Programmable Space
  - Unique 64-byte Device Identifier
- JEDEC Standard Manufacturer and Device ID Read
- 100,000 Program/Erase Cycles Per Page Minimum
- Data Retention – 20 Years
- Green (Pb/Halide-free/RoHS Compliant) Packaging Options
- Temperature Range
  - Industrial: -40° C to +85° C

64-megabit 2.7-volt Dual-interface DataFlash®

AT45DB642D

1. Description

The AT45DB642D is a 2.7-volt, dual-interface sequential access Flash memory ideally suited for a wide variety of digital voice-, image-, program code- and data-storage applications. The AT45DB642D supports RapidS serial interface and Rapid8 8-bit interface. RapidS serial interface is SPI compatible for frequencies up to 66 MHz. The dual-interface allows a dedicated serial interface to be connected to a DSP and a dedicated 8-bit interface to be connected to a microcontroller or vice versa. However, the use of either interface is purely optional. Its 69,206,016 bits of memory are organized as 8,192 pages of 1,024 bytes (binary page size) or 1,056 bytes (standard DataFlash page size) each. In addition to the main memory, the AT45DB642D also contains two SRAM buffers of 1,024 (binary buffer size) bytes/1,056 bytes (standard DataFlash buffer size) each. The buffers allow receiving of data while a page in the main Memory is being reprogrammed, as well as writing a continuous data stream. EEPROM emulation (bit or byte alterability) is easily handled with a self-contained three step read-modify-write operation. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash uses either a RapidS serial interface or a 8-bit Rapid8 interface to sequentially access its data. The simple sequential access dramatically reduces active pin count, facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage and low-power are essential.

To allow for simple in-system reprogrammability, the AT45DB642D does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB642D is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK), or an 8-bit interface consisting of the input/output pins (I/O7 - I/O0) and the clock pin (CLK).

All programming and erase cycles are self-timed.

18. Electrical Specifications

Table 18-1. Absolute Maximum Ratings*

Temperature under Bias	-55° C to +125° C
Storage Temperature	-65° C to +150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18-2. DC and AC Operating Range

		AT45DB642D
Operating Temperature (Case)	Ind.	-40° C to 85° C
V_{CC} Power Supply		2.7V to 3.6V

Table 18-3. DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DP}	Deep Power-down Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		9	18	µA
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		25	50	µA
I_{CC1} (1)	Active Current, Read Operation, Serial Interface	f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	15	mA
I_{CC2} (1)	Active Current, Read Operation, Rapid8 Interface	f = 33 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		10	15	mA
I_{CC3}	Active Current, Program Operation, Page Program	V_{CC} = 3.6V			25	mA
I_{CC4}	Active Current, Page Erase, Block Erase, Sector Erase Operation	V_{CC} = 3.6V			25	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

Notes: 1. AI_{CC1} and I_{CC2} during a buffer read is 25 mA maximum.
2. All inputs are 5 volts tolerant.

Table 18-4. AC Characteristics – RapidS/Serial Interface

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Frequency			66	MHz
f_{CAR1}	SCK Frequency for Continuous Array Read			66	MHz
f_{CAR2}	SCK Frequency for Continuous Array Read (Low Frequency)			33	MHz
t_{WH}	SCK High Time	6.8			ns
t_{WL}	SCK Low Time	6.8			ns
t_{SCKR}[1]	SCK Rise Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{SCKF}[1]	SCK Fall Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	50			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			100	ns
t_{SU}	Data In Setup Time	2			ns
t_{H}	Data In Hold Time	3			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			6	ns
t_{V}	Output Valid			6	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1	µs
t_{EDPD}	$\overline{CS}$ High to Deep Power-down Mode			3	µs
t_{RDPD}	$\overline{CS}$ High to Standby Mode			35	µs
t_{XFR}	Page to Buffer Transfer Time			400	µs
t_{comp}	Page to Buffer Compare Time			400	µs
t_{EP}	Page Erase and Programming Time (1,024/1,056 bytes)		17	40	ms
t_{P}	Page Programming Time (1,024/1,056 bytes)		3	6	ms
t_{PE}	Page Erase Time (1,024/1,056 bytes)		15	35	ms
t_{BE}	Block Erase Time (8,192/8,448 bytes)		45	100	ms
t_{SE}	Sector Erase Time (262,144/270,336 bytes)		1.6	5	s
t_{CE}	Chip Erase Time		TBD	TBD	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

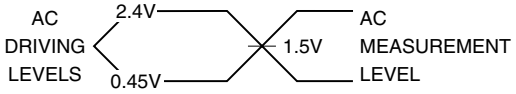
Note: 1. Values are based on device characterization, not 100% tested in production.

Table 18-5. AC Characteristics – Rapid8 8-bit Interface

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK1}	CLK Frequency			50	MHz
f_{CAR1}	CLK Frequency for Continuous Array Read			50	MHz
t_{WH}	CLK High Time	9			ns
t_{WL}	CLK Low Time	9			ns
t_{CLKR} (1)	CLK Rise Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{CLKF} (1)	CLK Fall Time, Peak-to-Peak (Slew Rate)	0.1			V/ns
t_{CS}	Minimum $\overline{CS}$ High Time	50			ns
t_{CSS}	$\overline{CS}$ Setup Time	5			ns
t_{CSH}	$\overline{CS}$ Hold Time	5			ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low			100	ns
t_{SU}	Data In Setup Time	2			ns
t_H	Data In Hold Time	5			ns
t_{HO}	Output Hold Time	0			ns
t_{DIS}	Output Disable Time			12	ns
t_V	Output Valid			12	ns
t_{WPE}	$\overline{WP}$ Low to Protection Enabled			1	µs
t_{WPD}	$\overline{WP}$ High to Protection Disabled			1	µs
t_{EDPD}	$\overline{CS}$ High to Deep Power-down Mode			3	µs
t_{RDPD}	$\overline{CS}$ High to Standby Mode			35	µs
t_{XFR}	Page to Buffer Transfer Time			400	µs
t_{comp}	Page to Buffer Compare Time			400	µs
t_{EP}	Page Erase and Programming Time (1,024/1,056 bytes)		17	40	ms
t_P	Page Programming Time (1,024/1,056 bytes)		3	6	ms
t_{PE}	Page Erase Time (1,024/1,056 bytes)		15	35	ms
t_{BE}	Block Erase Time (8,192/8,448 bytes)		45	100	ms
t_{SE}	Sector Erase Time (262,144/270,336 bytes)		1.6	5	s
t_{RST}	$\overline{RESET}$ Pulse Width	10			µs
t_{REC}	$\overline{RESET}$ Recovery Time			1	µs

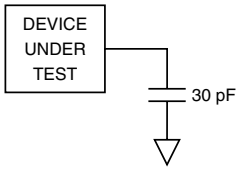
Note: Values are based on device characterization, not 100% tested in production.

19. Input Test Waveforms and Measurement Levels



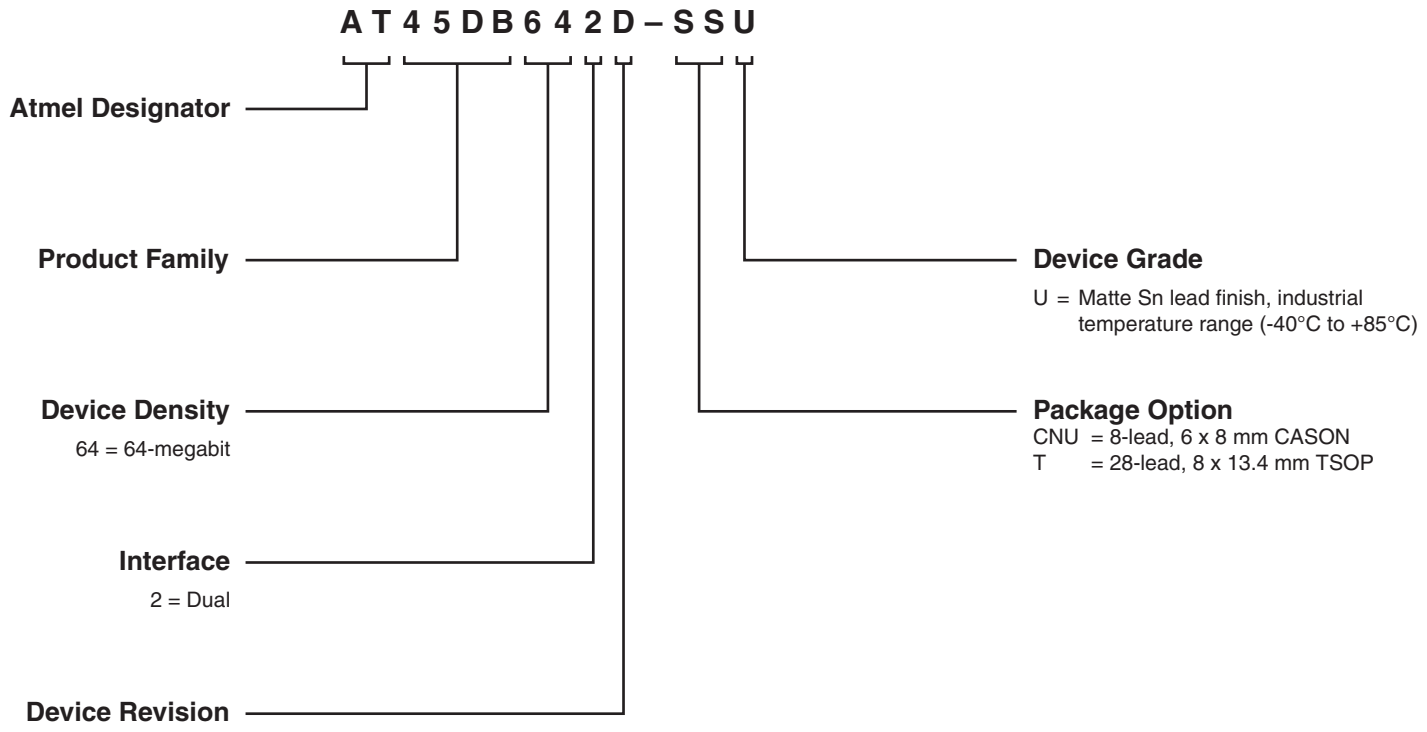
t_R, t_F < 2 ns (10% to 90%)

20. Output Test Load



27. Ordering Information

27.1 Ordering Code Detail



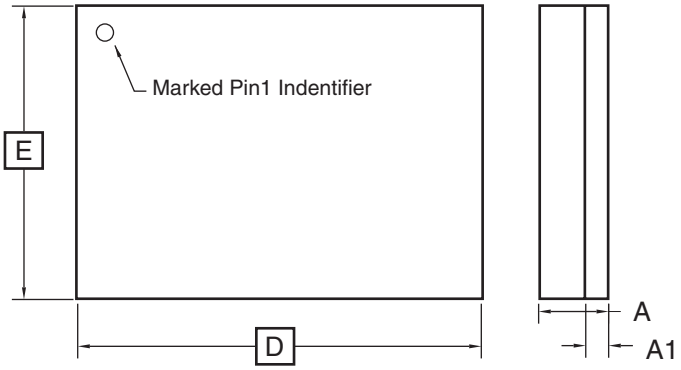
27.2 Green Package Options (Pb/Halide-free/RoHS Compliant)

Ordering Code[1][2]	Package	Lead Finish	Operating Voltage	f_{SCK} (MHz)	Operation Range
AT45DB642D-CNU AT45DB642D-CNU-SL954[3] AT45DB642D-CNU-SL955[4]	8CN3	Matte Sn	2.7V to 3.6V	66	Industrial (-40° C to 85° C) 2.7V to 3.6V
AT45DB642D-TU	28T				

Notes:
1. The shipping carrier option is not marked on the devices.
2. Standard parts are shipped with the page size set to 1056 bytes. The user is able to configure these parts to a 1024-byte page size if desired.
3. Parts ordered with suffix SL954 are shipped in bulk with the page size set to 1024 bytes. Parts will have a 954 or SL954 marked on them.
4. Parts ordered with suffix SL955 are shipped in tape and reel with the page size set to 1024 bytes. Parts will have a 954 or SL954 marked on them.

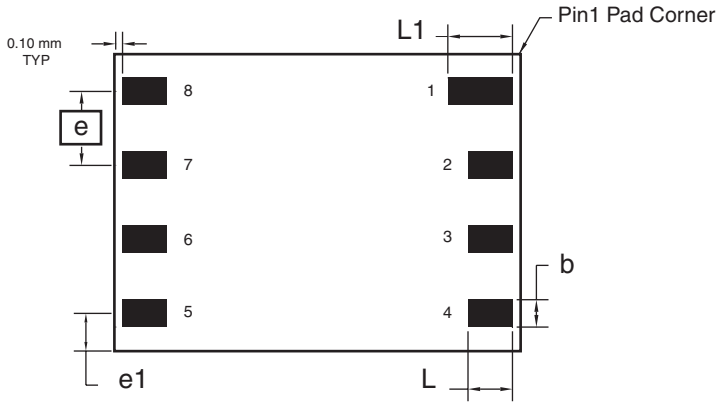
Package Type	
28T	28-lead, (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)
8CN3	8-pad (6 mm x 8 mm) Chip Array Small Outline No Lead Package (CASON)

28.2 8CN3 – CASON



Top View

Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A			1.0	
A1	0.17	0.21	0.25	
b		0.41 TYP		4
D	7.90	8.00	8.10	
E	5.90	6.00	6.10	
e		1.27 BSC		
e1		1.095 REF		
L		0.67 TYP		4
L1	0.92	0.97	1.02	4

Notes:
1. All dimensions and tolerance conform to ASME Y 14.5M, 1994.
2. The surface finish of the package shall be EDM Charmille #24-27.
3. Unless otherwise specified tolerance: Decimal ±0.05, Angular ±2°.
4. Metal Pad Dimensions.

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8CN3,** 8-pad (6 x 8 x 1.0 mm Body), Lead Pitch 1.27 mm, Chip Array Small Outline No Lead Package (CASON)	8CN3	B