AS1543/44

DataSheet

8/4-Channel, 1 Msps, 12-Bit ADC with Sequencer

1 General Description

The AS1543/44 is a 12-bit high-speed, low-power, 8/4-channel, successive-approximation ADC that operates from a single 2.7 to 5.25V supply. The device features high throughput rates (1Msps) and a low-noise, wide-bandwidth track-and-hold amplifier that can handle input frequencies in excess of 1 MHz.

The AS1543 features 8 single-ended or 4 fully differential analog inputs while the AS1544 offers 4 single-ended or 2 fully differential analog inputs. Both include a channel sequencer to allow a programmed selection of channels to be converted sequentially. The conversion time is determined by the SCLK frequency (also used as the master clock to control the conversion).

The conversion process and data acquisition are controlled using a chip select pin and a serial clock signal, allowing the device to easily interface with microprocessors or DSPs. The input signal is sampled on the falling edge of CSN and conversion is also initiated at this point. There are no pipeline delays associated with the device.

The AS1543/44 uses advanced design techniques to achieve very low power dissipation at high throughput rates. At maximum throughput rates, the AS1543/44 consumes just 2.8mA (@3.6V), and 3.5mA (@5.25V).

By using internal control register, single-ended or fully-differential conversion mode with different input ranges can be used with either straight binary or twos complement output coding.

The device is available in a TQFN(4x4)-20 pin package.

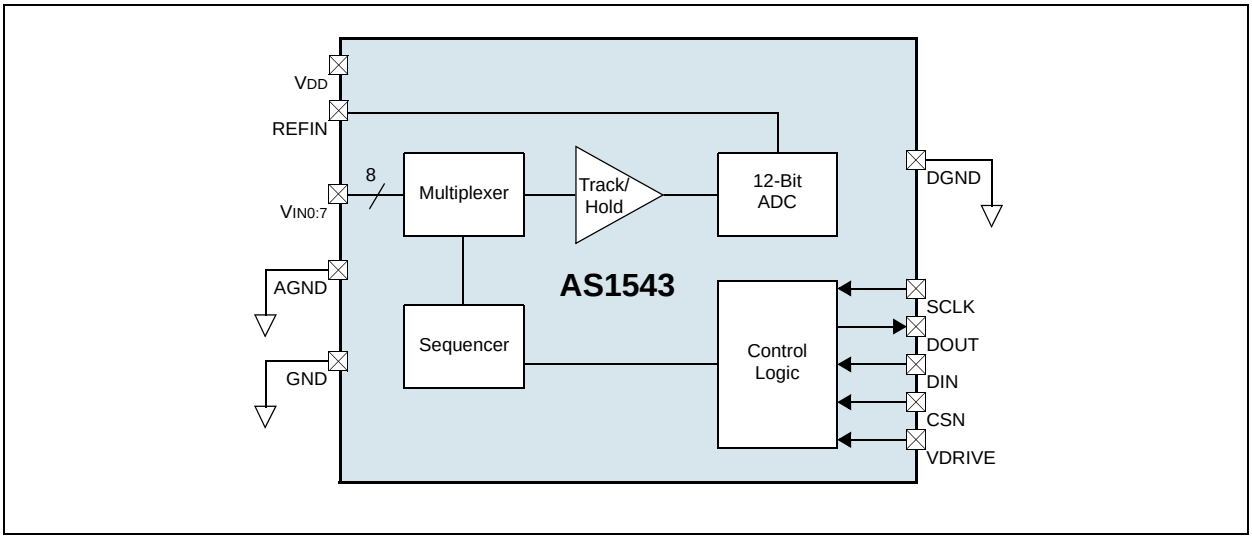
2 Key Features

- Single Supply Operation with VDRIVE Function: 2.7 to 5.25V
- Fast Throughput Rate: 1 Msps
- Sequencer & Channel Counter
- Software-Configurable Analog Input Types:
  - 8/4-Channel Single-Ended
  - 4/2-Channel Fully-Differential
- Software-Configurable Input Range
- Low Power Consumption at Max Throughput Rates:
  - 10.1mW @ 1Msps (3.6V Supply)
  - 18.4mW @ 1Msps (5.25V Supply)
- Shutdown Mode Current: 0.5µA
- Flexible Power/Serial Clock Speed Management
- Wide Input Bandwidth: 71dB SNR @ 50 kHz Input Frequency
- No Pipeline Delays
- High Speed SPI/QSPI/Microwire/DSP Interface
- TQFN(4x4)-20 Package

3 Applications

The devices are ideal for remote sensors, data-acquisition and data-logging devices, pen-digitizers, process control, or any other space-limited A/D application with low power-consumption requirements.

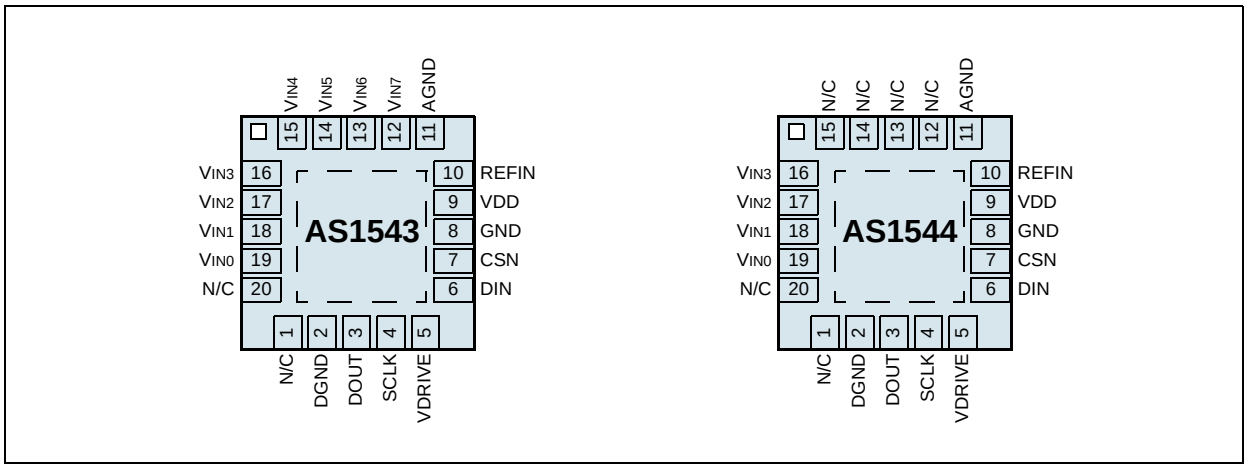
Figure 1. Typical Application



4 Pinout

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
(see Figure 2)	VINx	**Analog Inputs**. 8/4 single-ended or 4/2 fully-differential analog input channels that are multiplexed into the track-and-hold circuitry. Input channels are selected by using address bits ADDR3:ADDR0 (page 14) of the control register. The address bits in conjunction with bits SEQ (page 14) and SHADOW (page 14) allow the sequence register to be programmed. The bit SE/FDN (page 14) of the control register selects single-ended or fully-differential conversion mode. In case of single-ended mode the input range can extend from [0V to VREFIN] or [0V to 2 x VREFIN]. In case of fully-differential mode the differential input range can extend from [-VREFIN/2 to +VREFIN/2] or [-VREFIN to +VREFIN]. **Note:** Unused inputs should be connected to AGND to avoid noise.
	REFIN	**Reference Input**. An external reference must be applied to this input. The voltage range for the external reference is 2.5V ±1% for specified performance.
	SCLK	**Serial Clock**. Provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the ADC conversion process
	VDD	**2.7 to 5.25V Supply Input.** For the [0V to 2 x VREFIN] range, VDD must be between 4.75 and 5.25V
	VDRIVE	**Logic Power Supply Input**. The voltage supplied at this pin determines the operating voltage of the AS1543/44 serial interface. VDRIVE ≤ VDD required.
	DOUT	**Digital Output**. The ADC conversion result is provided serially on this output. Data bits are clocked out on the falling edge of SCLK. The data stream consists of four address bits indicating the corresponding conversion channel, followed by 12 bits of conversion data (MSB first). Output coding may be selected as straight binary or two's complement depending on the setting of bit CODING (page 14).
	DIN	**Digital Input**. Data is clocked into to the AS1543/44 control register on this input (see Control Register on page 14).
	CSN	**Chip Select**. Active low input. Initiates conversions and also is used to frame the serial data transfer.
	AGND	**Analog Ground**. Ground reference point for all analog circuitry. All analog input signals and any external reference signal should be referenced to pin AGND. **Note:** AGND, GND and DGND pins must be connected together.
	DGND	**Digital Logic Ground**. Ground reference point for the VDRIVE logic power supply input. VDRIVE should be decoupled to pin DGND.
	GND	**Supply Ground**. Ground reference point for the VDD supply input. The supply input VDD should be decoupled to pin GND.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{DD} to GND/ AGND/ DGND	-0.3	+7	V	
V_{DRIVE} to GND/ AGND/ DGND	-0.3	V_{DD} + 0.3	V	
V_{INx}, REFIN to GND/ AGND/ DGND	-0.3	V_{DD} + 0.3	V	
CSN, SCLK, DIN, DOUT to GND/ AGND/ DGND	-0.3	V_{DRIVE} + 0.3	V	
Input Current (any pin except V_{DD} and V_{INx})	-10	+10	mA	
θ_{JA} Thermal Impedance		30.8	ºC/W	
Electro-Static Discharge		1	kV	
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-65	+150	ºC	
Junction Temperature		+150	ºC	
Package Body Temperature		+260	ºC	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices".* The lead finish for Pb-free leaded packages is matte tin (100% Sn).

6 Electrical Characteristics

V_{DD} = V_{DRIVE} = 2.7 to 5.25V, REFIN = 2.5V, f_{SCLK} = 20MHz (50% Duty cycle), V_{CMIN} = V_{REFIN}/2 (when SE/FDN = 0), T_{AMB} = -40 to +85°C. Typical values at T_{AMB} = +25°C and V_{DD} = V_{DRIVE} = 5.25V (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
DC Accuracy							
	Resolution					12	Bits
INL	Integral Nonlinearity					±1	LSB
DNL	Differential Nonlinearity	Straight Binary Output Coding; Guaranteed No Missed Codes to 12 Bits		-0.95		+1.2	LSB
	Offset Error	Bit SE/FDN = 1, bit CODING = 1	Bit RANGE = 1			±4	LSB
	Offset Error Match				±0.5		LSB
	Gain Error					±4	LSB
	Gain Error Match				±0.6		LSB
	Offset Error		Bit RANGE = 0			±4	LSB
	Offset Error Match				±0.5		LSB
	Gain Error					±4	LSB
	Gain Error Match				±0.6		LSB
	Zero Code Error	Bit SE/FDN = 0, bit CODING = 0	Bit RANGE = 1		±0.6	±4	LSB
	Zero Code Error Match				±0.5		LSB
	Gain Error					±4	LSB
	Gain Error Match				±0.5		LSB
	Zero Code Error		Bit RANGE = 0		±0.6	±4	LSB
	Zero Code Error Match				±0.5		LSB
	Gain Error					±4	LSB
	Gain Error Match				±0.5		LSB
Dynamic Specifications 50kHz sinewave input							
SINAD	Signal to Noise + Distortion Ratio	Bit RANGE = 1, bit SE/FDN = 1			71.2		dB
SNR	Signal-to-Noise Ratio				71.8		dB
THD	Total Harmonic Distortion				-82		dB
SFDR	Spurious-Free Dynamic Range				84		dB
SINAD	Signal to Noise + Distortion	Bit RANGE = 0, bit SE/FDN = 0, bit CODING = 0		68	71		dB
SNR	Signal-to-Noise Ratio			68.5	71.5		dB
THD	Total Harmonic Distortion				-83	-71	dB
SFDR	Spurious-Free Dynamic Range			73	85		dB
IMD	Intermodulation Distortion	f_A = 40.1kHz, f_B = 41.5kHz	Second Order Terms		-83		dB
			Third Order Terms		-91		
	Channel-to-Channel Isolation	f_{IN} = 400kHz			-79		dB
	Full Power Bandwidth	@ 3dB			35		MHz
		@ 0.1dB			3.6		

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
Conversion Rate							
tCONV	Conversion Time	16 SCLK Cycles, SCLK = 20MHz				800	ns
	Track-and-Hold Acquisition Time					300	ns
	Throughput Rate					1	Msps
	Aperture Delay				4		ns
	Aperture Jitter				50		ps
Analog Input							
VINx	Input Voltage Ranges	Bit SE/FDN = 1	Bit RANGE = 1	0		VREFIN	V
			Bit RANGE = 0	0		2 x VREFIN	
VINx - VINy	Differential Input Voltage Ranges	Bit SE/FDN = 0	Bit RANGE = 1	-VREFIN/2		VREFIN/2	V
			Bit RANGE = 0	-VREFIN		VREFIN	
VCMIN	Input Common Mode Voltage	Bit SE/FDN = 0	Bit RANGE = 1	VREFIN/2		VDD - VREFIN/2	V
			Bit RANGE = 0	VREFIN		VDD - VREFIN	
	DC Leakage Current			-1		+1	µA
	Input Capacitance				20		pF
Reference Input							
	REFIN Input Voltage[1]	2.5V ±1% for Specified Performance		1		VDD	V
	DC Leakage Current					±1	µA
	REFIN Input Impedance	fSAMPLE = 1Msps			44		kΩ
Digital Inputs: CSN, SCLK, DIN							
VIH	Input High Voltage			0.7 x VDRIVE			V
VIL	Input Low Voltage					0.3 x VDRIVE	V
IIN	Input Current,	VIN = 0V or VDRIVE		-1		+1	µA
CIN	Input Capacitance				5		pF
Digital Output: DOUT							
VOH	Output High Voltage	ISOURCE = 200µA; VDD = 2.7 to 5.25V		VDRIVE - 0.2			V
VOL	Output Low Voltage	ISINK = 200µA				0.4	V
	Floating-State Leakage Current	Bit WEAK/TRIN (page 14) set to 0		-1		+1	µA
	Floating-State Output Capacitance	Bit WEAK/TRIN set to 0			10		pF
	Output Coding	Bit CODING (page 14) set to 1		Straight (natural) binary			
		Bit CODING set to 0		Two's complement			

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
Power Requirements							
V_{DD}	Input Supply Range			2.75		5.25	V
V_{DRIVE}	DRIVE Range	$V_{DRIVE} \leq V_{DD}$		2.75		5.25	V
I_{DD}	Input Current	Normal Mode (Static)	V_{DD} = 2.7 to 5.25V, SCLK On or Off		1.8		mA
		Normal Mode (Operational); f_S = Max Throughput	V_{DD} = 4.75 to 5.25V, f_{SCLK} = 20 MHz		3.0	3.5	mA
			V_{DD} = 2.7 to 3.6V, f_{SCLK} = 20 MHz		2.4	2.8	mA
		Auto Shutdown Mode	f_{SAMPLE} = 250ksps		1.4	1.6	mA
			Static		0.01	0.5	µA
	Power Dissipation (see Power vs. Throughput Rate on page 23).	Normal Mode (Operational); f_{SCLK} = 20MHz	V_{DD} = 4.75 to 5.25V			18.4	mW
			V_{DD} = 2.7 to 3.6V			10.1	mW
		Auto Shutdown Mode (Static)	V_{DD} = 4.75 to 5.25V			2.5	µW
			V_{DD} = 2.7 to 3.6V			1.5	µW

1. When bit RANGE = 0 and bit SE/FDN = 1, V_{REFIN} must not be larger than $V_{DD}/2$.

Timing Specifications

V_{DD} = 2.7 to 5.25V, VDRIVE ≤ V_{DD}, REFIN = 2.5V; T_{AMB} = -40 to +85°C (unless otherwise specified). Specifications based on load circuit shown in Figure 3 on page 8.

Table 4.

Symbol	Min	Typ	Max	Unit	Description
f_{SCLK}	0.01		20	MHz	SCLK frequency
t_{CP}	50			ns	SCLK periode
t_{QUIET}	50			ns	Minimum quiet time required between bus relinquish and next conversion start.
t_{CSS}	10			ns	CSN Fall to SCLK Fall Setup
t_{CSDOE}			20	ns	CSN Fall to DOUT Enabled.
t_{CSDOV}			40	ns	CSN Fall to DOUT Valid.
t_{CL}	0.4 t_{CP}			ns	SCLK Pulse Width Low.
t_{CH}	0.4 t_{CP}			ns	SCLK Pulse Width High.
t_{DOH}	10			ns	SCLK Fall to DOUT Hold.
t_{DOV}			50	ns	SCLK Fall to DOUT Valid.
t_{DOD}	15		50	ns	SCLK Fall to DOUT Disable.
t_{DS}	20			ns	DIN to SCLK Fall Setup.
t_{DH}	5			ns	DIN to SCLK Fall Hold.
t_{CSH}	20			ns	Sixteenth SCLK Fall to CSN Rise Hold.
t_{WAKEUP}			1	µs	Power-up time from auto shutdown mode.

Figure 3. Load Circuit for Digital Output Timing Specifications

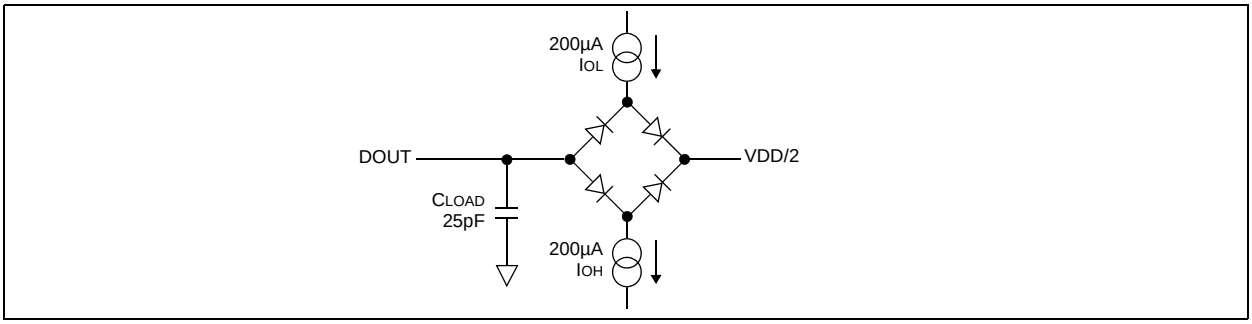
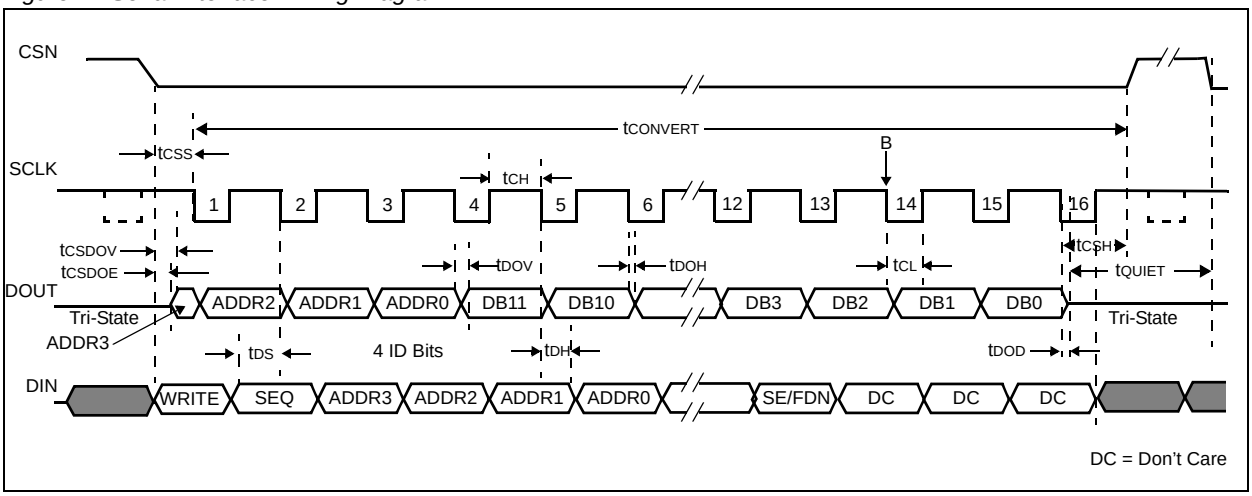


Figure 4. Serial Interface Timing Diagram



7 Typical Operating Characteristics

V_{DD} = 5.25V; V_{REF} = 2.5V, C_{REF} = 4.7µF, RANGE=1, SE/FDN=1, T_{AMB} = +25ºC (unless otherwise specified).

Figure 5. Integral Nonlinearity vs. Digital Output Code

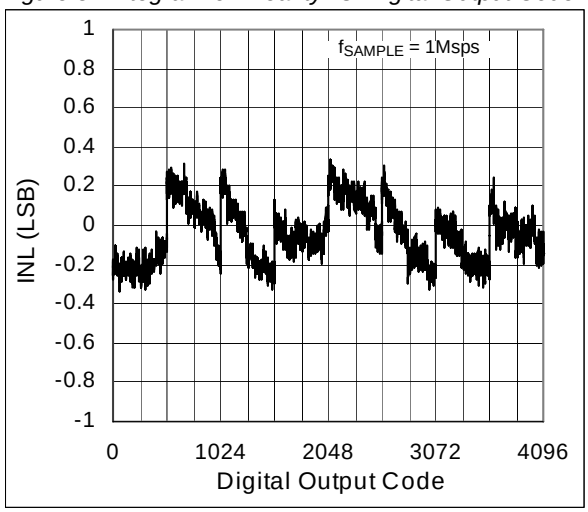


Figure 6. Differential Nonlinearity vs. Digital Output Code

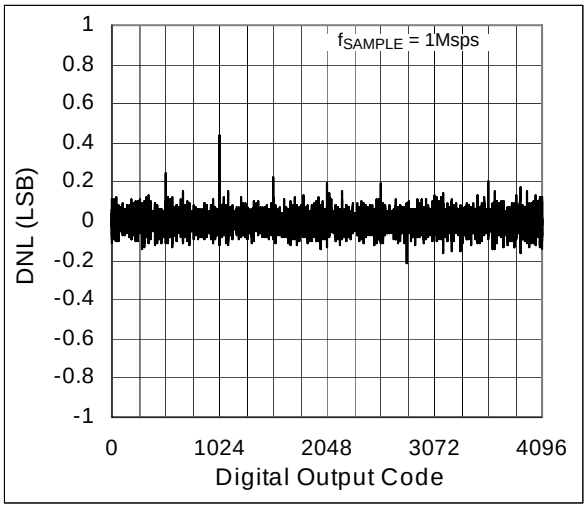


Figure 7. FFT @ 50kHz; RANGE=1, SE/FDN=1

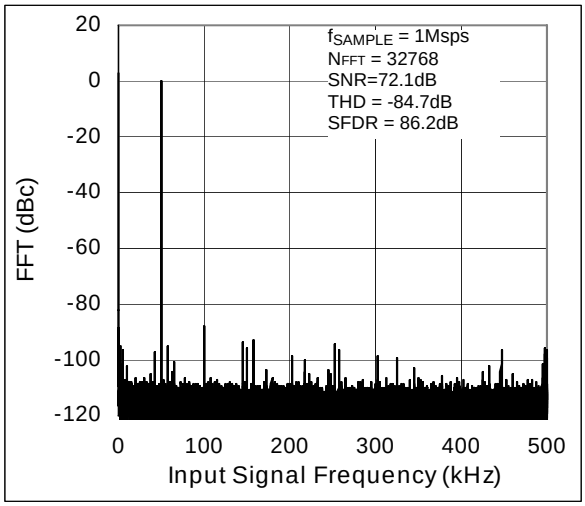


Figure 8. FFT @ 50kHz; RANGE=1, SE/FDN=0

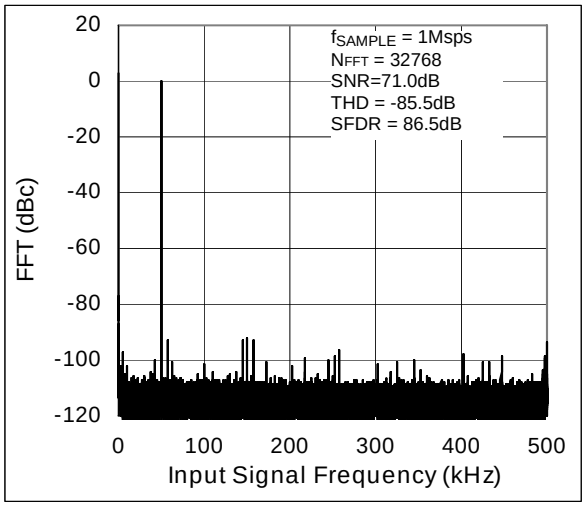


Figure 9. ENOB vs. V_{REFIN}; RANGE=1, SE/FDN=1

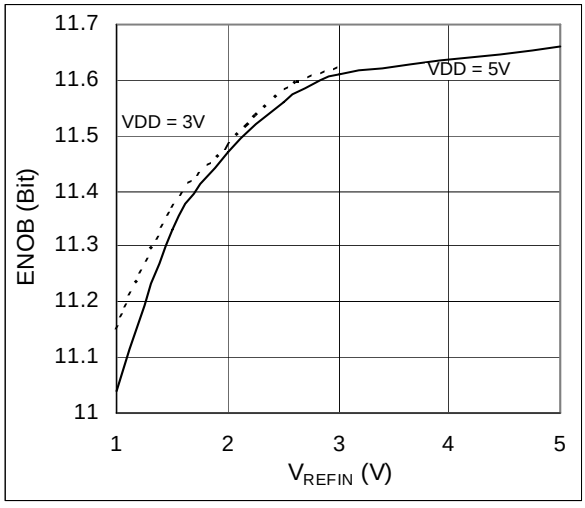


Figure 10. ENOB vs. Input Signal Frequency

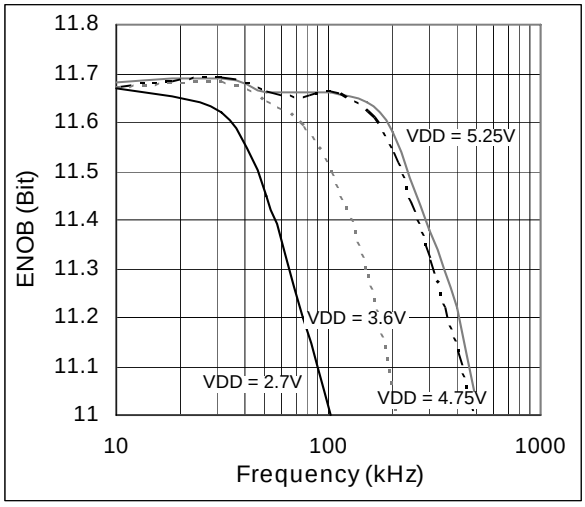


Figure 11. THD vs. Input Signal Frequency

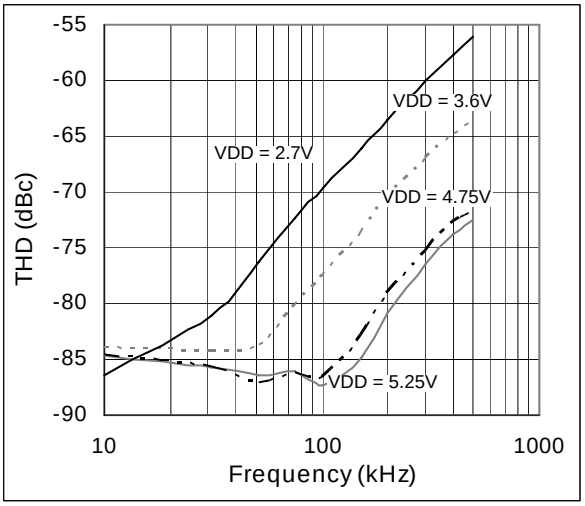


Figure 12. SINAD vs. Input Signal Frequency

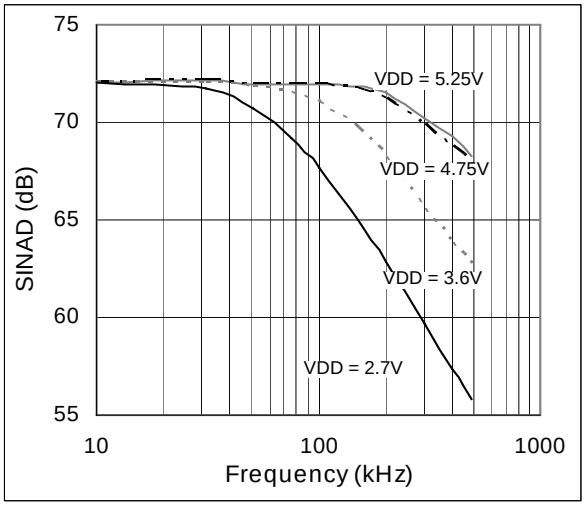


Figure 13. THD vs. Input Signal Frequency

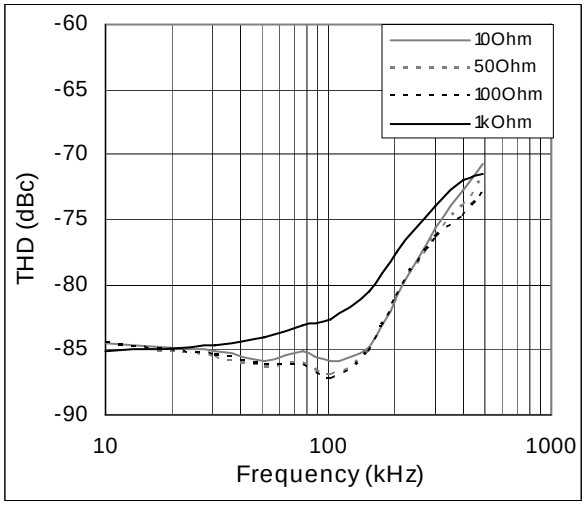


Figure 14. SINAD vs. Input Signal Frequency

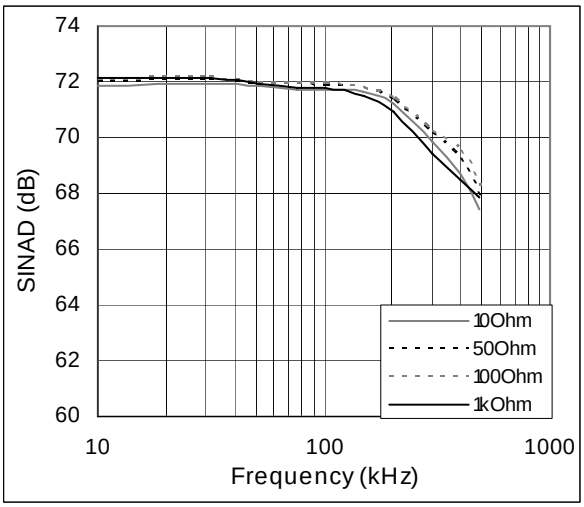


Figure 15. Supply Current vs. Supply Voltage

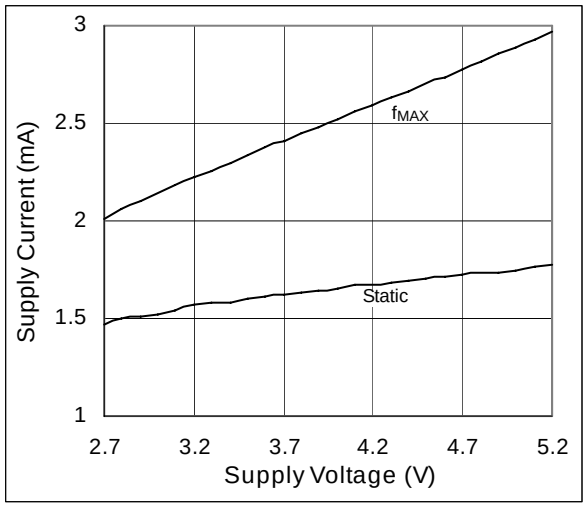


Figure 16. Supply Current vs. Temperature

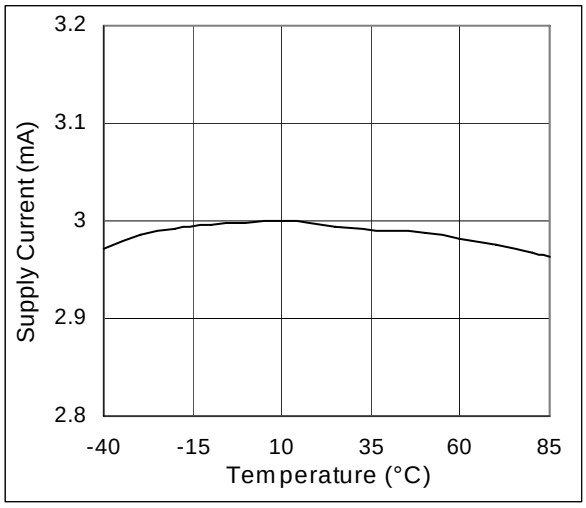


Figure 17. Shutdown Supply Current vs. V_{DD}

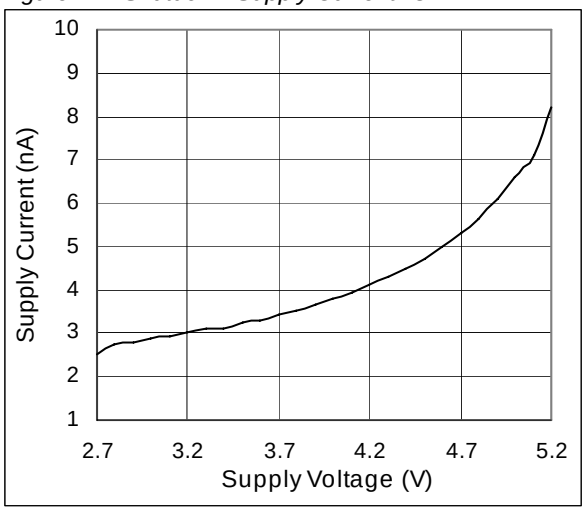


Figure 18. Shutdown Supply Current vs. Temp.

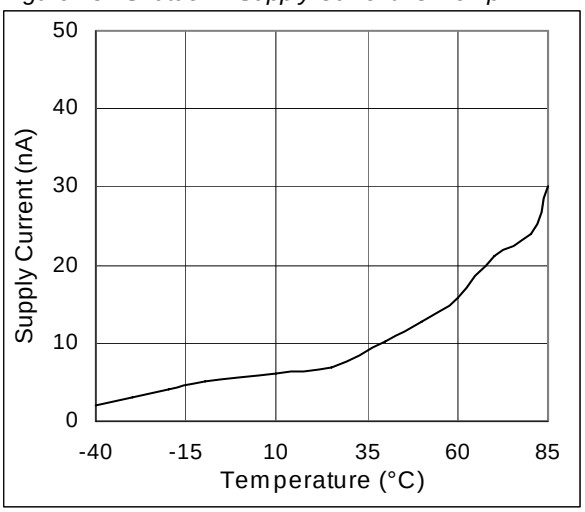


Figure 19. Supply Current vs. Throughput Rate

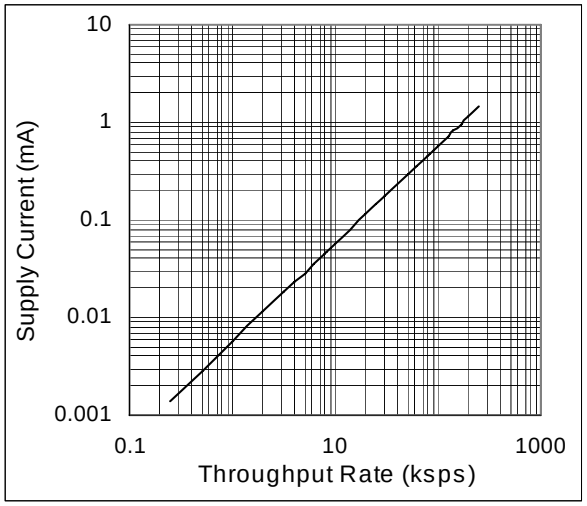
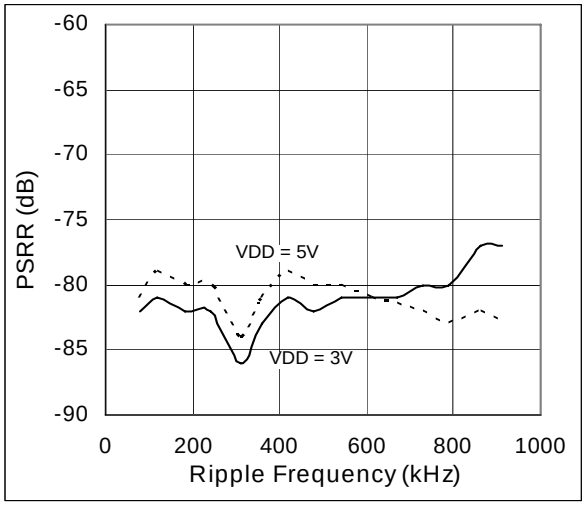


Figure 20. PSRR vs. Supply Signal Frequency



8 Detailed Description

The AS1543/44 is a fast, 8/4-channel, 12-bit, single-supply, A/D converter, which can be operated from a 2.7 to 5.25V supply. The AS1543/44 is capable of throughput rates of up to 1Msps when provided with a 20MHz clock. The AS1543/44 features on-chip track/hold, A/D converter, sequencer and a serial interface in a TQFN(4x4)-20 package.

The AS1543/44 has 8/4 single-ended or 4/2 fully-differential input channels with a channel sequencer, allowing the selection of the sequence of channels the ADC can cycle through on (each consecutive CSN falling edge). The serial clock input accesses data from the AS1543/44, controls the transfer of data written to the ADC, and provides the clock source for the successive-approximation A/D converter.

The analog input range for the AS1543/44 is [0 to V_{REFIN}] or [0V to 2 x V_{REFIN}] for 8/4 single ended input channels or [-V_{REFIN}/2 to +V_{REFIN}/2] or [-V_{REFIN} to +V_{REFIN}] for 4/2 fully differential input channels depending on the setting of bit RANGE (page 14) and SE/FDN (page 14). For the [0V to 2 x V_{REFIN}] mode, the device must be operated from a 4.75 to 5.25V supply.

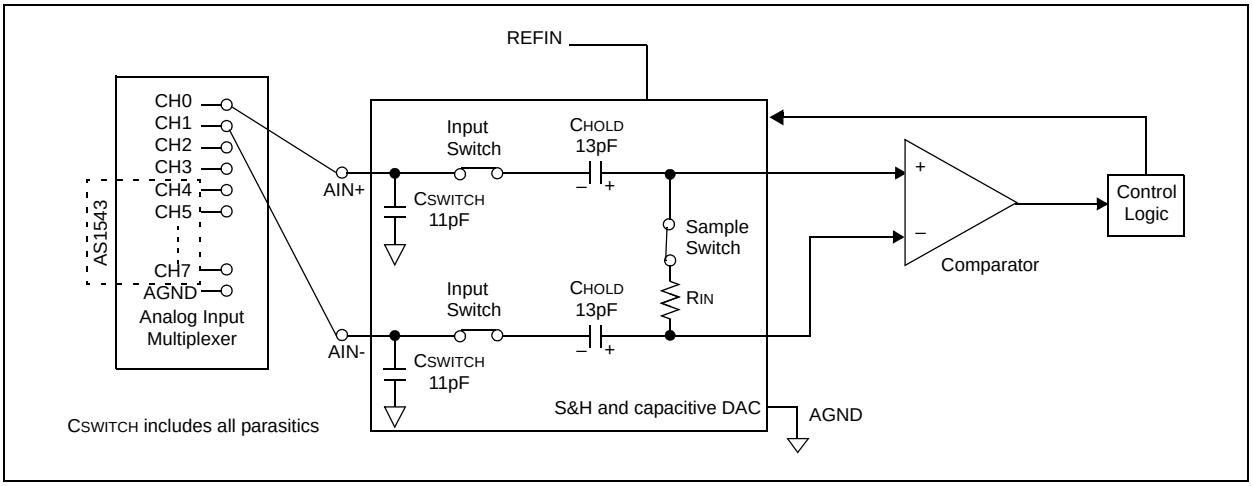
The AS1543/44 provides flexible power management options (see bits PM1, PM0 (page 14) of the control register) for the best power performance for a given throughput rate.

Converter Operation

The AS1543/44 is a 12-bit successive approximation analog-to-digital converter based around a capacitive DAC. The AS1543/44 can convert analog input signals in the range [0V to V_{REFIN}] or [0V to 2 x V_{REFIN}] or [-V_{REFIN}/2 to +V_{REFIN}/2] or [-V_{REFIN} to +V_{REFIN}] .

Figure 21 and Figure 22 show simplified diagrams of the ADC operation. The ADC circuitry is made up of control logic, SAR, and a capacitive DAC, which are used to redistribute fixed amounts of charge with the capacitive DAC to bring the comparator back into a balanced condition. Figure 21 shows the ADC during its acquisition phase. Sample switch and input switch are closed. The comparator is held in a balanced condition and the sampling capacitors C_{HOLD} acquires the signal on the selected V_{INx} channel.

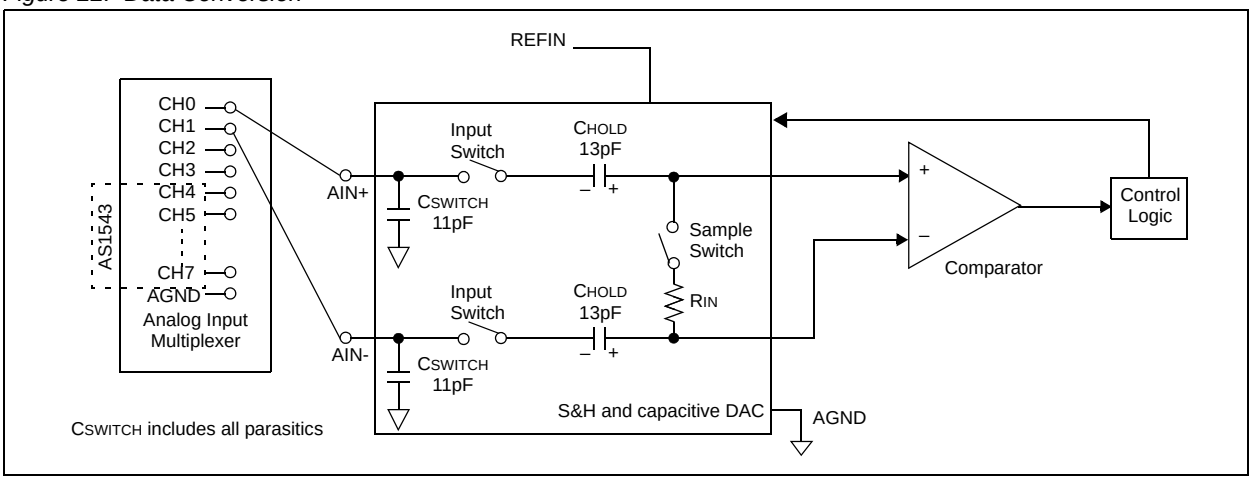
Figure 21. Data Acquisition



When a conversion is started (see Figure 22), sample switch and input switch opens causing the comparator to become unbalanced. The control logic and the capacitive DAC are used to redistribute fixed amounts of charge from the sampling capacitor to bring the comparator back into a balanced condition. When the comparator is re-balanced, the conversion is complete. Control logic generates the ADC output code.

See page 16 for the ADC transfer functions.

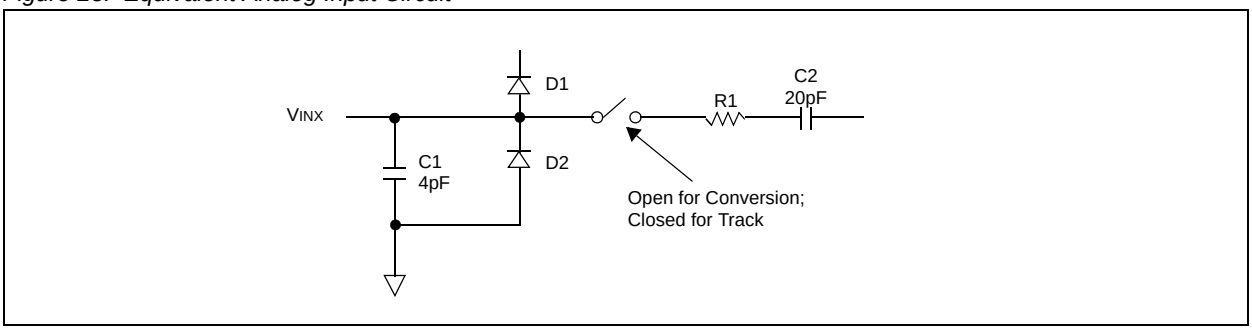
Figure 22. Data Conversion



Analog Input

Figure 23 shows an equivalent circuit of one analog input. The two diodes, D1 and D2, provide ESD protection for the analog inputs. Care should be taken to ensure that the analog input signal never exceeds the supply rails by more than 300mV. This will cause these diodes to become forward biased and start conducting current into the substrate. 10mA is the maximum current these diodes can conduct without causing irreversible damage to the AS1543/44.

Figure 23. Equivalent Analog Input Circuit



Capacitor C1 in Figure 23 is typically about 4pF and can primarily be attributed to pin capacitance. The resistor R1 is a lumped component made up of the on-resistance of a switch (track/hold switch) and also includes the on-resistance of the input multiplexer. The total resistance is typically about 400Ω. Capacitor C2 is the ADC sampling capacitor and typically has a capacitance of 20pF.

Track/Hold

The Track/Hold stage enters hold mode on the falling edge of CSN. For AC applications, removing high frequency components from the analog input signal is recommended by use of an R/C low-pass filter on the relevant analog input pin. In applications where harmonic distortion and signal-to-noise ratio are critical, the analog input should be driven from a low impedance source. Large source impedances will significantly affect the ac performance of the ADC. This may necessitate the use of an input buffer amplifier. The choice of the op-amp will be a function of the particular application.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance will depend on the amount of total harmonic distortion that can be tolerated. The THD will increase as the source impedance increases, and performance will degrade (see Figure 13 on page 10).

Control Register

The AS1543/44 control register is a 13-bit, write-only register. Data is loaded into the register from pin DIN on the falling edge of the SCLK signal. Data is transferred on pin DIN at the same time as the conversion result is read from the device. The data transferred on pin DIN corresponds to the AS1543/44 configuration for the next conversion. This requires 16 serial clocks for every data transfer.

Only the information provided on the first 13 falling clock edges (after CSN falling edge) is loaded to the control register. The control register bits are defined in Table 6.

Table 5. 12-Bit Control Register Format

12 (MSB)	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
WRITE	SEQ	ADDR3	ADDR2	ADDR1	ADDR0	PM1	PM0	SHADOW	WEAK/ TRIN	RANGE	CODING	SE/FDN

Table 6. Control Register Bit Definitions

Bit Number	Bit Name	Description
12	WRITE	Determines if the subsequent 12 bits will be loaded to the control register. 1 = The subsequent 12 bits will be written to the control register. 0 = The subsequent 12 bits are not loaded to the control register and its contents are unchanged.
11	SEQ	This bit is used in conjunction with the SHADOW bit to control the sequencer (see Table 11 on page 17) and access the shadow register (see page 18).
10:7	ADDR3:ADDR0	These four address bits and the bit SE/FDN are loaded at the end of the present conversion sequence, and select which single analog input or pair of input channels is to be converted in the next serial transfer. The selected input channel is decoded as shown in Table 8 on page 15. These bits also may select the final channel in a consecutive sequence as described in Table 11 on page 17. The address bits corresponding to the conversion result are also output on DOUT prior to the 12 bits of data (see Serial Interface on page 20). The next channel to be converted on will be selected by the multiplexer on the 14th SCLK falling edge.
6, 5	PM1, PM0	These two power management bits set the mode of operation of the AS1543/44 (see Table 10 on page 17).
4	SHADOW	This bit is used in conjunction with the SEQ bit to control the sequencer (see Table 11 on page 17) and access the shadow register (see page 18).
3	WEAK/TRIN	This bit selects the state of pin DOUT upon completion of the current serial transfer. 1 = DOUT will be weakly driven to the channel address specified by bit ADDR3 of the subsequent conversion. 0 = DOUT will return to tri-state at the end of the serial transfer (see Serial Interface on page 20).
2	RANGE	This bit selects the analog input range to be used for the subsequent conversion. This results in conjunction with bit SE/FDN in 4 possible analog input ranges, as explained in Table 7 on page 15
1	CODING	This bit selects the type of output coding to be used for the conversion result. 1 = The output coding for the next conversion is straight binary. 0 = The output coding for the next conversion is twos complement.
0	SE/FDN	This bit selects in conjunction with the adress bits ADDR3:ADDR0 the input channels to be used (see Table 8 on page 15). 1 = 8/4 single-ended input channels 0 = 4/2 fully-differential channels

Analog Input Configuration

Table 7. Analog Input Configuration via bits RANGE and SE/FDN

Analog Input Configuration	RANGE	SE/FDN	Comments
8/4-channel single-ended	1	1	V_{INx} from [0V to V_{REFIN}]
	0	1	V_{INx} from [0V to 2xV_{REFIN}]
4/2-channel fully-differential	1	0	V_{INx} - V_{INy} from [-V_{REFIN}/2 to +V_{REFIN}/2]
	0	0	V_{INx} - V_{INy} from [-V_{REFIN} to +V_{REFIN}]

Note: If bit RANGE = 0 and bit SE/FDN =1 V_{DD} must be at least two times larger than V_{REFIN}.

Input Channel Selection

The input channels for conversion are selected using control register bits ADDR3:ADDR0 and bit SE/FDN.

Table 8. Channel Selection via Bits ADDR3:ADDR0 and SE/FDN, AS1544

	ADDR3	ADDR2	ADDR1	ADDR0	Analog Input Channel SE/FDN = 1 (Single-Ended)	Analog Input Channel SE/FDN = 0 (Fully-Differential)
AS1544	X	X	0	0	V_{IN0}	V_{IN0} - V_{IN1}
	X	X	0	1	V_{IN1}	V_{IN1} - V_{IN0}
	X	X	1	0	V_{IN2}	V_{IN2} - V_{IN3}
	X	X	1	1	V_{IN3}	V_{IN3} - V_{IN2}

Table 9. Channel Selection via Bits ADDR3:ADDR0 and SE/FDN, AS1543

	ADDR3	ADDR2	ADDR1	ADDR0	Analog Input Channel SE/FDN = 1 (Single-Ended)	Analog Input Channel SE/FDN = 0 (Fully-Differential)
AS1543	X	0	0	0	V_{IN0}	V_{IN0} - V_{IN1}
	X	0	0	1	V_{IN1}	V_{IN1} - V_{IN0}
	X	0	1	0	V_{IN2}	V_{IN2} - V_{IN3}
	X	0	1	1	V_{IN3}	V_{IN3} - V_{IN2}
	X	1	0	0	V_{IN4}	V_{IN4} - V_{IN5}
	X	1	0	1	V_{IN5}	V_{IN5} - V_{IN4}
	X	1	1	0	V_{IN6}	V_{IN6} - V_{IN7}
	X	1	1	1	V_{IN7}	V_{IN7} - V_{IN6}

Transfer Functions

Output coding and transfer function depend on the control register bits RANGE (page 14), SE/FDN (page 14) and CODING (page 14).

Figure 24. Straight Binary Transfer Function for SE/FDN = 1 and CODING = 1

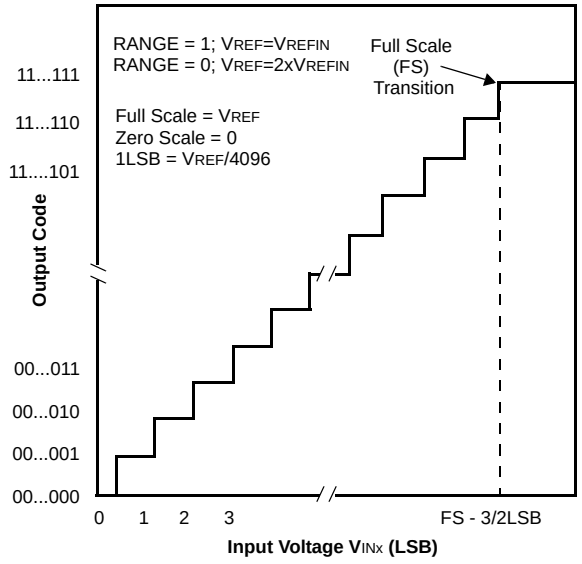


Figure 25. Straight Binary Transfer Function for SE/FDN = 0 and CODING = 1

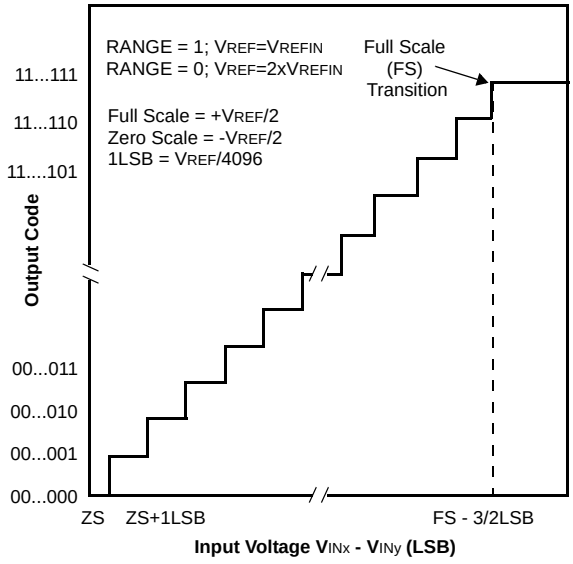


Figure 26. Two's Complement Transfer Function for SE/FDN = 1 and CODING = 0

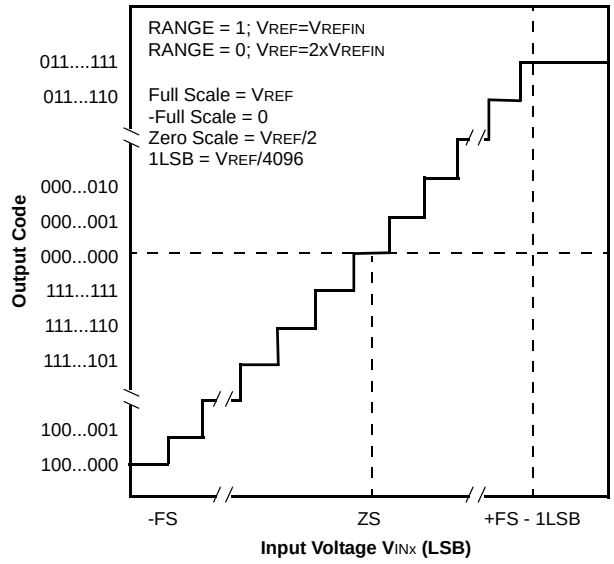
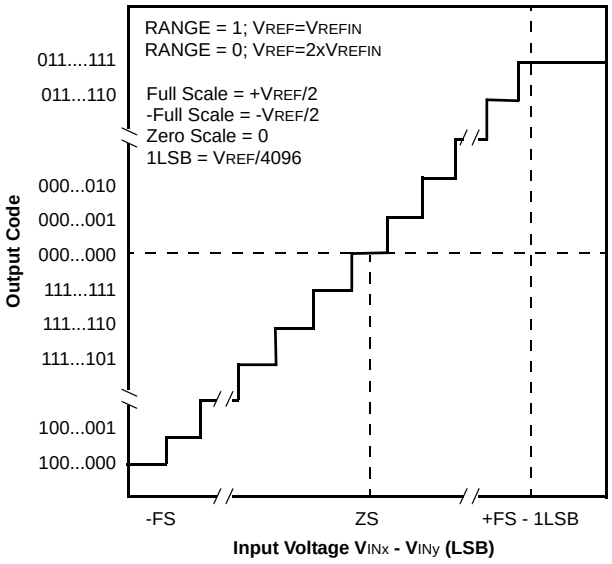


Figure 27. Two's Complement Transfer Function for SE/FDN = 0 and CODING = 0



Power Mode Selection

Control register bits PM1 and PM0 are used to configure the AS1543/44 power mode.

Table 10. Power Mode Selection via Bits PM1 and PM0

PM1	PM0	Mode	Description
1	1	Normal Operation	In this mode, the AS1543/44 remains in full power mode regardless of the status of any of the logic inputs. This mode allows the fastest possible throughput rate.
0	X	Auto Shutdown	In this mode, the AS1543/44 automatically enters shutdown mode at the end of each conversion when the control register is updated. Wake-up time from shutdown is 1µs. **Note:** Ensure that 1µs has elapsed before attempting to perform a valid conversion in this mode.

Sequencer Operation

The setting of control register bits SEQ and SHADOW sets the sequencer operation and also selects the shadow register for programming.

Table 11. Sequencer Configuration via Bits SEQ and SHADOW

SEQ	SHADOW	Description
0	0	These settings indicate that the sequencer is not used. The analog input channel selected for each individual conversion is determined by the contents of the channel address bits ADDR3:ADDR0 (page 14) in each prior write operation. This mode of operation reflects the normal operation of a multi-channel ADC (without the sequencer) where each write to the AS1543/44 specifies the next input channel for conversion (see Figure 28 on page 18).
0	1	These settings select the shadow register for programming. After a write to the control register, the following write operation will load the contents of the shadow register. This will program the sequence of channels to be repeatedly converted each successive valid CSN falling edge (see Table 12 on page 18 and Figure 29 on page 19). **Note:** The specified input channels need not be consecutive.
1	0	With these settings, the sequencer will not be interrupted upon completion of a write operation. This allows other bits of the control register (PM1, PM0, WEAK/TRIN, RANGE, CODING and SE/FDN) to be altered while in a sequence without terminating the cycle.
1	1	These settings are used in conjunction with the channel address bits ADDR3:ADDR0 to program continuous conversions on a consecutive sequence of channels (channel 0 ... channel *n*) as determined by the address bits ADDR3:ADDR0 (page 14) of the control register (see Figure 30 on page 20).

Shadow Register

The shadow register is a 16-bit, write-only register. Data is loaded from pin DIN of the AS1543/44 on the falling edge of SCLK. The data is transferred on pin DIN at the same time as a conversion result is read from the device. This requires 16 serial falling edges for the data transfer.

The information is clocked into the shadow register (provided bits SEQ (page 14) and SHADOW (page 14) were set to 0, 1 respectively), in the previous write to the control register.

Each bit represents one of the input channels (V_{IN0} through V_{IN3}/V_{IN7}). Multiple channels can be selected for continuous cycling on each consecutive CSN falling edge after a write to the shadow register. To select a sequence of channels, the associated bit must be set for each analog input channel.

The AS1543/44 will continuously cycle through the selected channels in ascending order, beginning with the lowest channel, until a write operation occurs (i.e., bit WRITE (page 14) is set to 1) with bits SEQ and SHADOW configured in any way except 1, 0 (see Table 11 on page 17).

Table 12. 16-Bit Shadow Register Format, AS1543

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
V_{IN0}	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN4}	V_{IN5}	V_{IN6}	V_{IN7}	V_{IN0}	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN4}	V_{IN5}	V_{IN6}	V_{IN7}

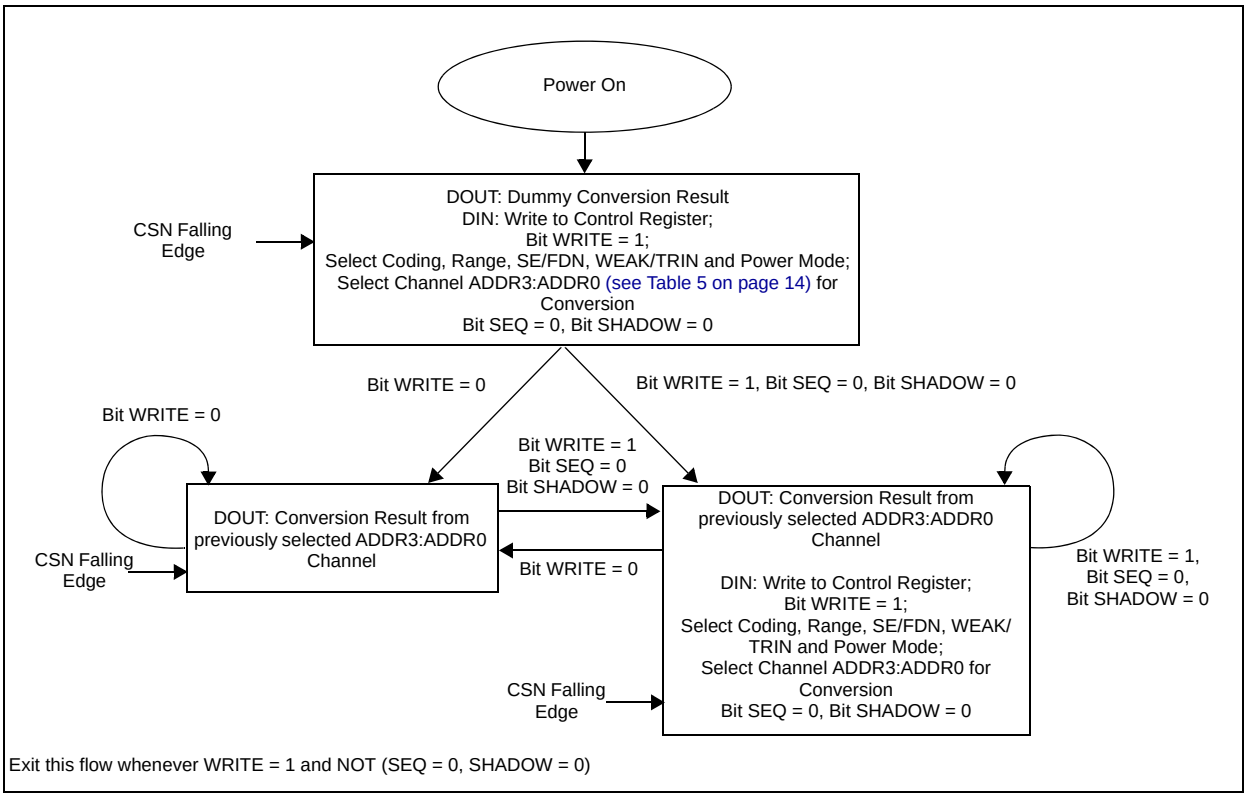
Table 13. 16-Bit Shadow Register Format, AS1544

15 (MSB)	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0 (LSB)
V_{IN0}	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN0}	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN0}	V_{IN1}	V_{IN2}	V_{IN3}	V_{IN0}	V_{IN1}	V_{IN2}	V_{IN3}

Direct Conversion (SEQ = 0, SHADOW = 0)

Figure 28 shows the normal flow of an ADC with multiple input channels selected, where each serial transfer selects the next channel for conversion. In this mode of operation, the sequencer function is not used.

Figure 28. Bit SEQ = 0, Bit SHADOW = 0 Flowchart

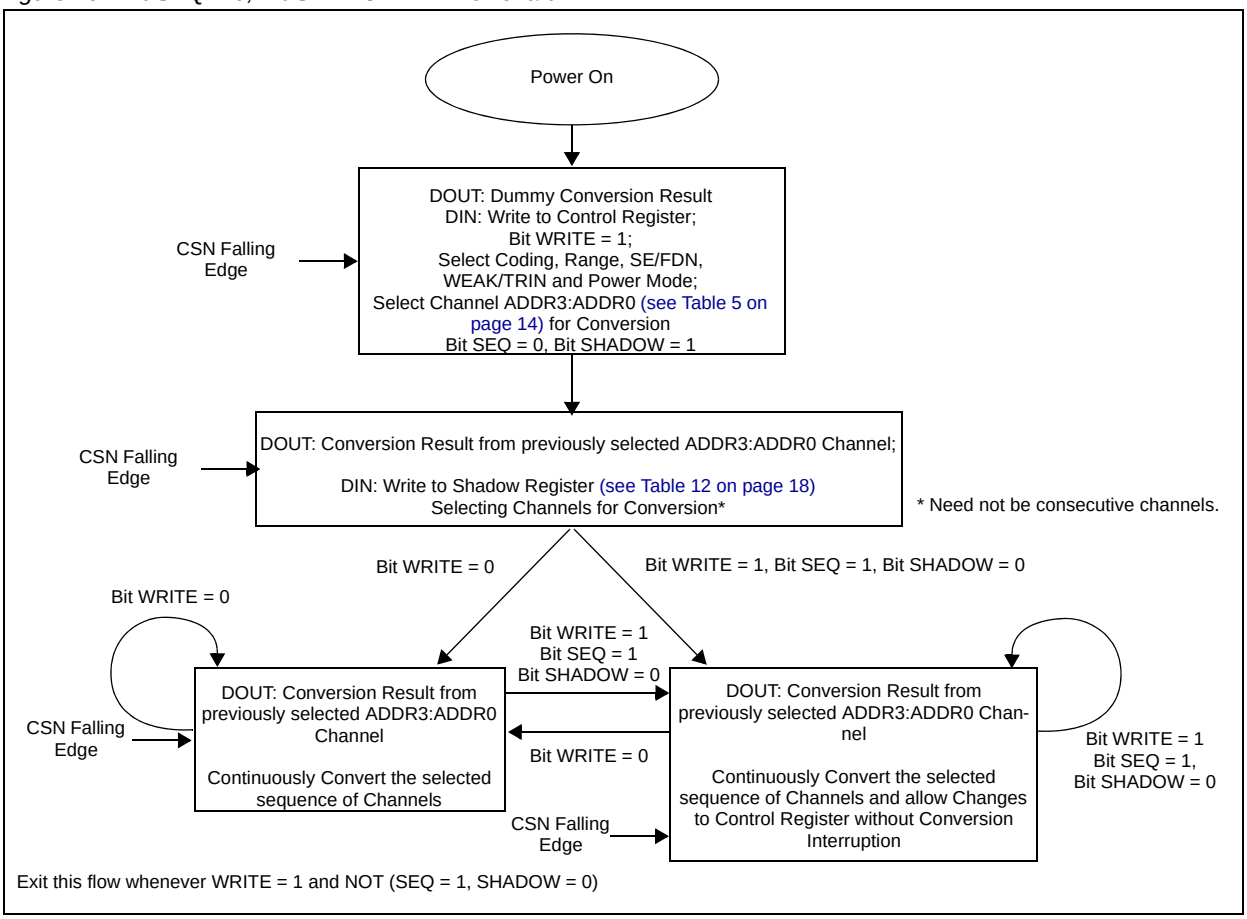


Shadow Register Conversion (SEQ = 0, SHADOW = 1)

Figure 29 shows how to program the AS1543/44 to continuously convert from a particular sequence of channels. To exit this mode of operation and revert back to the normal mode of operation of a multi-channel ADC (as outlined in Figure 28), verify bit WRITE (page 14) = 1 and bits SEQ and SHADOW = 0 on the next serial transfer.

Note: If all 0s are written into the Shadow Register (see Table 12 on page 18) channel 3/7 will be chosen by default.

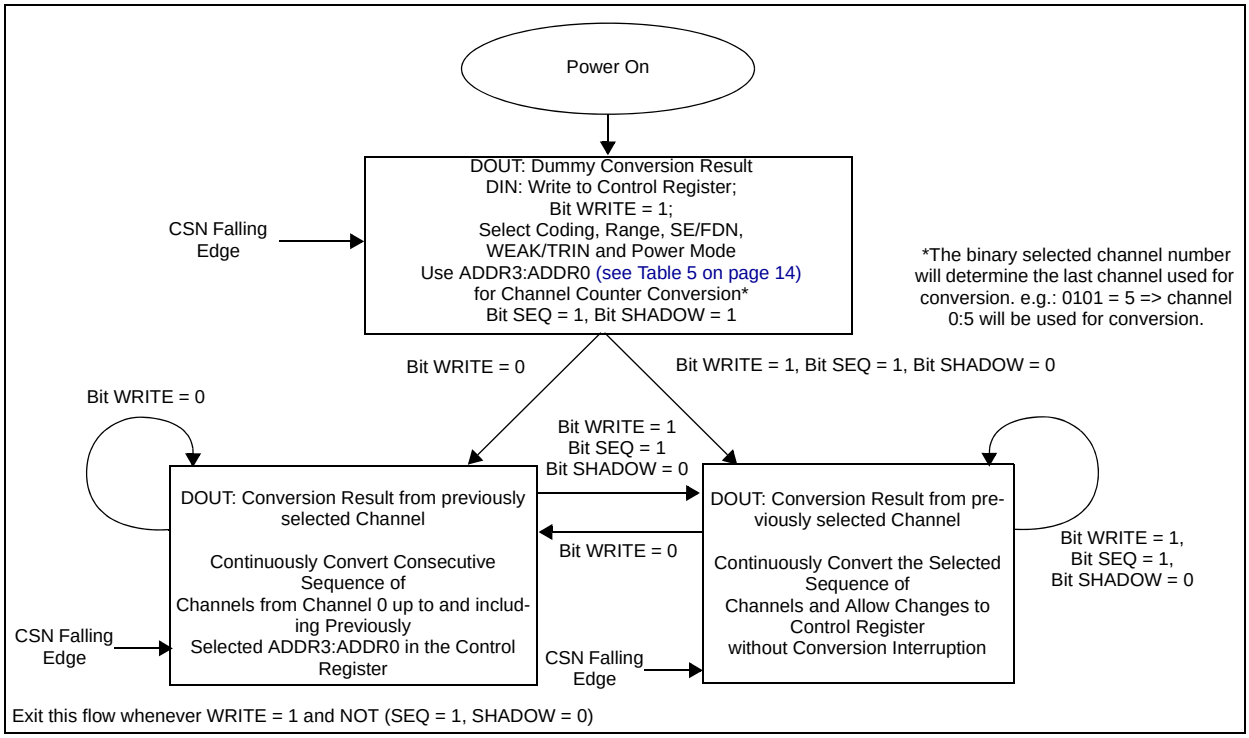
Figure 29. Bit SEQ = 0, Bit SHADOW = 1 Flowchart



Channel Counter Conversion (SEQ = 1, SHADOW = 1)

Figure 30 shows how a sequence of consecutive channels can be converted from without having to program the shadow register or write to the part on each serial transfer. To exit this mode of operation and revert back to the normal mode of operation of a multi-channel ADC (as outlined in Figure 29), verify bit WRITE (page 14) = 1 and bits SEQ and SHADOW = 0 on the next serial transfer.

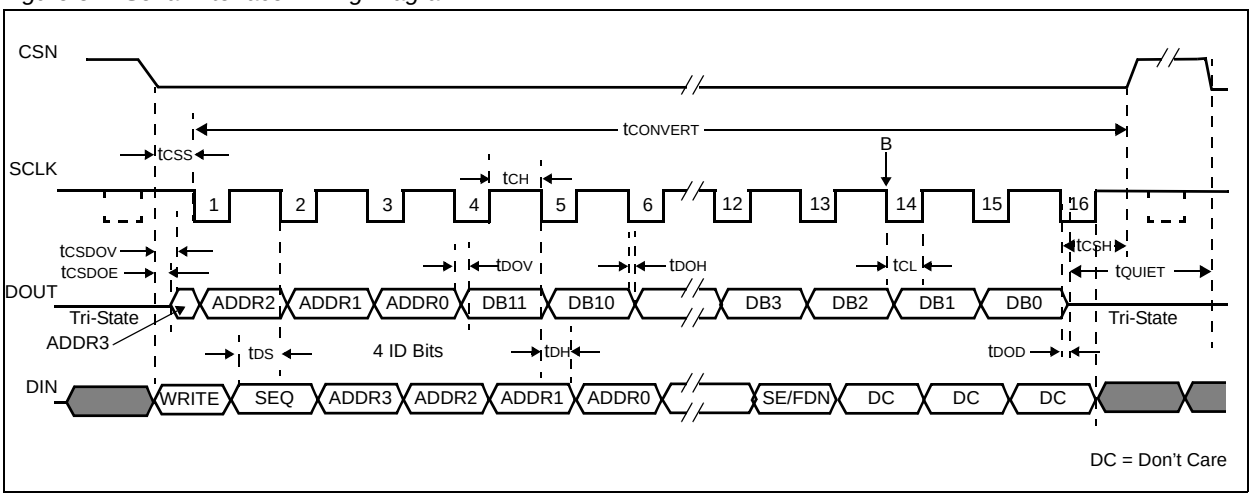
Figure 30. Bit SEQ = 1, Bit SHADOW = 1 Flowchart



Serial Interface

Figure 31 shows the detailed timing diagram for serial interfacing to the AS1543/44. The serial clock provides the conversion clock and also controls the transfer of information to and from the AS1543/44 during each conversion.

Figure 31. Serial Interface Timing Diagram



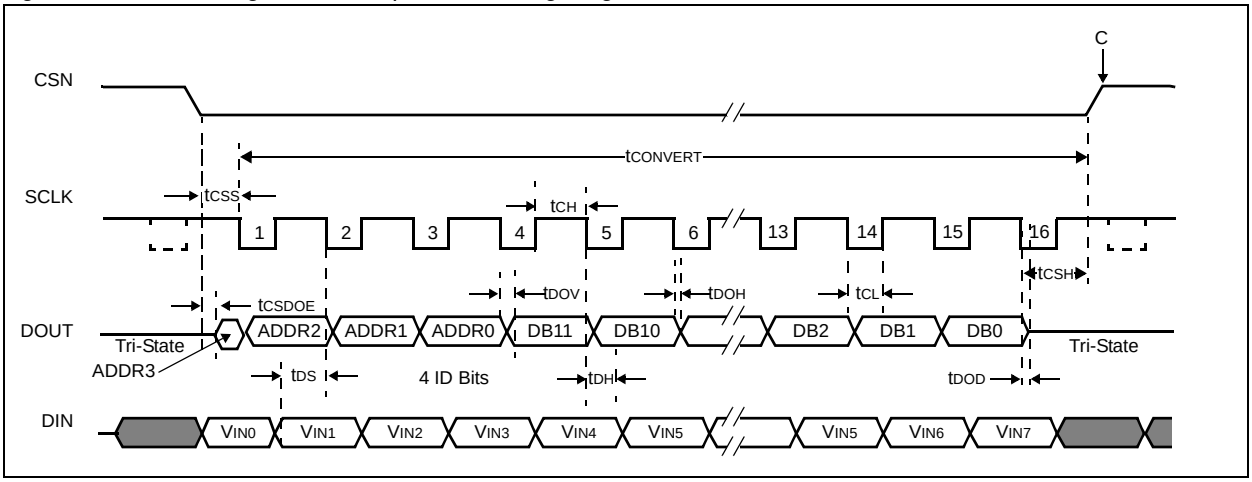
The CSN signal initiates the data transfer and conversion process. The falling edge of CSN puts the track and hold into hold mode, takes the bus out of three-state, and the analog input is sampled at this point. The conversion is also initiated at this point and will require 16 SCLK cycles to complete.

The track and hold will go back into track on the 14th SCLK falling edge (point B in Figure 31) except when the write is to the shadow register, in which case the track and hold will not return to track until the rising edge of CSN, (point C in Figure 32).

On the 16th SCLK falling edge, signal DOUT will go back into tri-state (assuming bit WEAK/TRIN (page 14) is set to 0). Sixteen serial clock cycles are required to perform the conversion process and to access data from the AS1543/44. The 12 bits of data are preceded by the four channel address bits ADDR3:ADDR0 (page 14), identifying which channel the conversion result corresponds to.

CSN going low provides address bit ADDR3 to be read in by the microprocessor or DSP. The remaining address bits and data bits are then clocked out by subsequent SCLK falling edges beginning with the second address bit ADDR2; thus the first SCLK falling edge on the serial clock has address bit ADDR3 provided and also clocks out address bit ADDR2. The final bit in the data transfer is valid on the 16th falling edge, having being clocked out on the previous (15th) falling edge.

Figure 32. Shadow Register Write Operation Timing Diagram, AS1543



Writing information to the control register takes place on the first 13 falling edges of SCLK in a data transfer, assuming the MSB, i.e., bit WRITE (page 14), has been set to 1. If the control register is programmed to use the shadow register, writing of information to the shadow register will take place on all 16 SCLK falling edges in the next serial transfer (see Figure 32). The shadow register will be updated upon the rising edge of CSN and the track and hold will begin to track the first channel selected in the sequence.

Note: It is important to note that, if channel 7 (V_{IN7}) is active in the shadow register, 17 clocks will be needed during the programming of the shadow register. CSN will then go high after the 17th clock. In all other cases, 16 clocks will be enough to program the shadow register.

If bit WEAK/TRIN (page 14) is set to 1, rather than returning to true tri-state upon the 16th SCLK falling edge, the DOUT signal will instead be pulled weakly to the logic level corresponding to bit ADDR3 of the next serial transfer. This is done to ensure that the MSB of the next serial transfer is set up in time for the first SCLK falling edge after the CSN falling edge.

If bit WEAK/TRIN is set to 0 and the DOUT signal has been in true tri-state between conversions, then depending on the particular DSP or microcontroller interfacing to the AS1543/44, address bit ADDR3 may not be set up in time for the DSP/micro to clock it in successfully. In this case, ADDR3 would only be driven from the falling edge of CSN and must then be clocked in by the DSP on the following falling edge of SCLK.

However, if bit WEAK/TRIN is set to 1, then although DOUT is driven with address bit ADDR3 since the last conversion, it is nevertheless so weakly driven that another device may still take control of the bus. It will not lead to a bus contention (e.g., a 10 kΩ pull-up or pull-down resistor would be sufficient to overdrive the logic level of ADDR3 between conversions) and all 16 channels may be identified. However, if this does happen and another device takes control of the bus, it is not guaranteed that DOUT will be fully driven to ADDR3 again in time for the read operation when control of the bus is taken back.

This is useful if using an automatic sequence mode to identify channel-result pairs. Obviously, if only the first eight channels are in use, then address bit ADDR3 does not need to be decoded, and whether it is successfully clocked in as a 1 or 0 will not matter as long as it is still counted by the DSP as the MSB of the 16-bit serial transfer.

Power Modes

The AS1543/44 can be operated in 2 different modes:

- Normal Mode (see page 22)
- Auto Shutdown (see page 23)

These modes are designed to provide flexible power management options, and can be selected to optimize the power dissipation and throughput-rate ratio for differing application requirements. The mode of operation of the AS1543/44 is controlled by bits PM1, PM0 (page 14) of the control register.

Note: When power supplies are first applied to the AS1543/44, internal power-on reset circuitry sets the device for Auto Shutdown (PM1 = 0, PM0 = x). The AS1543/44 remains in shutdown the first CSN falling edge is received.

Normal Mode (PM1 = 1, PM0 = 1)

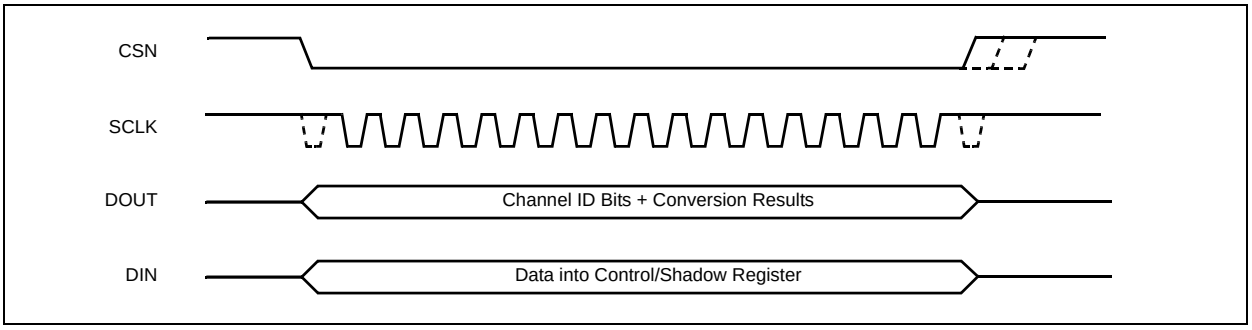
This mode is intended for the fastest throughput rate performance as the user does not have to worry about any power-up times with the AS1543/44 remaining fully powered at all times. Figure 33 shows the operation of the AS1543/44 in normal mode.Conversion is initiated on the falling edge of CSN and the track and hold will enter hold mode.

The data presented to pin DIN during the first 13 clock cycles of the data transfer is loaded to the control register (if bit WRITE (page 14) is set to 1). If bit SEQ (page 14) = 0, and bit SHADOW (page 14) = 1 on the previous write, data presented on pin DIN during the first 16 SCLK cycles is loaded into the shadow register. The device will remain fully powered up in normal mode at the end of the conversion as long as bits PM1, PM0 (page 14) are set to 1 in the write transfer during that conversion.

To ensure continued operation in normal mode, bits PM1 and PM0 are loaded with 1 on every data transfer. Sixteen serial clock cycles are required to complete the conversion and access the conversion result. The track and hold will go back into track on the 14th SCLK falling edge.

Once a data transfer is complete (DOUT has returned to tri-state, bit WEAK/TRIN (page 14) = 0), another conversion can be initiated after the quiet time (t_{QUIET}) has elapsed by bringing CSN low again.

Figure 33. Normal Mode Operation



Notes:

1. Control register data is loaded on the 1st 13 SCLK cycles.
2. Shadow register data is loaded on the 1st 16 SCLK cycles.

Auto Shutdown (PM1 = 0, PM0 = X)

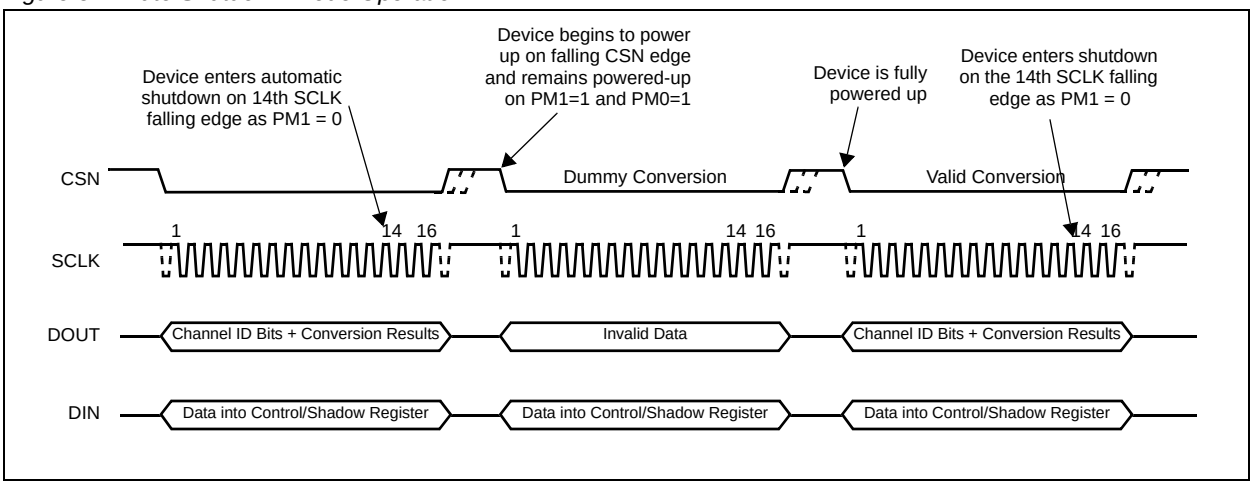
In this mode, the AS1543/44 automatically enters shutdown after the 14th SLK falling edge of each conversion is updated. When the device is in shutdown mode, the track/hold circuitry is in hold mode.

Note: The control register maintains its data while in shutdown mode.

Figure 34 shows the operation of the AS1543/44 when it is in automatic shutdown mode The AS1543/44 remains in shutdown until the next CSN falling edge it receives. On this CSN falling edge, the track and hold that was in hold while the device was in shutdown will return to track.

Note: Wake-up time from auto shutdown is 1µs.

Figure 34. Auto Shutdown Mode Operation



Notes:

1. Control register data is loaded on the 1st 13 SCLK cycles.
2. Set control register bits PM1 = 1 and PM0 = 1 to keep the device in normal mode.

When running the AS1543/44 with a 20MHz clock, one dummy cycle of 1µs (see Figure 34) (16 SCLKs plus Track&Hold aquisation time) should be sufficient to ensure the part is fully powered up.

This dummy cycle effectively halves the throughput rate, with every other conversion result being valid. In this mode, the power consumption of the part is greatly reduced with the part entering shutdown at the end of each conversion.

Note: The end of shutdown can be controlled by the CSN signal.

Power vs. Throughput Rate

By operating the AS1543/44 in auto shutdown (see page 23) the average power consumption of the ADC decreases at lower throughput rates. The Power vs. Throughput Rate graph in the Typical Operating Characteristics section shows how as the throughput rate is reduced, the part remains in its shutdown state longer and the average power consumption over time drops accordingly.

If the AS1543/44 is operated in a continuous sampling mode with a throughput rate of 100ksps and a SCLK of 20 MHz (V_{DD} = 5V), with bit PM1 (page 14) = 0, i.e., the device is in auto shutdown mode (see page 23), then the power consumption is calculated as follows:

The maximum power dissipation during normal operation is 18.4mW (V_{DD} = 5.25V). If the power-up time from auto shutdown is one dummy cycle (i.e., 1µs) and the remaining conversion time is another cycle (i.e., 1µs) then the AS1543/44 will dissipate approximately 18.4mW for 2µs during each conversion cycle. For the remainder of the conversion cycle (8µs), the device remains in shutdown mode. The AS1543/44 will dissipate approximately 2.5µW for the remaining 8µs of the conversion cycle. If the throughput rate is 100ksps, the cycle time is 10µs and the average power dissipated during each cycle is:

$$((2/10) \times 18.4mW) + ((8/10) \times 2.5\mu W) = 3.682mW \quad (EQ\ 1)$$

The Power vs. Throughput Rate graph in the Typical Operating Characteristics section shows the power vs. throughput rate when using the auto shutdown mode and auto standby mode with 5V supplies (similar power calculations can be done at 3V, althought the power is decreased even more when using 3V supplies).

VDRIVE

VDRIVE controls the serial interface voltage. VDRIVE allows easy interface to 3V and 5V processors. For example, if the AS1543/44 were operated with a VDD of 5V, pin VDRIVE could be powered from a 3V supply. The AS1543/44 has better dynamic performance with a VDD of 5V while still being able to interface to 3V processors.

Note: VDRIVE must not exceed VDD by more than 0.3V (see Absolute Maximum Ratings on page 4)

External Reference

An external reference source should be connected directly to the pin VREFIN of the AS1543/44. The external reference voltage can reach from 1V to VDD. The correlation between performance of the AS1543/44 and the reference voltage is shown in Figure 9 on page 9. However for specified performance the reference voltage has to stay at 2.5V ±1%. The analog input range depends on VREFIN and the setting of bit RANGE and bit SE/FDN of the control register (see Analog Input Configuration on page 15). Errors in the reference source will result in gain errors in the AS1543/44 transfer function and will add to the specified full scale errors of the device.

Note: A capacitor of at least 0.1µF should be placed on pin REFIN.

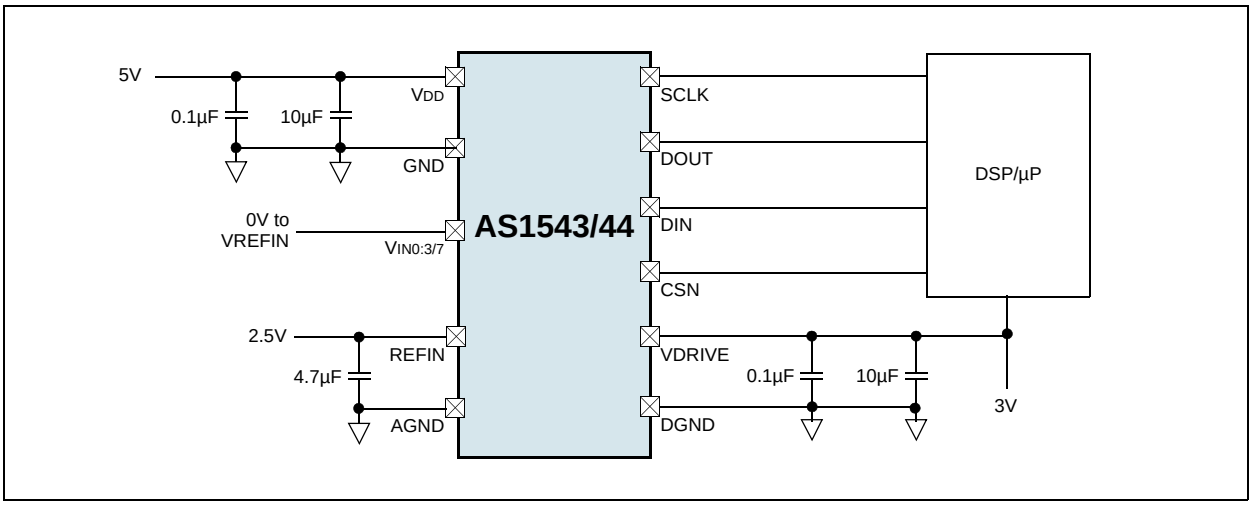
9 Application Information

Figure 35 shows a typical connection diagram for the AS1543/44. In this configuration, pin AGND, GND and DGND connected to the analog ground plane of the system. In Figure 35, REFIN is connected to a decoupled 2.5V reference source, to provide an analog input range of 0 to 2.5V (if RANGE (page 14) is 1 and bit SE/FDN (page 14) = 1) or 0 to 5V (if bit RANGE is 0 and bit SE/FDN = 1). In Figure 35 the AS1543/44 is connected to a V_{DD} of 5V, however the serial interface is connected to a 3V microprocessor.

Pin V_{DRIVE} is connected to the same 3V supply of the microprocessor to allow a 3V logic interface. The conversion result is output in a 16-bit word. This 16-bit data stream consists of four address bits indicating which channel the conversion result corresponds to, followed by the 12 bits of conversion data.

Note: For applications where power consumption is of concern, the power-down modes should be used between conversions or bursts of several conversions to improve power performance (see Power Modes on page 22).

Figure 35. Typical Application



Note: For the circuit shown in Figure 35, unused input channels should be connected to ground. For optimum performance decouple all analog input channels and the reference input voltage to the ground of AGND.

Initialisation

When power is first applied to the AS1543/44 interal power-on reset circuitry sets the device for Auto Shutdown (PM1 = 0, PM0 = X) on page 23.

Note: The device requires 10µs after the power supplies stabilize; no conversions should be initiated during this time.

The digital output at pin DOUT will be set to tri-state after internal power-on reset.

Grounding and Layout Considerations

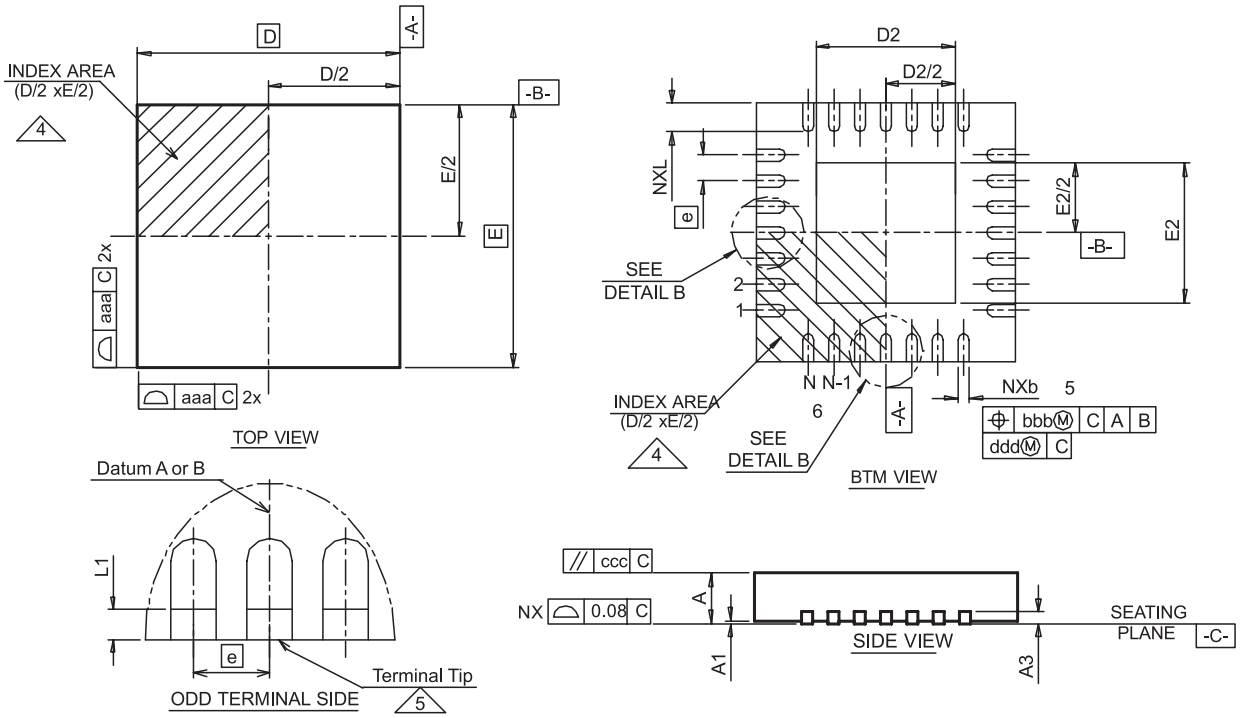
The AS1543/44 has excellent immunity to noise on the power supplies as can be seen by the PSRR vs. Supply Signal Frequency graph on page 11, however, the following should be considered regarding grounding and PCB layout:

- The PCB should be designed such that the analog and digital sections are confined to separate areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes as it gives the best shielding.
- Pins AGND and GND should be tied to the analog ground plane. Pin DGND should be tied to the digital ground plane.
- Digital and analog ground planes should be joined at only one place. If the AS1543/44 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point – a star ground point which should be established as close as possible to the AS1543/44.
- Avoid running digital lines under the device as these will couple noise onto the die.
- The analog ground plane should be allowed to run under the AS1543/44 to avoid noise coupling.
- The power supply lines to the AS1543/44 should use as large a trace as possible to provide low-impedance paths and reduce the effects of glitches on the power supply line.
- Fast-switching signals (e.g., clocks) should be shielded with digital ground to avoid radiating noise to other sections of the PCB.
- Clock signals should not be run near the analog inputs.
- Avoid crossover of digital and analog signals.
- Traces on opposite sides of the board should run at right angles to each other. This will reduce the effects of feedthrough through the board. A microstrip technique is the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.
- All analog input channels and the reference input voltage should be decoupled to the ground pin of AGND.
- All analog supplies should be decoupled with 10µF tantalum in parallel with 0.1µF capacitors to GND. To achieve the best from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. The 0.1µF capacitors should be low ESR and ESI (e.g., common ceramic or surface mount types) which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

10 Package Drawings and Markings

The device is available in an TQFN(4x4)-20 package.

Figure 36. TQFN(4x4)-20 Package



Symbol	Min	Typ	Max	Notes
A	0.70	0.75	0.80	1, 2
A1	0.00	0.02	0.05	1, 2
A3		REF		1, 2
L1	0.03		0.15	1, 2
aaa		0.10		1, 2
bbb		0.10		1, 2
ccc		0.10		1, 2
ddd		0.05		1, 2

Symbol	Min	Typ	Max	Notes
D BSC		4.00		1, 2
E BSC		4.00		1, 2
D2	2.00	2.15	2.25	1, 2
E2	2.00	2.15	2.25	1, 2
L	0.45	0.55	0.65	1, 2
b	0.18	0.25	0.30	1, 2, 5
e		0.5		
N		20		1, 2
ND		5		1, 2, 5

Notes:

1. Dimensioning and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters, angle is in degrees.
3. N is the total number of terminals.
4. Terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the area indicated. The terminal #1 identifier may be either a mold, embedded metal or mark feature.
5. Dimension b applies to metallized terminal and is measured between 0.15 and 0.30mm from terminal tip.
6. ND refers to the maximum number of terminals on D side.
7. Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

11 Ordering Information

The device is available as the standard products shown in Table 14.

Table 14. Ordering Information

Model	Marking	Description	Delivery Form	Package
AS1543-BTST	AS1543	8-Channel, 1 Msps, 12-Bit ADC with Sequencer	Tape and Reel	TQFN(4x4)-20
AS1544-BTST	AS1544	4-Channel, 1 Msps, 12-Bit ADC with Sequencer	Tape and Reel	TQFN(4x4)-20

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