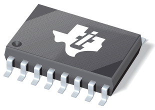


20MHz, Second-Order, Isolated Delta-Sigma Modulator for Current-Shunt Measurement

Check for Samples: AMC1204

FEATURES

- **±250mV Input Voltage Range Optimized for Shunt Resistors**
- **Certified Digital Isolation:**
  - **CSA, IEC60747-5-2, and UL1577 Approved**
  - **Isolation Voltage: 4000V_{PEAK}**
  - **Working Voltage: 1200V_{PEAK}**
  - **Transient Immunity: 15kV/µs**
- **Long Isolation Barrier Lifetime (see Application Report SLLA197)**
- **High Electromagnetic Field Immunity (see Application Note SLLA181A)**
- **Outstanding AC Performance:**
  - **SNR: 84dB (min)**
  - **THD: –80dB (max)**
- **Excellent DC Precision:**
  - **INL: ±8LSB (max)**
  - **Gain Error: ±2% (max)**
- **External Clock Input for Easier Synchronization**
- **Fully Specified Over the Extended Industrial Temperature Range**

APPLICATIONS

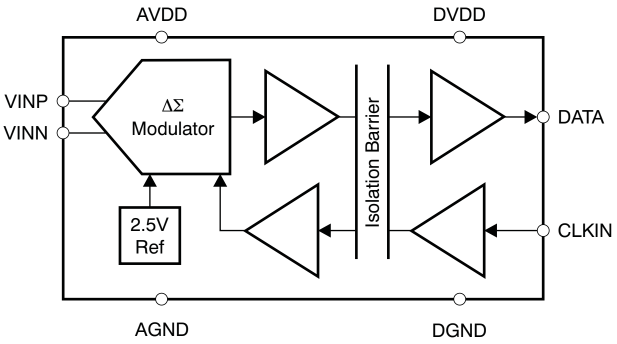
- **Shunt Resistor Based Current Sensing in:**
  - **Motor Control**
  - **Green Energy**
  - **Inverter Applications**
  - **Uninterruptible Power Supplies**

DESCRIPTION

The AMC1204 is a 1-bit digital output, isolated delta-sigma (ΔΣ) modulator that can be clocked at up to 20MHz. The digital isolation of the modulator output is provided by a silicon dioxide (SiO_2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide basic galvanic isolation of up to 4000V_{PEAK} according to UL1577, IEC60747-5-2, and CSA standards or specifications.

The AMC1204 provides a single-chip solution for measuring the small signal of a shunt resistor across an isolated barrier. These types of resistors are typically used to sense currents in motor control inverters, green energy generation systems, and other industrial applications. The AMC1204 differential inputs easily connect to the shunt resistor or other low-level signal sources. An internal reference eliminates the need for external components. When used with an appropriate external digital filter, an effective number of bits (ENOB) of 14 is achieved at a data rate of 78kSPS.

A 5V analog supply (AVDD) is used by the modulator while the isolated digital interface operates from a 3V, 3.3V, or 5V supply (DVDD). The AMC1204 is available in an SO-16 (DW) package and is specified from –40°C to +105°C.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

FAMILY OVERVIEW

PART NUMBER	MODULATOR CLOCK (MHz)	DIGITAL SUPPLY	CLOCK SOURCE	INL (LSB)	GAIN ERROR (%)	THD (dB)
AMC1203	10	5V	Internal	±9	±2	–84.5
AMC1203B	10	5V	Internal	±6	±1	–88
AMC1204	20	3V, 3.3V, or 5V	External	±8	±2	–80

ABSOLUTE MAXIMUM RATINGS(1)

Over the operating ambient temperature range, unless otherwise noted.

PARAMETER		AMC1204		UNIT
		MIN	MAX	
Supply voltage, AVDD to AGND or DVDD to DGND		–0.3	+6	V
Analog input voltage at VINP, VINN		AGND – 0.5	AVDD + 0.5	V
Digital input voltage at CLKIN		DGND – 0.3	DVDD + 0.3	V
Input current to any pin except supply pins		–10	+10	mA
Maximum virtual junction temperature, T_J			+150	°C
Operating ambient temperature range, T_{OA}		–40	+125	°C
Electrostatic discharge (ESD), all pins	Human body model (HBM) JEDEC standard 22, test method A114-C.01	–3000	+3000	V
	Charged device model (CDM) JEDEC standard 22, test method C101	–1500	+1500	V
	Machine model (MM) JEDEC standard 22, test method A115A	–200	+200	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Electrical Characteristics is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		AMC1204	UNITS
		DW	
		16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	78.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	41.3	
θ_{JB}	Junction-to-board thermal resistance	50.2	
ψ_{JT}	Junction-to-top characterization parameter	11.5	
ψ_{JB}	Junction-to-board characterization parameter	41.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

REGULATORY INFORMATION

VDE/IEC	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA component acceptance notice	Recognized under 1577 component recognition program
File number: 40016131	File number: 2350550	File number: E181974

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output (I/O) circuitry. A failure of the I/O circuitry can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

The safety-limiting constraint is the operating virtual junction temperature range specified in the Absolute Maximum Ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determine the junction temperature. The assumed junction-to-air thermal resistance in the Thermal Information table is that of a device installed in the JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages* and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = +78.5°C/W, V_I = 5.5V, T_J = +150°C, T_A = +25°C			10	mA
T_C	Maximum case temperature				+150	°C

IEC 61000-4-5 RATINGS

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOSM}	Surge immunity	1.2/50μs voltage surge and 8/20μs current surge	±6000	V

IEC 60664-1 RATINGS

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage ≤ 150V_{RMS}	I-IV
	Rated mains voltage < 300V_{RMS}	I-IV
	Rated mains voltage < 400V_{RMS}	I-III
	Rated mains voltage < 600V_{RMS}	I-III

ISOLATION CHARACTERISTICS

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IORM}	Maximum working insulation voltage per IEC		1200	V_{PEAK}
$V_{PD(t)}$	Partial discharge test voltage per IEC	t = 1s (100% production test), partial discharge < 5pC	2250	V_{PEAK}
V_{IOTM}	Transient overvoltage	t = 60s (qualification test)	4000	V_{PEAK}
		t = 1s (100% production test)	4000	V_{PEAK}
R_S	Isolation resistance	V_{IO} = 500V at T_S	> 10^9	Ω
PD	Pollution degree		2	Degrees

ISOLATOR CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal to terminal distance through air	7.9			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal to terminal distance across the package surface	7.9			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112/VDE 0303 part 1	≥ 175			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.014			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500V, all pins on each side of the barrier tied together to create a two-terminal device, T_A < +85°C		> 10^{12}		Ω
		Input to output, V_{IO} = 500V, +100°C ≤ T_A < T_A max		> 10^{11}		Ω
C_{IO}	Barrier capacitance input to output	$V_I = 0.8V_{PP}$ at 1MHz		1.2		pF
C_I	Input capacitance to ground	$V_I = 0.8V_{PP}$ at 1MHz		3		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of a specific application. Care should be taken to maintain the creepage and clearance distance of the board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal according to the measurement techniques shown in the *Isolation Glossary* section. Techniques such as inserting grooves and/or ribs on the PCB are used to help increase these specifications.

ELECTRICAL CHARACTERISTICS

All minimum/maximum specifications at T_A = –40°C to +105°C, AVDD = 4.5V to 5.5V, DVDD = 2.7V to 5.5V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted. Typical values are at T_A = +25°C, AVDD = 5V, and DVDD = 3.3V.

PARAMETER		TEST CONDITIONS	AMC1204			UNIT
			MIN	TYP	MAX	
T_A	Specified ambient temperature range		–40		+105	°C
RESOLUTION						
	Resolution		16			Bits
DC ACCURACY						
INL	Integral linearity error[1]	T_A = –40°C to +85°C	–8	±2	8	LSB
		T_A = –40°C to +105°C	-16	±5	16	LSB
DNL	Differential nonlinearity		–1		1	LSB
V_{OS}	Offset error[2]		–1	±0.1	1	mV
TCV_{OS}	Offset error thermal drift		–3.5	±1	3.5	μV/°C
G_{ERR}	Gain error[2]		–2	±0.5	2	%
TCG_{ERR}	Gain error thermal drift			±30		ppm/°C
PSRR	Power-supply rejection ratio			79		dB
ANALOG INPUTS						
FSR	Full-scale differential voltage input range	VINP – VINN		±320		mV
	Specified FSR		–250		250	mV
V_{CM}	Operating common-mode signal[3]		AGND		AVDD	V
C_I	Input capacitance to AGND	VINP or VINN		7		pF
C_{ID}	Differential input capacitance			3.5		pF
R_{ID}	Differential input resistance			12.5		kΩ
I_{IL}	Input leakage current	VINP – VINN = ±250mV	–10		10	μA
		VINP – VINN = ±320mV	-50		50	μA
CMTI	Common-mode transient immunity		15			kV/μs
CMRR	Common-mode rejection ratio	V_{IN} from 0V to 5V at 0Hz		108		dB
		V_{IN} from 0V to 5V at 100kHz		114		dB
EXTERNAL CLOCK						
t_{CLKIN}	Clock period		45.5	50	200	ns
f_{CLKIN}	Input clock frequency		5	20	22	MHz
$Duty_{CLKIN}$	Duty cycle	5MHz ≤ f_{CLKIN} < 20MHz	40	50	60	%
		20MHz ≤ f_{CLKIN} ≤ 22MHz	45	50	55	%
AC ACCURACY						
SINAD	Signal-to-noise + distortion	f_{IN} = 1kHz, T_A = –40°C to +85°C	78	87		dB
		f_{IN} = 1kHz, T_A = –40°C to +105°C	70	87		dB
SNR	Signal-to-noise ratio	f_{IN} = 1kHz, T_A = –40°C to +85°C	84	88		dB
		f_{IN} = 1kHz, T_A = –40°C to +105°C	83	88		dB
THD	Total harmonic distortion	f_{IN} = 1kHz, T_A = –40°C to +85°C		–96	–80	dB
		f_{IN} = 1kHz, T_A = –40°C to +105°C		-96	-70	dB
SFDR	Spurious-free dynamic range	f_{IN} = 1kHz, T_A = –40°C to +85°C	82	96		dB
		f_{IN} = 1kHz, T_A = –40°C to +105°C	72	96		dB
DIGITAL INPUTS[3]						
I_{IN}	Input current	V_{IN} = DVDD to DGND	–10		10	μA
C_{IN}	Input capacitance			5		pF
CMOS logic family			CMOS with Schmitt-trigger			
V_{IH}	High-level input voltage	DVDD = 4.5V to 5.5V	0.7DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage	DVDD = 4.5V to 5.5V	–0.3		0.3DVDD	V

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified 560mV input range.
(2) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(3) Ensured by design.

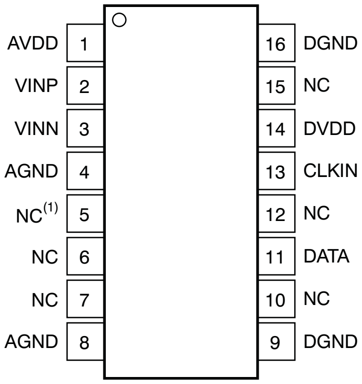
ELECTRICAL CHARACTERISTICS (continued)

All minimum/maximum specifications at T_A = –40°C to +105°C, AVDD = 4.5V to 5.5V, DVDD = 2.7V to 5.5V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted. Typical values are at T_A = +25°C, AVDD = 5V, and DVDD = 3.3V.

			AMC1204			
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
LVCMOS logic family			LVCMOS			
V_{IH}	High-level input voltage	DVDD = 2.7V to 3.6V	2		DVDD + 0.3	V
V_{IL}	Low-level input voltage	DVDD = 2.7V to 3.6V	–0.3		0.8	V
DIGITAL OUTPUTS(3)						
C_{OUT}	Output capacitance			5		V
C_{LOAD}	Load capacitance				30	V
CMOS logic family			CMOS			
V_{OH}	High-level output voltage	DVDD = 4.5V, I_{OH} = –100µA	4.4			V
V_{OL}	Low-level output voltage	DVDD = 4.5V, I_{OL} = +100µA			0.5	V
LVCMOS logic family			LVCMOS			
V_{OH}	High-level output voltage	I_{OH} = 20µA	DVDD – 0.1			V
		I_{OH} = –4mA, 2.7V ≤ DVDD ≤ 3.6V	DVDD – 0.4			V
		I_{OH} = –4mA, 4.5V ≤ DVDD ≤ 5.5V	DVDD – 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 20µA			0.1	V
		I_{OL} = 4mA			0.4	V
POWER SUPPLY						
AVDD	High-side supply voltage		4.5	5	5.5	V
DVDD	Controller-side supply voltage		2.7	3.3	5.5	V
I_{AVDD}	High-side supply current	4.5V ≤ AVDD ≤ 5.5V		11	16	mA
I_{DVDD}	Controller-side supply current	2.7V ≤ DVDD ≤ 3.6V		2	4	mA
		4.5V ≤ DVDD ≤ 5.5V		2.8	5	mA
P_D	Power dissipation	AVDD = 5.5V, DVDD = 3.6V		61.6	102.4	mW

PIN CONFIGURATION

DW PACKAGE
TSSOP-16
(TOP VIEW)



(1) NC = no internal connection.

PIN DESCRIPTIONS

PIN NAME	PIN#	FUNCTION	DESCRIPTION
AVDD	1	Power	High-side power supply
VINP	2	Analog input	Noninverting analog input
VINN	3	Analog input	Inverting analog input
AGND	4, 8(1)	Power	High-side ground
DGND	9, 16	Power	Controller-side ground
DATA	11	Digital output	Modulator data output
CLKIN	13	Digital input	Modulator clock input
DVDD	14	Power	Controller-side power supply
NC	5, 6, 7, 10, 12, 15	—	No internal connection; can be tied to any potential or left unconnected

(1) Both pins are connected internally via a low-impedance path; thus, only one of the pins must be tied to the ground plane.

TIMING INFORMATION

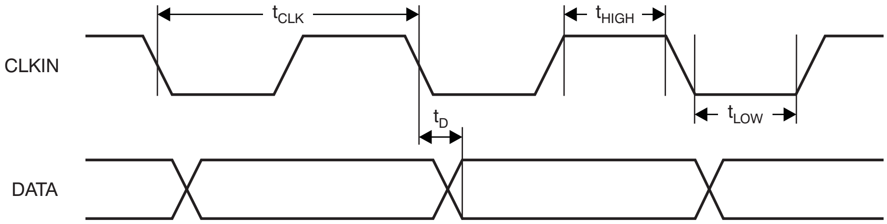


Figure 1. Modulator Output Timing

TIMING CHARACTERISTICS FOR Figure 1

Over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
t_{CLK}	CLKIN clock period	45.5	50	200	ns
t_{HIGH}	CLKIN clock high time	20	25	120	ns
t_{LOW}	CLKIN clock low time	20	25	120	ns
t_D	Delayed falling edge of CLKIN to DATA valid	2		15	ns

TYPICAL CHARACTERISTICS

At AVDD = 5V, DVDD = 3.3V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

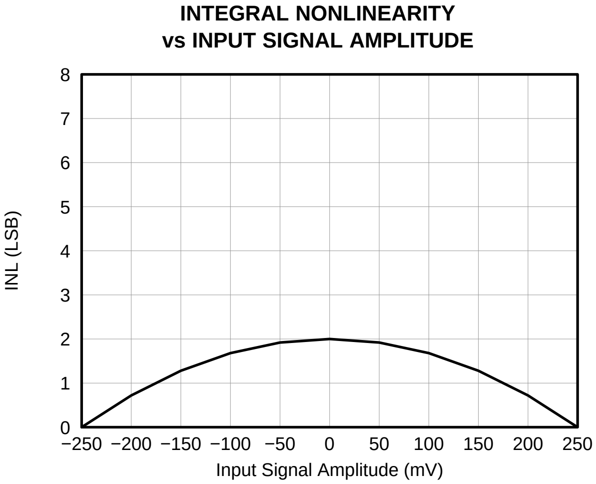


Figure 2.

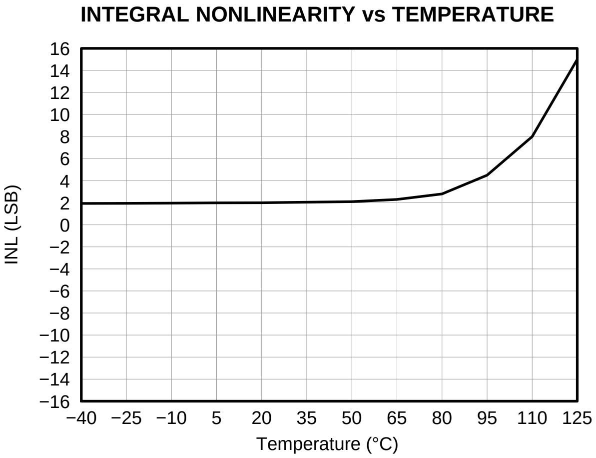


Figure 3.

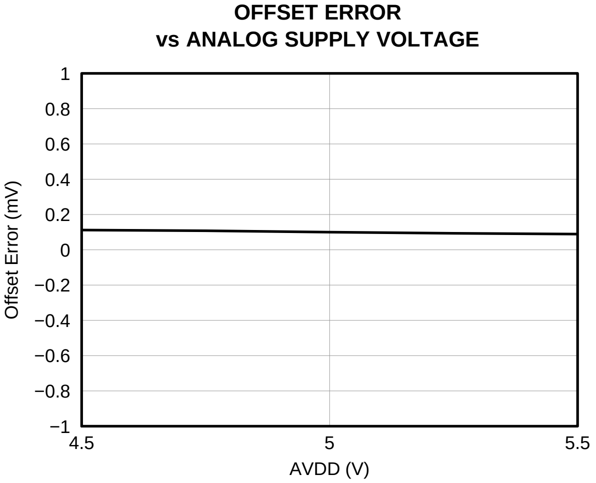


Figure 4.

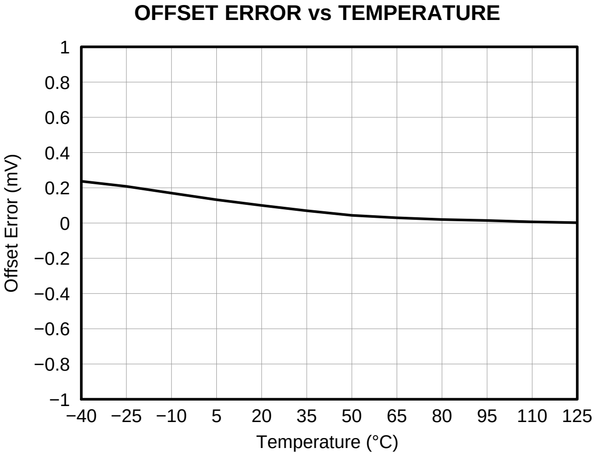


Figure 5.

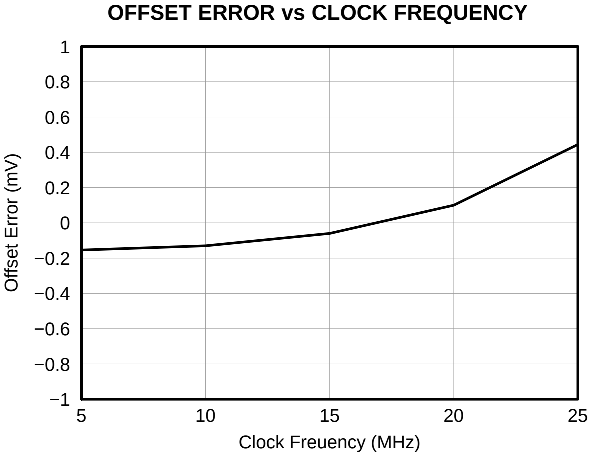


Figure 6.

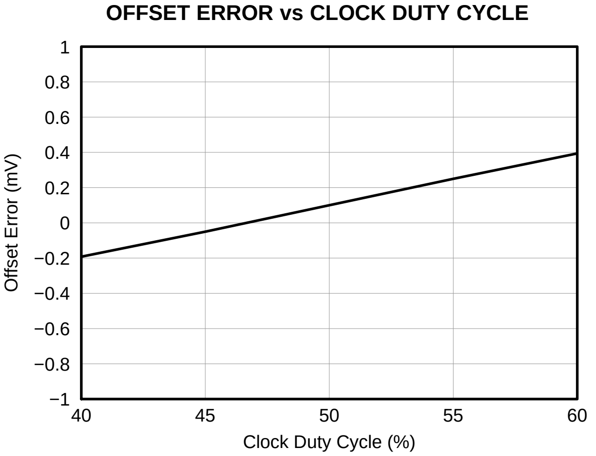


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, DVDD = 3.3V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

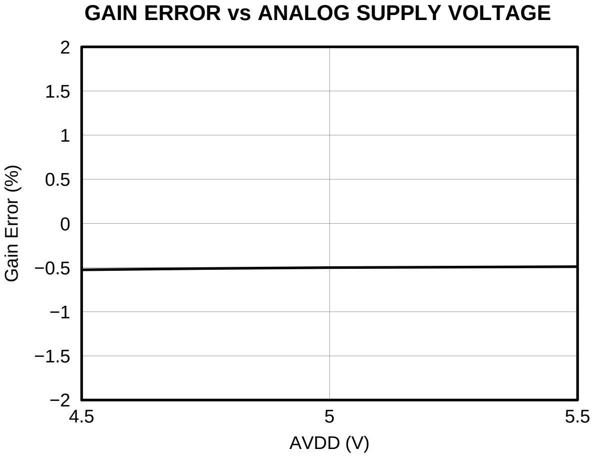


Figure 8.

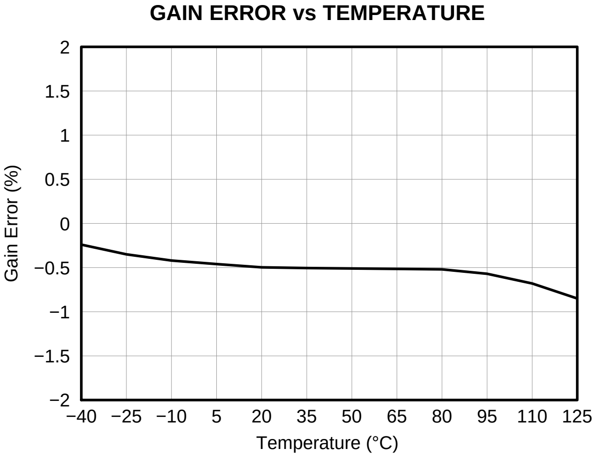


Figure 9.

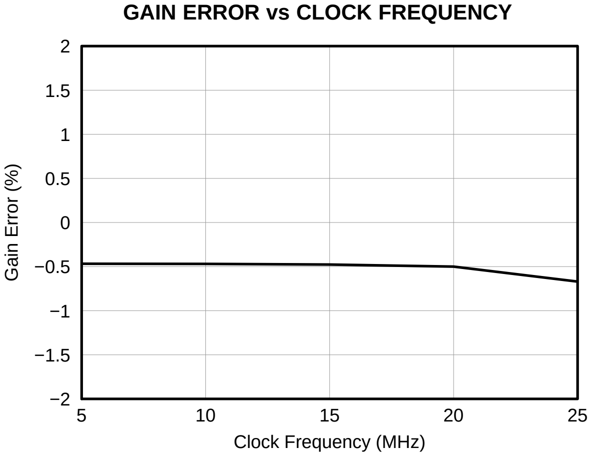


Figure 10.

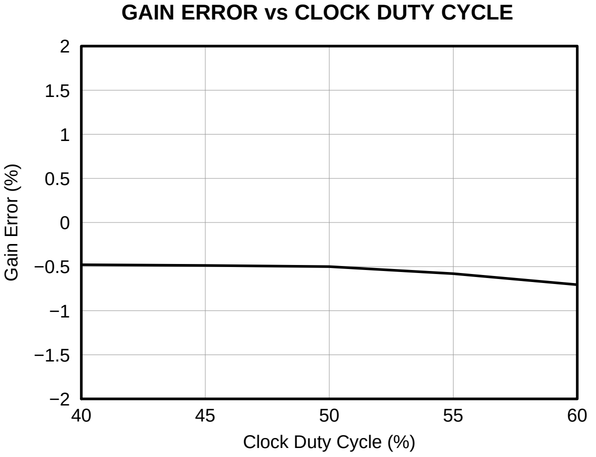


Figure 11.

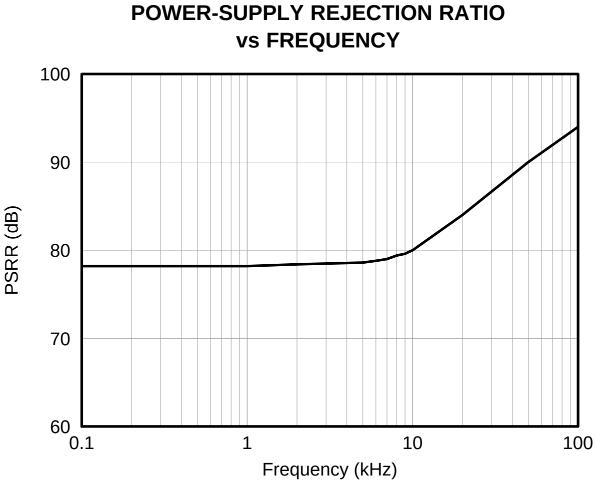


Figure 12.

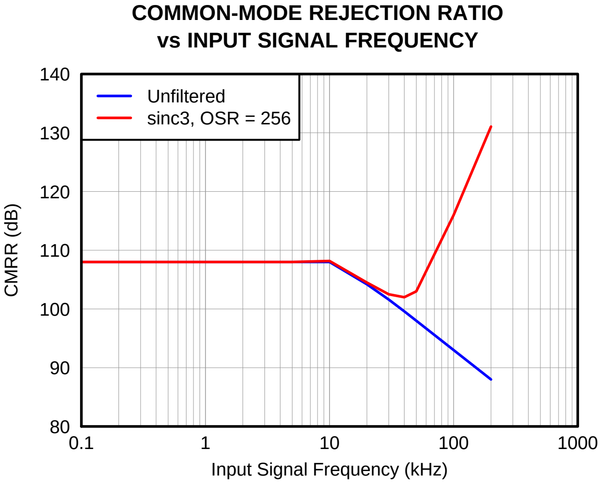


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, DVDD = 3.3V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

SINAD AND SNR vs ANALOG SUPPLY VOLTAGE

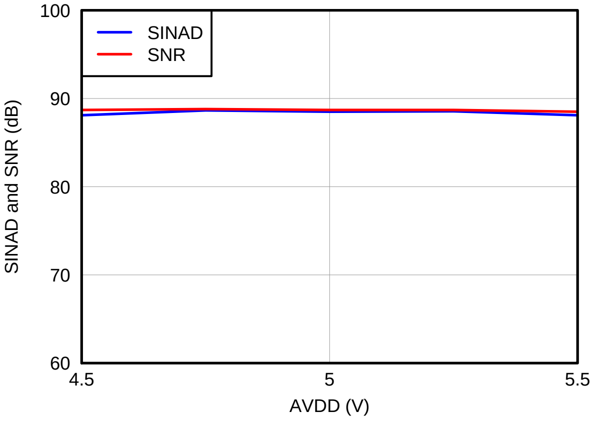


Figure 14.

SINAD AND SNR vs TEMPERATURE

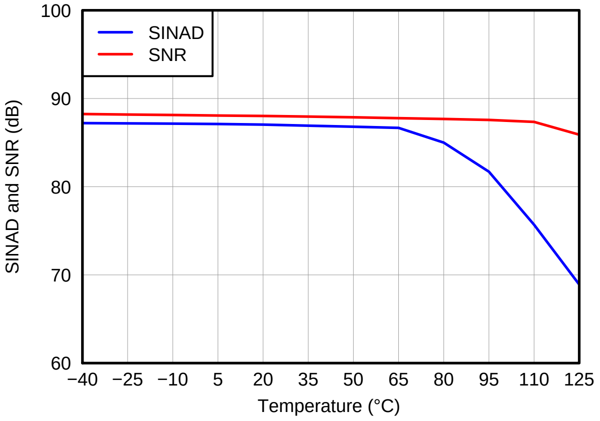


Figure 15.

SINAD AND SNR vs INPUT SIGNAL FREQUENCY

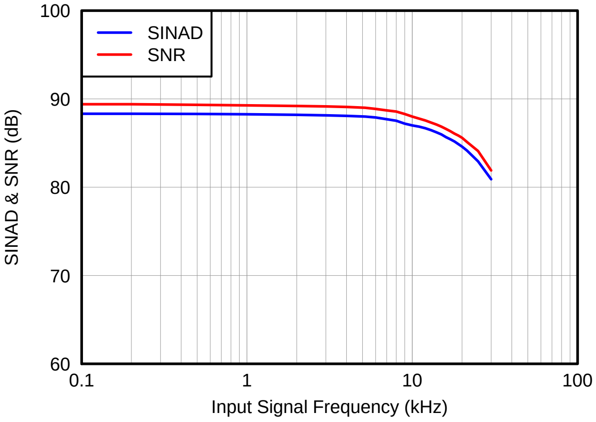


Figure 16.

SINAD AND SNR vs INPUT SIGNAL AMPLITUDE

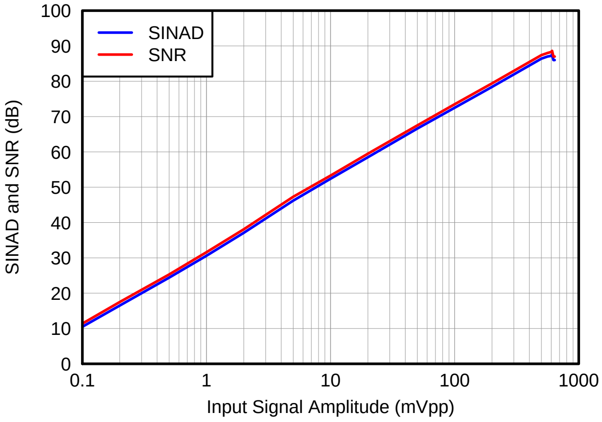


Figure 17.

SINAD AND SNR vs CLOCK FREQUENCY

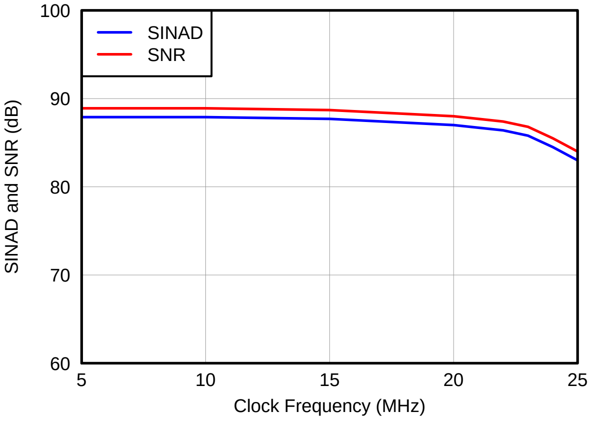


Figure 18.

SINAD AND SNR vs CLOCK DUTY CYCLE

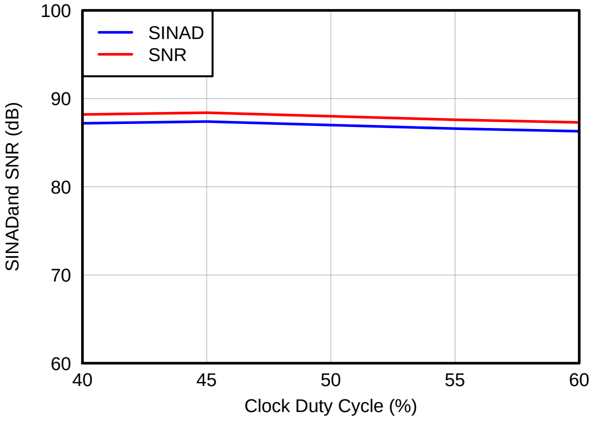


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, DVDD = 3.3V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

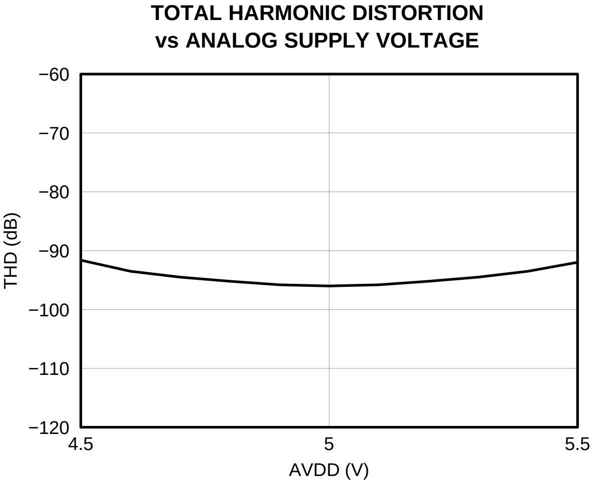


Figure 20.

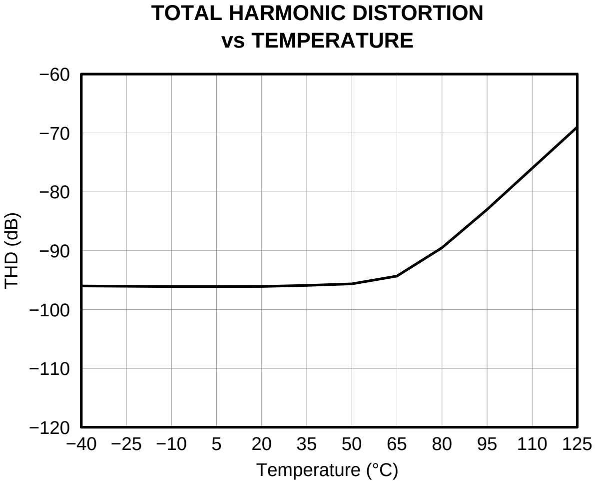


Figure 21.

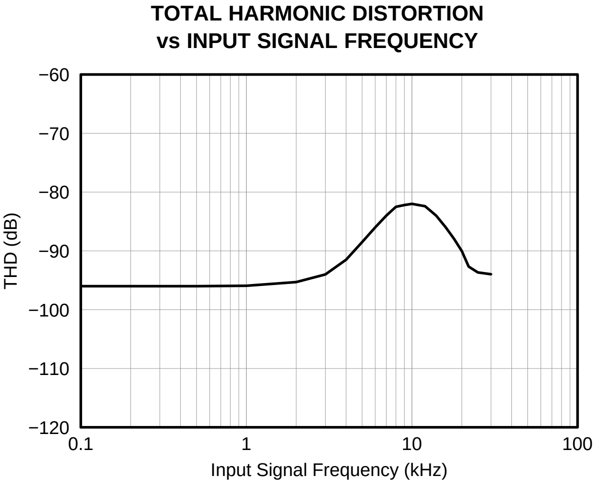
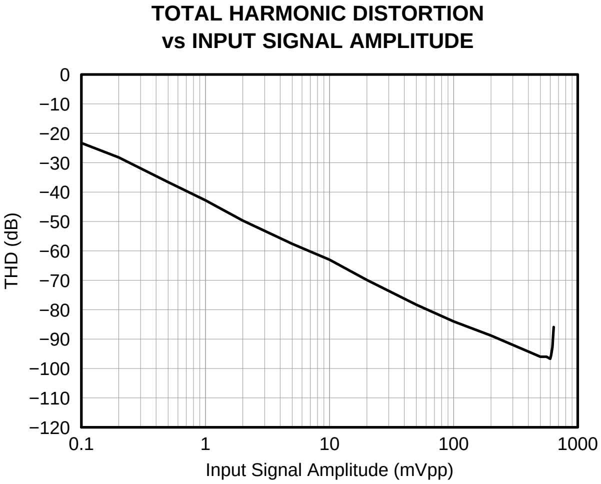


Figure 22.



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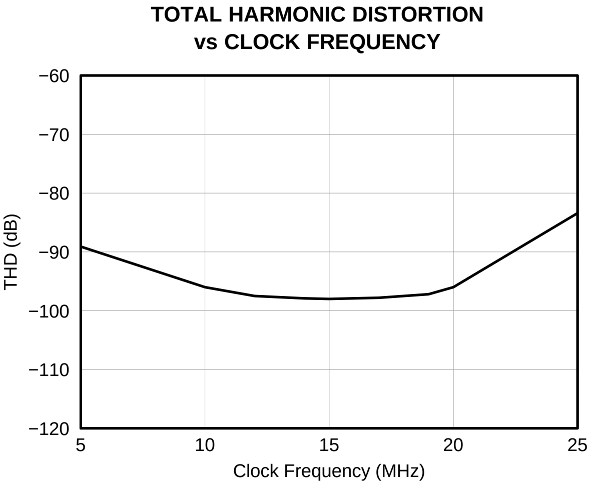

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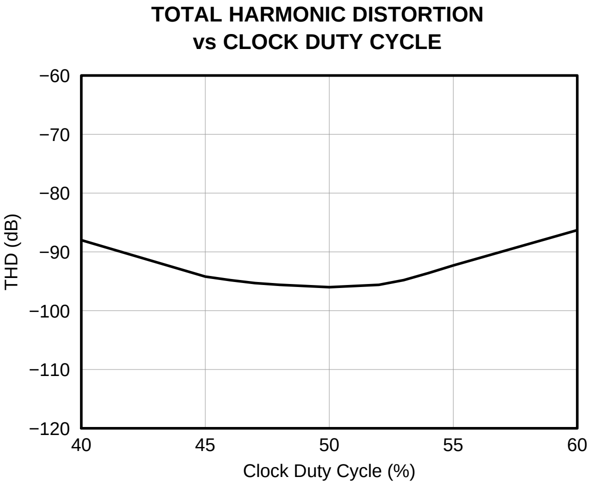


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, DVDD = 3.3V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE vs ANALOG SUPPLY VOLTAGE

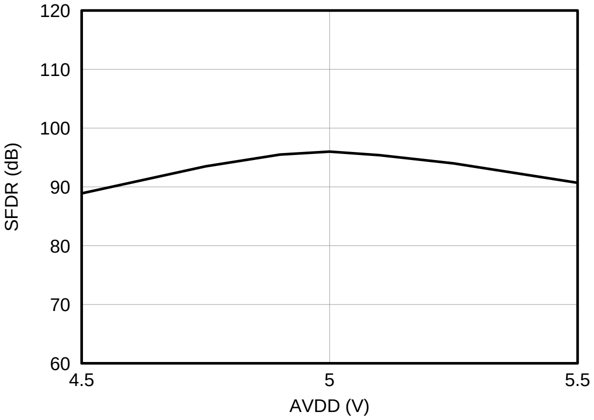


Figure 26.

SPURIOUS-FREE DYNAMIC RANGE vs TEMPERATURE

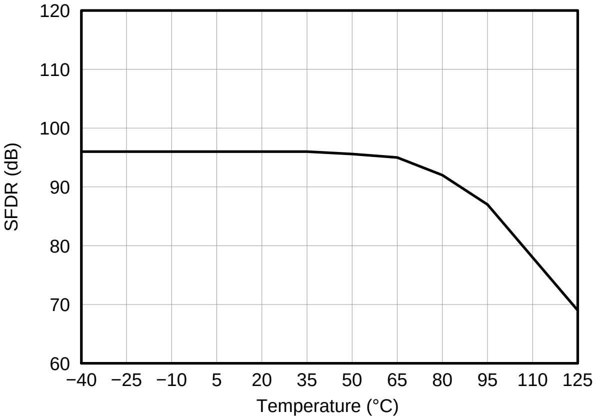


Figure 27.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT SUGNAL FREQUENCY

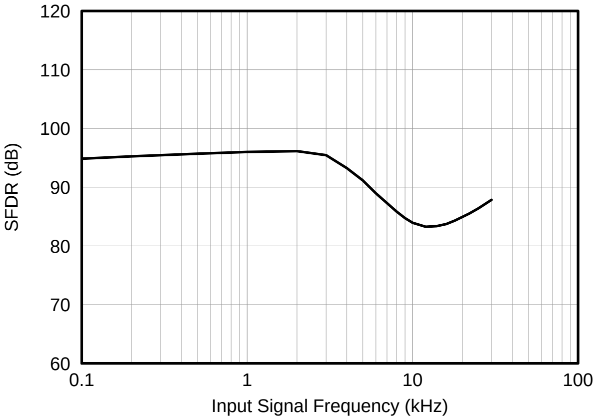


Figure 28.

SPURIOUS-FREE DYNAMIC RANGE vs INPUT SIGNAL AMPLITUDE

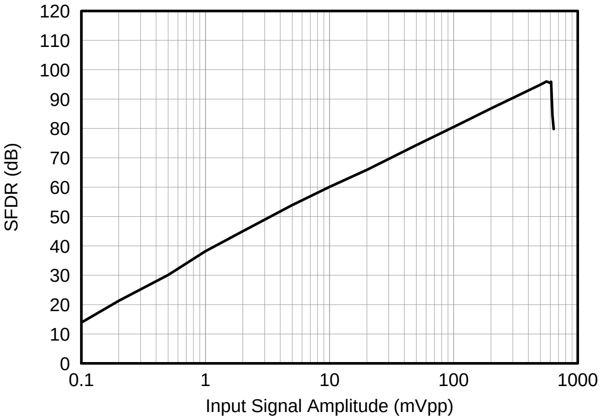


Figure 29.

SPURIOUS-FREE DYNAMIC RANGE vs CLOCK FREQUENCY

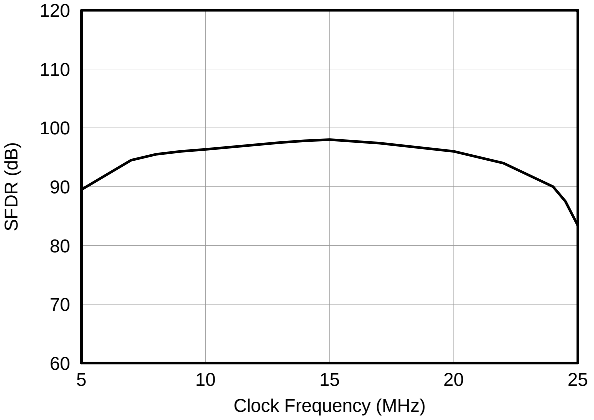


Figure 30.

SPURIOUS-FREE DYNAMIC RANGE vs CLOCK DUTY CYCLE

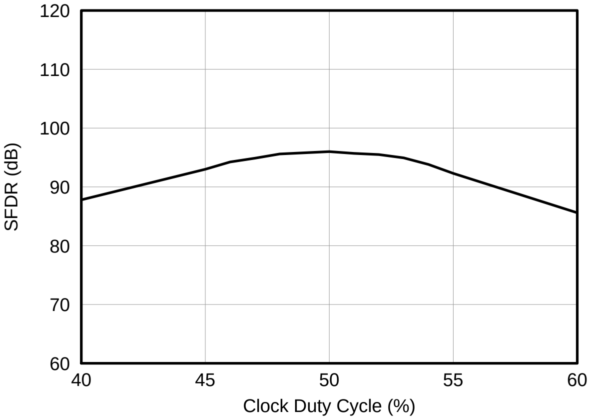


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, DVDD = 3.3V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

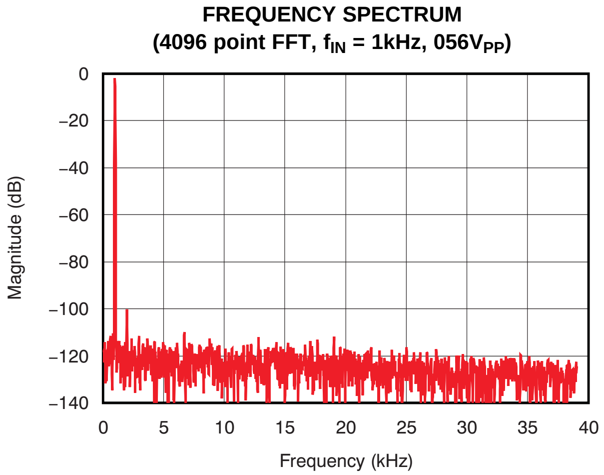


Figure 32.

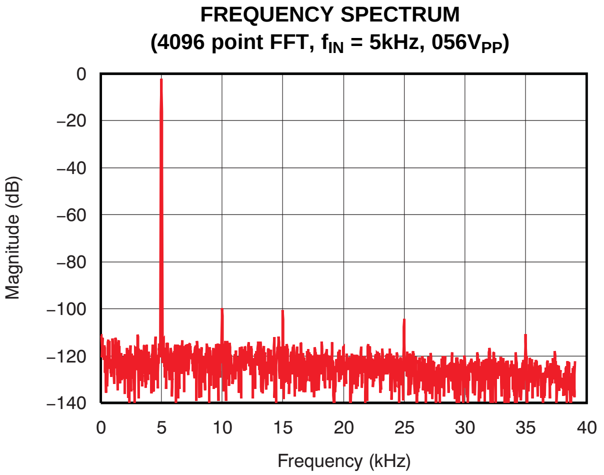


Figure 33.

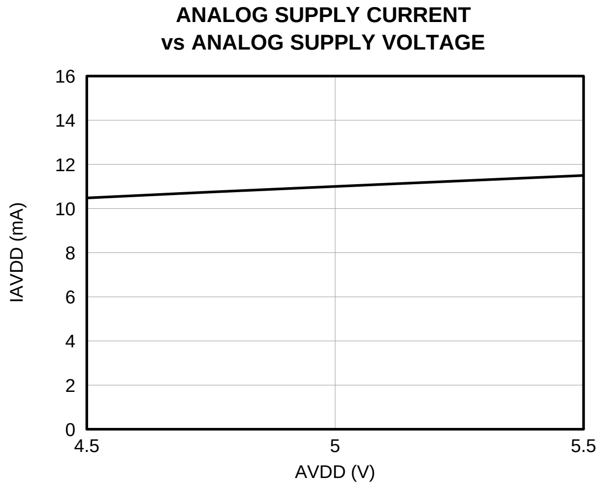


Figure 34.

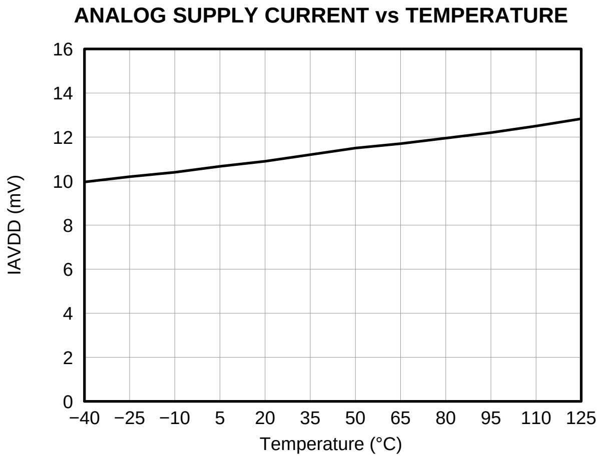


Figure 35.

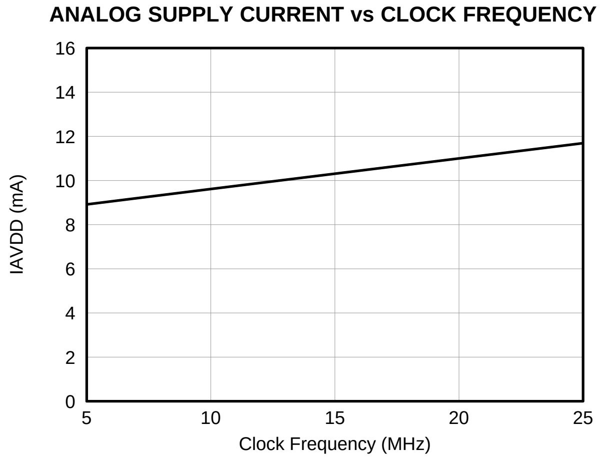


Figure 36.

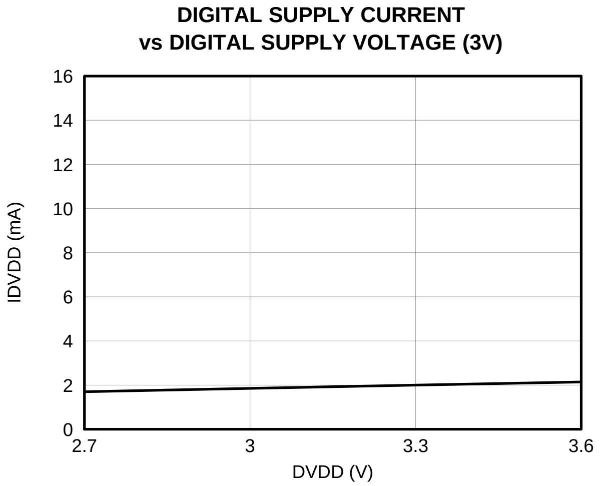


Figure 37.

TYPICAL CHARACTERISTICS (continued)

At AVDD = 5V, DVDD = 3.3V, VINP = –250mV to +250mV, VINN = 0V, and sinc^3 filter with OSR = 256, unless otherwise noted.

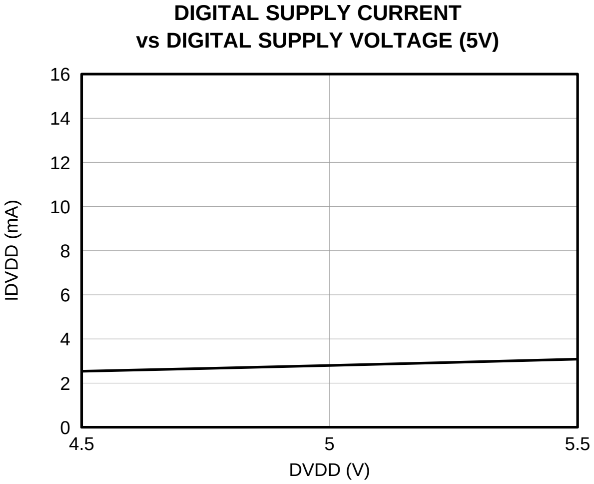


Figure 38.

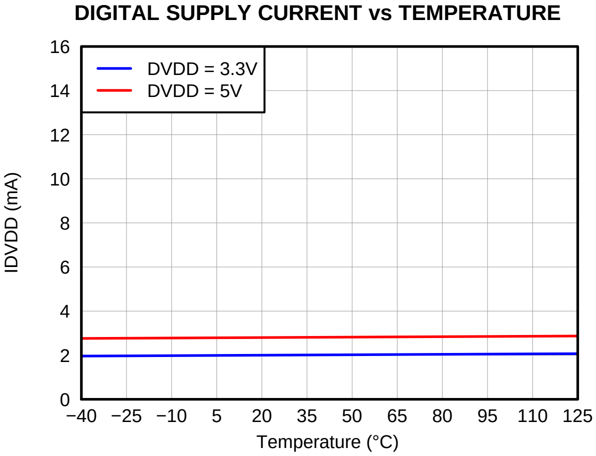


Figure 39.

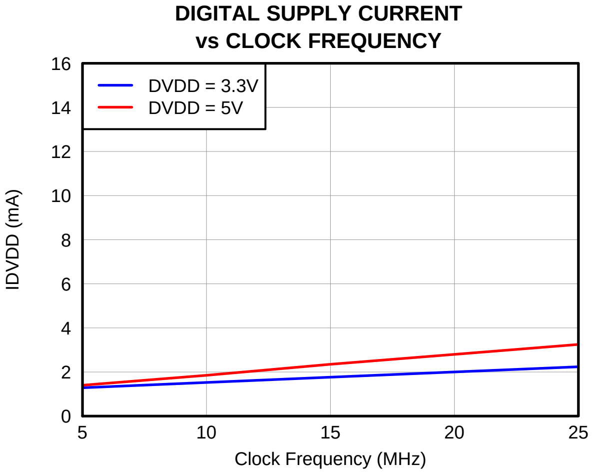


Figure 40.

GENERAL DESCRIPTION

The AMC1204 is a single-channel, second-order, delta-sigma (ΔΣ) modulator designed for medium- to high-resolution analog-to-digital conversions. The isolated output of the converter (DATA) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

Figure 41 shows a detailed block diagram of the AMC1204. The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. The SiO_2-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the application report *ISO72x Digital Isolator Magnetic-Field Immunity* (SLLA181A, available for download at www.ti.com). The external clock input simplifies the synchronization of multiple current sense channels on system level. The extended frequency range of up to 20MHz supports higher performance levels compared to the other solutions available on the market.

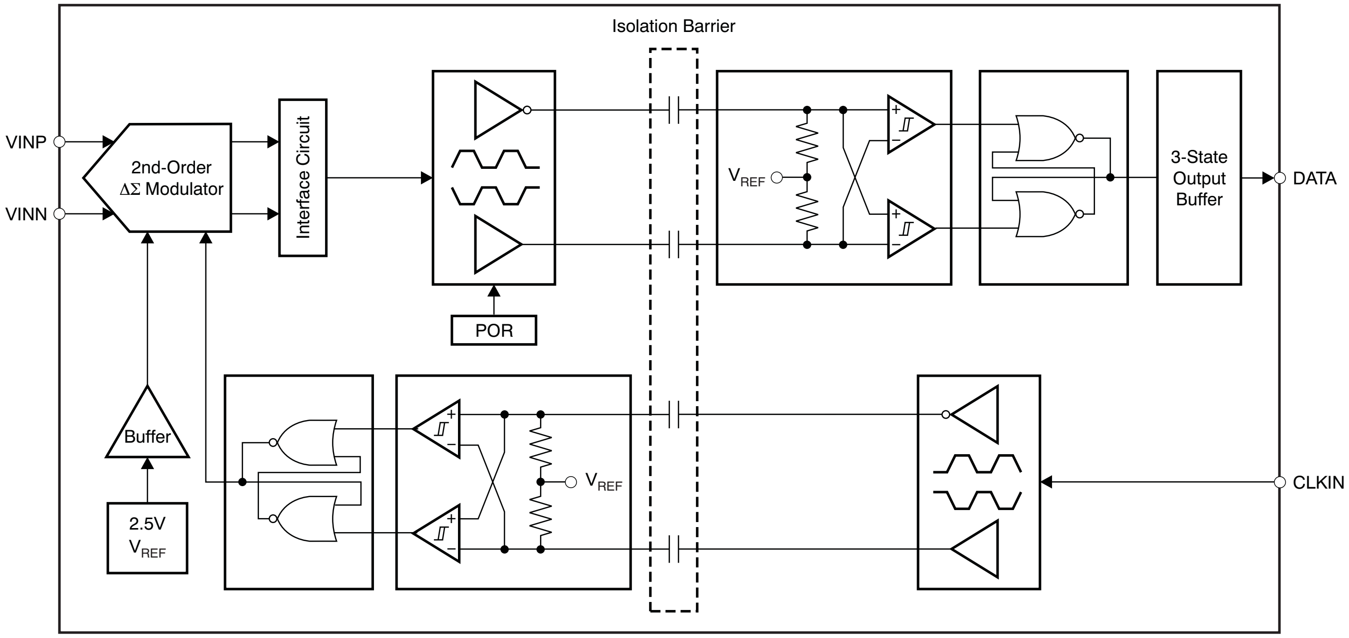


Figure 41. Detailed Block Diagram

THEORY OF OPERATION

The differential analog input of the AMC1204 is implemented with a switched-capacitor circuit. This switched-capacitor circuit implements a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The externally-provided clock source at the CLKIN pin is used by the capacitor circuit and the modulator and should be in the range of 5MHz to 22MHz. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream, accurately representing the analog input voltage over time, appears at the output of the converter at the DATA pin.

ANALOG INPUT

The AMC1204 measures the differential input signal V_{IN} = (VINP – VINN) against the internal reference of 2.5V using internal capacitors that are continuously charged and discharged. Figure 42 shows the simplified schematic of the ADC input circuitry; the right side of Figure 42 illustrates the input circuitry with the capacitors and switches replaced by an equivalent circuit.

In Figure 42, the S_1 switches close during the input sampling phase. With the S_1 switches closed, C_{DIFF} charges to the voltage difference across VINP and VINN. For the discharge phase, both S_1 switches open first and then both S_2 switches close. C_{DIFF} discharges approximately to AGND + 0.8V during this phase. This two-phase sample/discharge cycle repeats with a period of $t_{CLKIN} = 1/f_{CLKIN}$. f_{CLKIN} is the operating frequency of the modulator. The capacitors C_{IP} and C_{IN} are of parasitic nature and caused by bonding wires and the internal ESD protection structure.

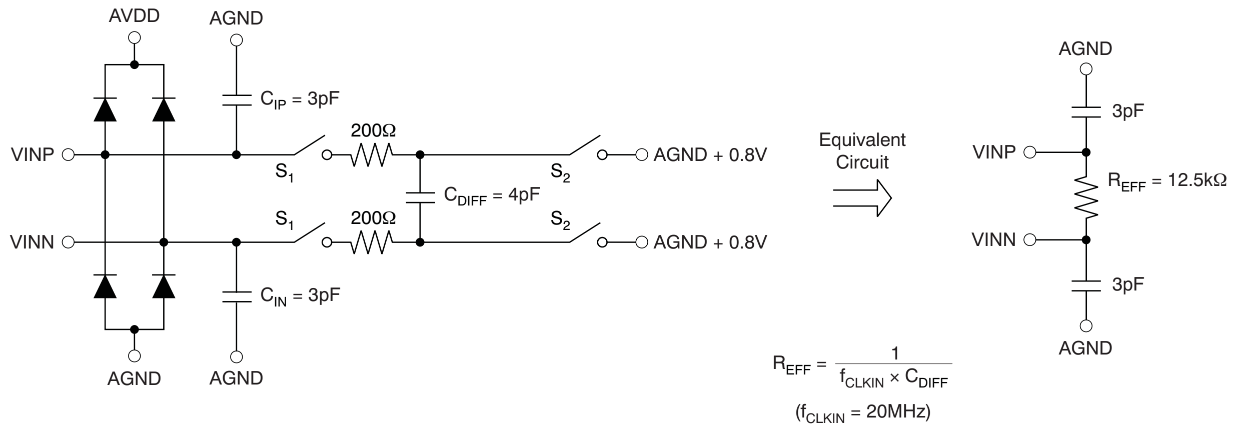


Figure 42. Equivalent Analog Input Circuit

The input impedance becomes a consideration in designs with high input signal source impedance. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect, however, depends on the desired system performance. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (105dB), and excellent power-supply rejection.

There are two restrictions on the analog input signals VINP and VINN. First, if the input voltage exceeds the range AGND – 0.5V to AVDD + 0.3V, the input current must be limited to 10mA because the input protection diodes on the front end of the converter begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250mV.

MODULATOR

The modulator topology of the AMC1204 is fundamentally a second-order, switched-capacitor, ΔΣ modulator, such as the one conceptualized in Figure 43. The analog input voltage ($X_{(t)}$) and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage (X_2) at the input of the first integrator or modulator stage. The output of the first integrator is further differentiated with the DAC output; the resulting voltage (X_3) feeds the input of the second integrator stage. When the value of the integrated signal (X_4) at the output of the second stage equals the comparator reference voltage, the output of the comparator switches from high to low, or vice versa, depending on its previous state. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage (X_6), causing the integrators to progress in the opposite direction, while forcing the value of the integrator output to track the average of the input.

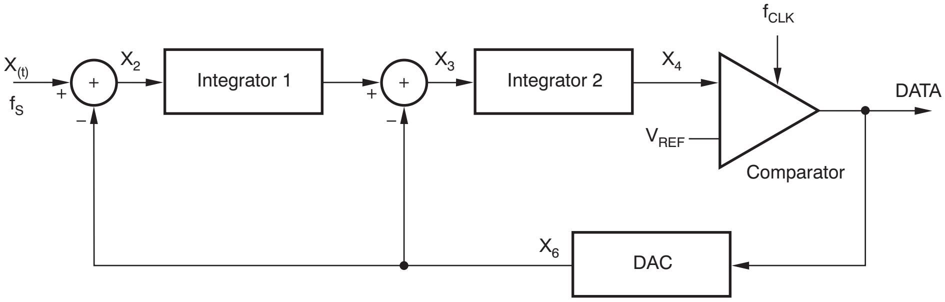


Figure 43. Block Diagram of a Second-Order Modulator

The modulator shifts the quantization noise to high frequencies, as shown in Figure 44; therefore, a low-pass digital filter should be used at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (µC), or field programmable gate array (FPGA) can be used to implement the filter. Another option is to use a suitable application-specific device such as the AMC1210, a four-channel digital sinc-filter.

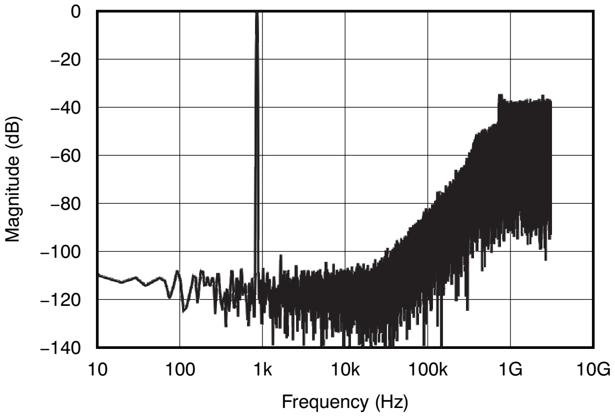


Figure 44. Quantization Noise Shaping

DIGITAL OUTPUT

A differential input signal of 0V ideally produces a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of +250mV produces a stream of ones and zeros that are high 78.1% of the time. A differential input of –250mV produces a stream of ones and zeros that are high 21.9% of the time. This is also the specified linear input range of the modulator with the performance as specified in this data sheet. The range between 250mV and 320mV (absolute values) is the non-linear range of the modulator. The output of the modulator clipps with a stream of only zeros with an input less than or equal to –320mV or with a stream of only ones with an input greater than or equal to 320mV. The input voltage versus the output modulator signal is shown in Figure 45.

The system clock of the AMC1204 is typically 20MHz and is provided externally at the CLKIN pin. The data are synchronously provided at 20MHz at the DATA output pin. The data are changing at the falling edge of CLKIN; for more details see the Timing Information section.

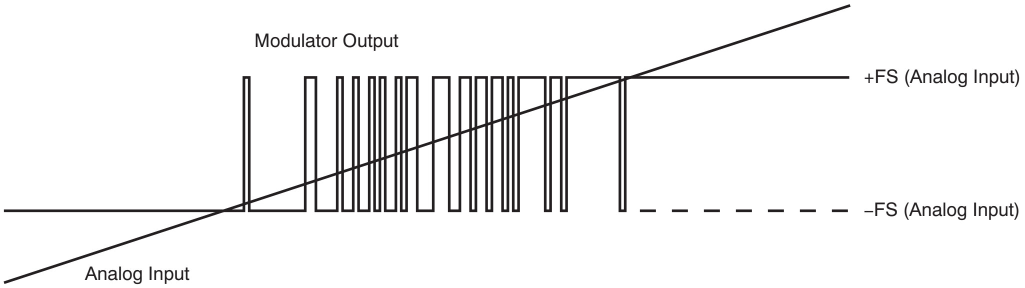


Figure 45. Analog Input versus AMC1204 Modulator Output

FILTER USAGE

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc^3-type filter, as shown in Equation 1:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3 \quad (1)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates). For an oversampling rate (OSR) in the range of 16 to 256, this filter is a good choice. All the characterization in this document is also done with a sinc^3 filter with OSR = 256 and an output word width of 16 bits.

In a sinc^3 filter response (shown in Figure 46 and Figure 47), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3dB point is located at half the Nyquist frequency or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type with different frequency response. Performance can be improved, for example, by using a cascaded filter structure. The first decimation stage could be built of a sinc^3 filter with a low OSR and the second stage using a high-order filter.

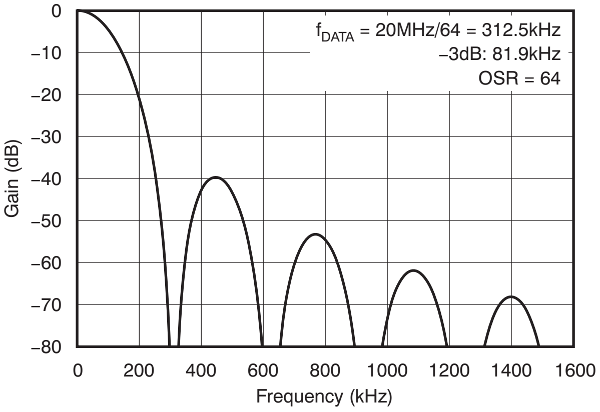


Figure 46. Frequency Response of the Sinc^3 Filter

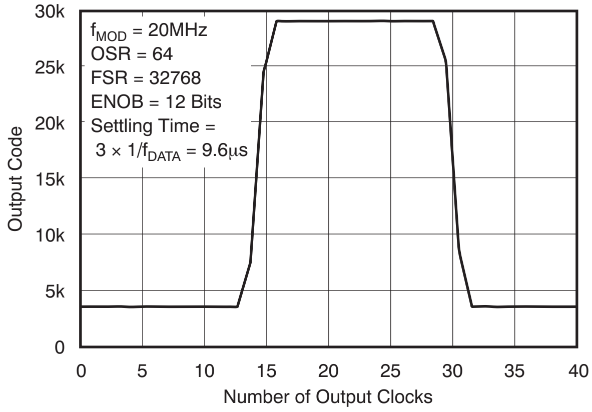


Figure 47. Pole Response of the Sinc^3 Filter

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 48 illustrates the ENOB of the AMC1204 with different oversampling ratios. In this data sheet, this number is calculated from SNR using Equation 2:

$$\text{SNR} = 1.76\text{dB} + 6.02\text{dB} \times \text{ENOB} \quad (2)$$

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter depends on its order; that is, a sinc^3 filter requires three data clocks for full settling (with $f_{DATA} = f_{CLK}/OSR$). Therefore, for overcurrent protection, filter types other than sinc^3 might be a better choice; an alternative is the sinc^2 filter. Figure 49 compares the settling times of different filter orders with sincfast being a modified sinc^2 filter with behavior as shown in Equation 3.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 (1 + z^{-2OSR}) \quad (3)$$

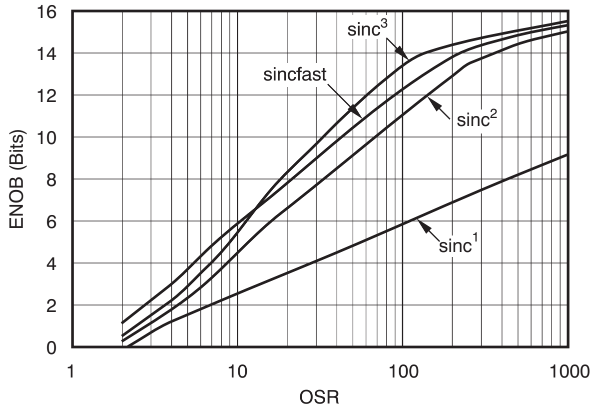


Figure 48. Measured Effective Number of Bits versus Oversampling Ratio

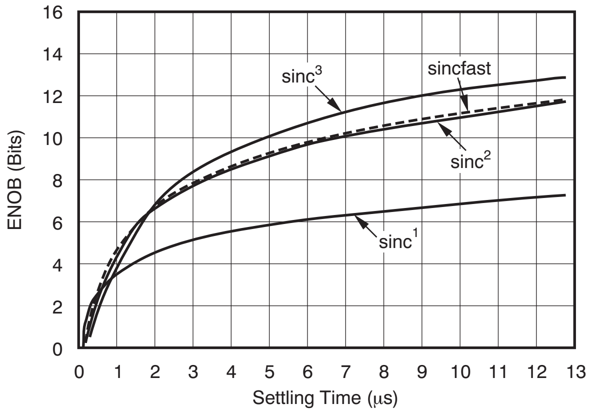


Figure 49. Measured Effective Number of Bits versus Settling Time

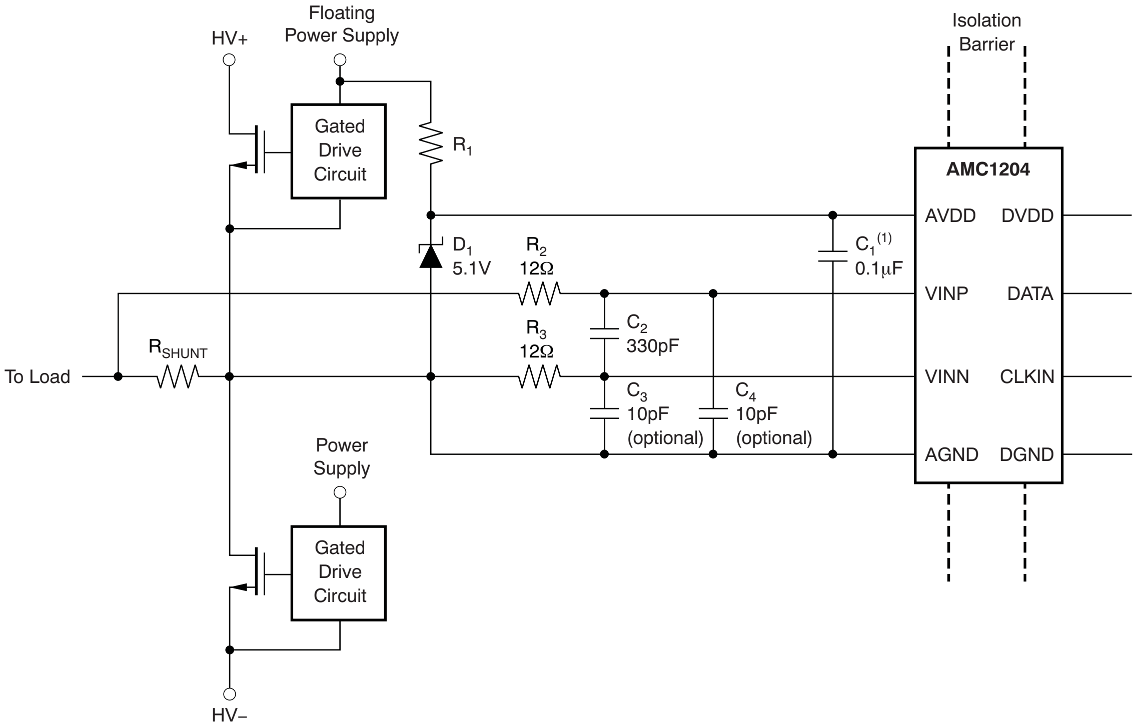
An example code for an implementation of a sinc^3 filter in an FPGA follows. For more information, see the application note *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications (SBAA094)*, available for download at www.ti.com.

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity FLT is
  port(RESN, MOUT, MCLK, CNR : in std_logic;
       CN5 : out std_logic_vector(23 downto 0));
end FLT;

architecture RTL of FLT is
  signal DN0, DN1, DN3, DN5 : std_logic_vector(23 downto 0);
  signal CN1, CN2, CN3, CN4 : std_logic_vector(23 downto 0);
  signal DELTA1 : std_logic_vector(23 downto 0);
begin

process(MCLK, RESn)
  begin
    if RESn = '0' then
      DELTA1 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      if MOUT = '1' then
        DELTA1 <= DELTA1 + 1;
      end if;
    end if;
  end process;

process(RESN, MCLK)
  begin
    if RESN = '0' then
      CN1 <= (others => '0');
      CN2 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      CN1 <= CN1 + DELTA1;
      CN2 <= CN2 + CN1;
    end if;
  end process;

process(RESN, CNR)
  begin
    if RESN = '0' then
      DN0 <= (others => '0');
      DN1 <= (others => '0');
      DN3 <= (others => '0');
      DN5 <= (others => '0');
    elsif CNR'event and CNR = '1' then
      DN0 <= CN2;
      DN1 <= DN0;
      DN3 <= CN3;
      DN5 <= CN4;
    end if;
  end process;

CN3 <= DN0 - DN1;
CN4 <= CN3 - DN3;
CN5 <= CN4 - DN5;

end RTL;
```

APPLICATION INFORMATION

A typical operation of the AMC1204 in a motor control application is shown in Figure 50. Measurement of the motor phase current is done via the shunt resistor R_{SHUNT} (in this case, a two-terminal shunt). For better performance, the differential signal is filtered using RC filters (components R_2, R_3, and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, care should be taken when choosing the quality of these capacitors—mismatch in values of these capacitors leads to a common-mode error at the input of the modulator.

The high-side power supply for the AMC1204 (AVDD) is derived from the power supply of the upper gate driver. For lowest cost, a zener diode can be used to limit the voltage to 5V ±10%. A decoupling capacitor of 0.1μF is recommended for filtering this power-supply path. This capacitor (C_1 in Figure 50) should be placed as close as possible to the AVDD pin for best performance. If better filtering is required, an additional 1μF to 10μF capacitor can be used. The floating ground reference AGND is derived from the end of the shunt resistor, which is connected to the negative input of the AMC1204 (VINN). If a four-terminal shunt is used, the inputs of AMC1204 are connected to the inner leads, while AGND is connected to one of the outer leads of the shunt. Both digital signals, CLKIN and DATA, can be directly connected to a digital filter (for example, the AMC1210); see Figure 51.



(1) Place C_1 close to the AMC1204.

Figure 50. Typical Application Diagram

Figure 51 shows an example of two AMC1204s and one ADS1209 (a dual-channel, 10MHz, non-isolated modulator) connected to an AMC1210, building the entire analog front-end of a resolver-based motor control application.

For detailed information on the ADS1209 and AMC1210, visit the respective device product folders at www.ti.com.

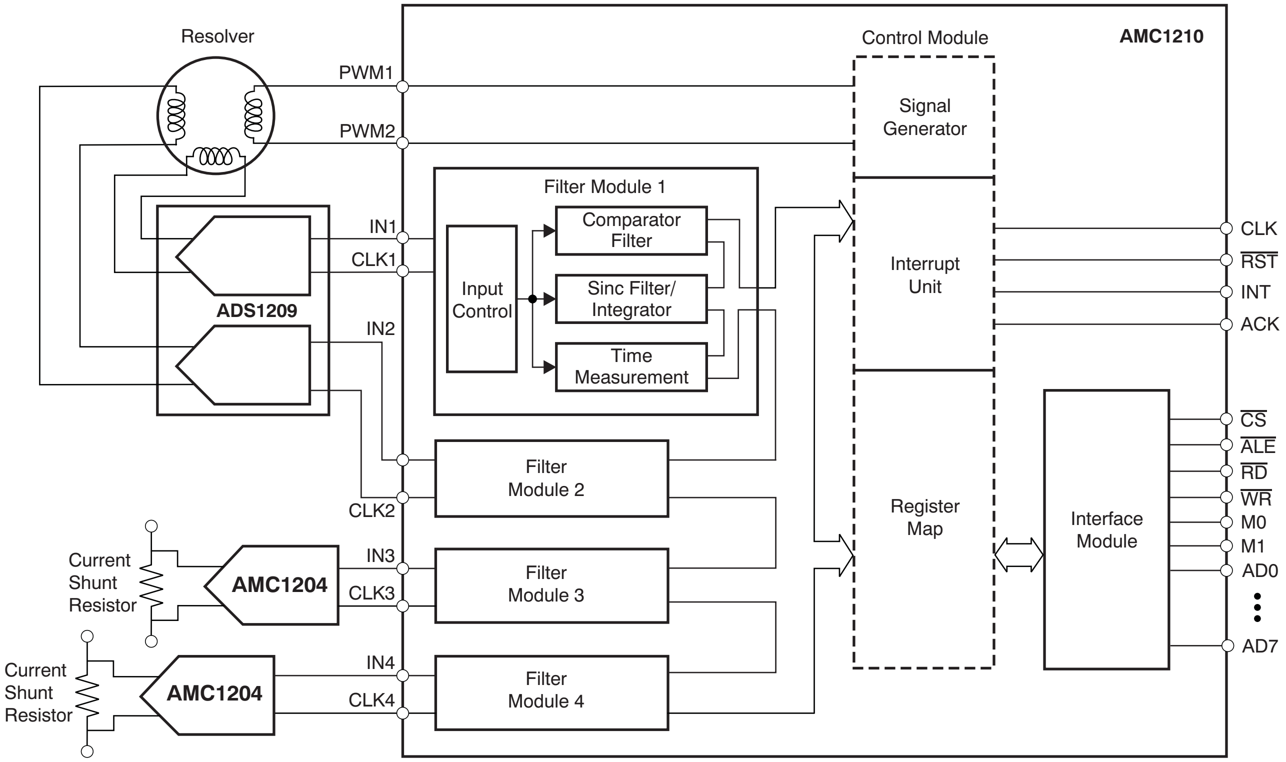


Figure 51. Example of a Resolver-Based Motor Control Analog Front-End

A layout recommendation showing the critical placement of the decoupling capacitor on the high-side and placement of the other components required by the AMC1204 is presented in Figure 52.

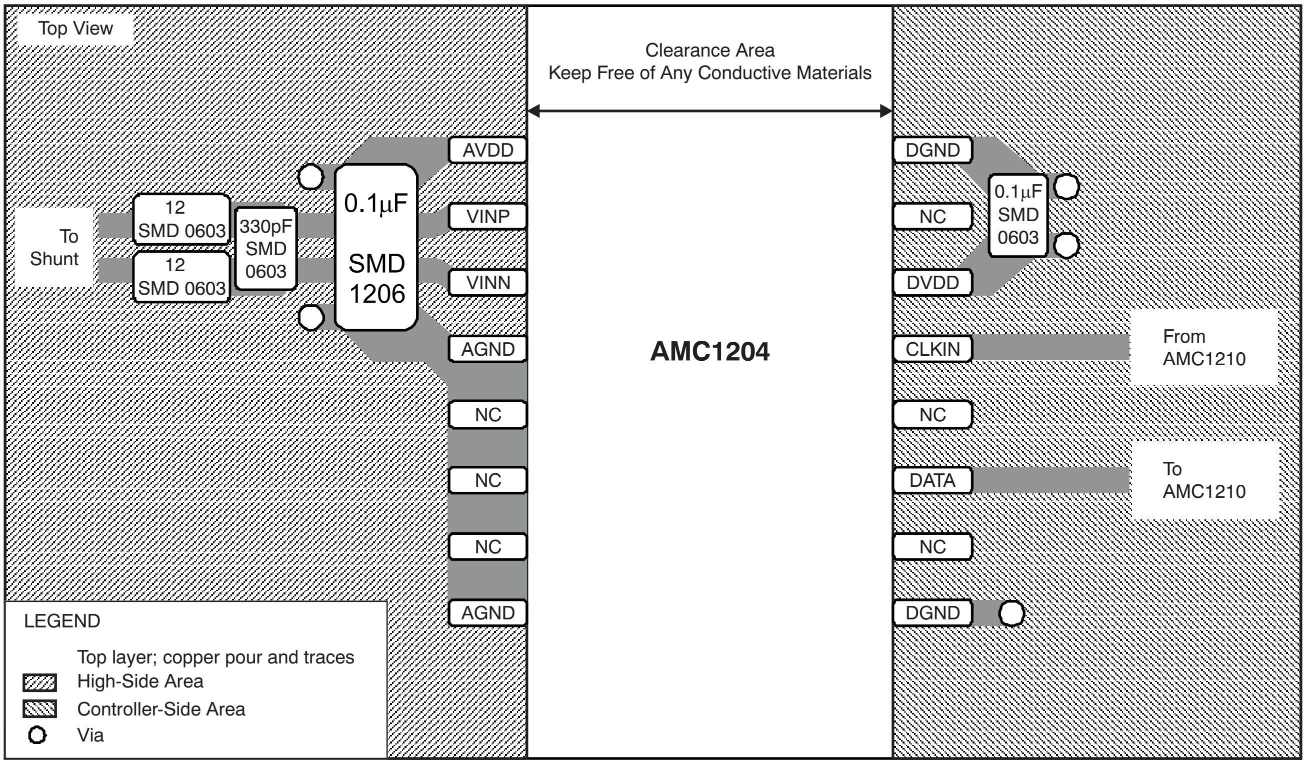
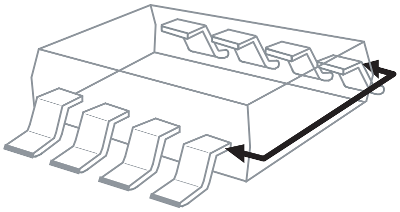


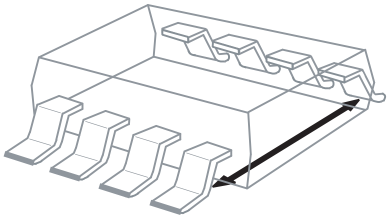
Figure 52. Recommended Layout

ISOLATION GLOSSARY

Creepage Distance: The shortest path between two conductive input to output leads measured along the surface of the insulation. The shortest distance path is found around the end of the package body.



Clearance: The shortest distance between two conductive input to output leads measured through air (line of sight).



Input-to-Output Barrier Capacitance: The total capacitance between all input terminals connected together, and all output terminals connected together.

Input-to-Output Barrier Resistance: The total resistance between all input terminals connected together, and all output terminals connected together.

Primary Circuit: An internal circuit directly connected to an external supply mains or other equivalent source that supplies the primary circuit electric power.

Secondary Circuit: A circuit with no direct connection to primary power that derives its power from a separate isolated source.

Comparative Tracking Index (CTI): CTI is an index used for electrical insulating materials. It is defined as the numerical value of the voltage that causes failure by tracking during standard testing. Tracking is the process that produces a partially conducting path of localized deterioration on or through the surface of an insulating material as a result of the action of electric discharges on or close to an insulation surface. The higher CTI value of the insulating material, the smaller the minimum creepage distance.

Generally, insulation breakdown occurs either through the material, over its surface, or both. Surface failure may arise from flashover or from the progressive degradation of the insulation surface by small localized sparks. Such sparks are the result of the breaking of a surface film of conducting contaminant on the insulation. The resulting break in the leakage current produces an overvoltage at the site of the discontinuity, and an electric spark is generated. These sparks often cause carbonization on insulation material and lead to a carbon track between points of different potential. This process is known as tracking.

Insulation:

Operational insulation—Insulation needed for the correct operation of the equipment.

Basic insulation—Insulation to provide basic protection against electric shock.

Supplementary insulation—Independent insulation applied in addition to basic insulation in order to ensure protection against electric shock in the event of a failure of the basic insulation.

Double insulation—Insulation comprising both basic and supplementary insulation.

Reinforced insulation—A single insulation system that provides a degree of protection against electric shock equivalent to double insulation.

Pollution Degree:

Pollution Degree 1—No pollution, or only dry, nonconductive pollution occurs. The pollution has no influence on device performance.

Pollution Degree 2—Normally, only nonconductive pollution occurs. However, a temporary conductivity caused by condensation is to be expected.

Pollution Degree 3—Conductive pollution, or dry nonconductive pollution that becomes conductive because of condensation, occurs. Condensation is to be expected.

Pollution Degree 4—Continuous conductivity occurs as a result of conductive dust, rain, or other wet conditions.

Installation Category:

Overvoltage Category—This section is directed at insulation coordination by identifying the transient overvoltages that may occur, and by assigning four different levels as indicated in IEC 60664.

1. Signal Level: Special equipment or parts of equipment.
2. Local Level: Portable equipment, etc.
3. Distribution Level: Fixed installation.
4. Primary Supply Level: Overhead lines, cable systems.

Each category should be subject to smaller transients than the previous category.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April 2011) to Revision B	Page
• Changed value of V_{IOSM} parameter in IEC 61000-4-5 Ratings table	3

Changes from Original (April 2011) to Revision A	Page
• Changed *Analog input voltage at VINP, VINN* parameter maximum specification in Absolute Maximum Ratings table	2
• Changed *Safety input, output, or supply current* parameter maximum specification in IEC Safety Limiting Values table	3
• Updated Figure 3	8
• Updated Figure 22	11
• Updated Figure 28	12

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
AMC1204DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
AMC1204DWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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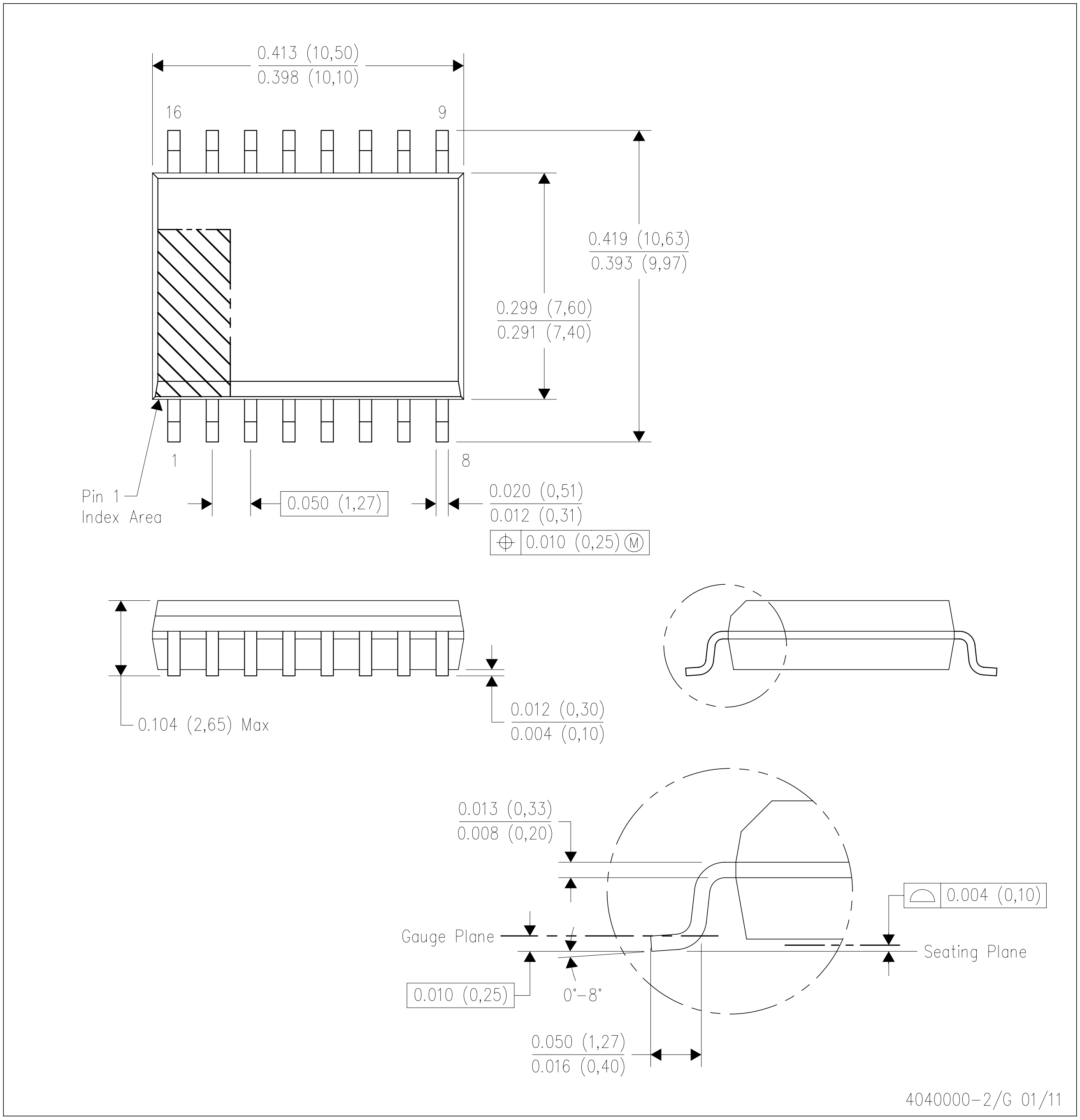
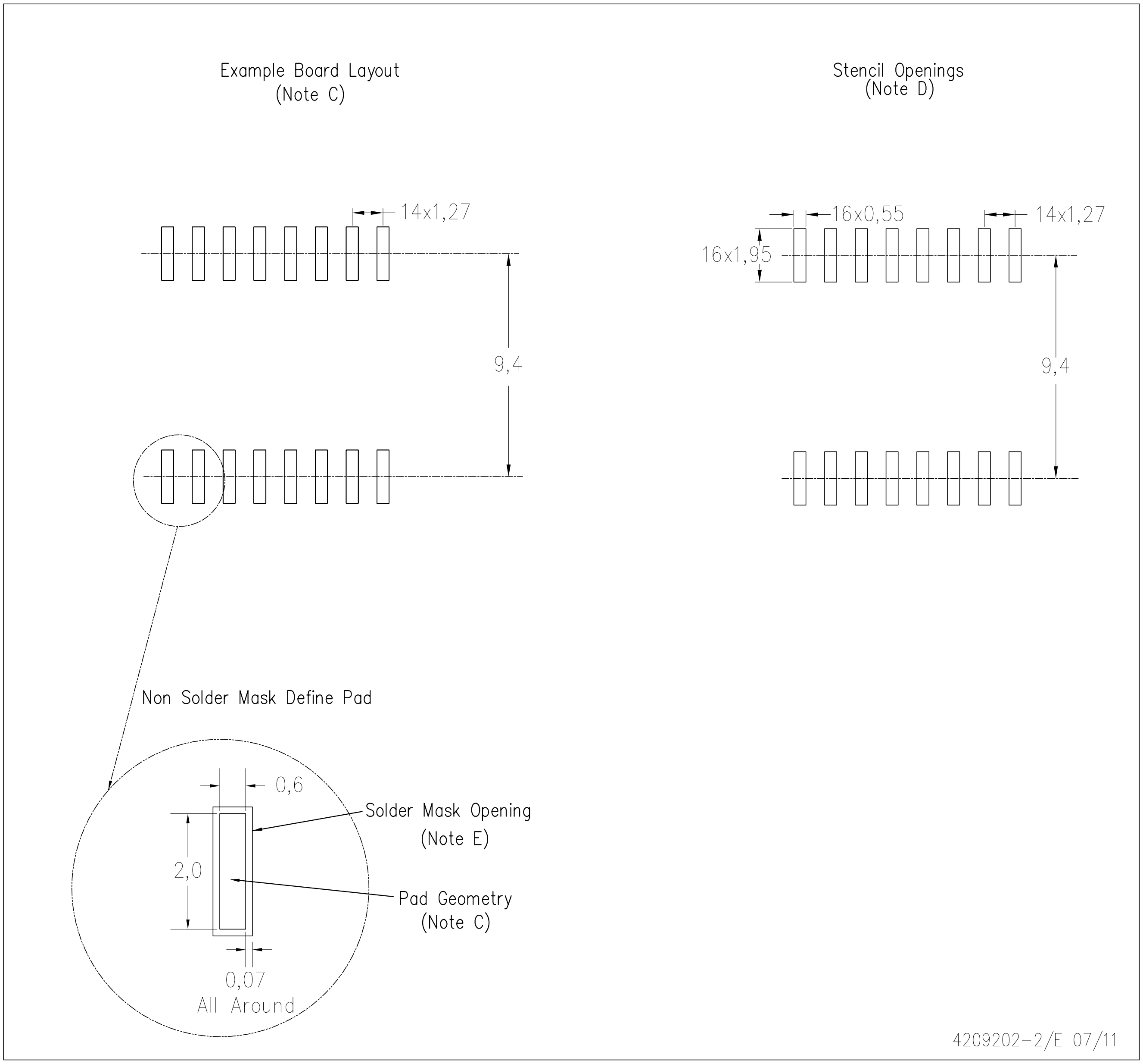
DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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