



# 16-Bit, High-Speed, 2.7V to 5V *micro*Power Sampling ANALOG-TO-DIGITAL CONVERTER

## FEATURES

- 100kHz SAMPLING RATE
- *micro*POWER:
  - 1.8mW at 100kHz and 2.7V
  - 0.3mW at 10kHz and 2.7V
- POWER-DOWN: 3μA max
- MSOP-8 PACKAGE
- PIN-COMPATIBLE TO ADS7816 AND ADS7822
- SERIAL (SPI™/SSI) INTERFACE

## APPLICATIONS

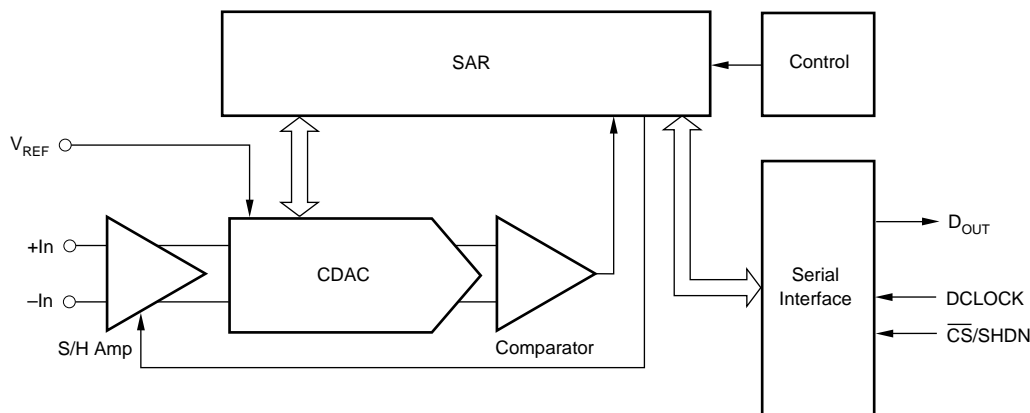
- BATTERY-OPERATED SYSTEMS
- REMOTE DATA ACQUISITION
- ISOLATED DATA ACQUISITION
- SIMULTANEOUS SAMPLING,  
MULTICHANNEL SYSTEMS
- INDUSTRIAL CONTROLS
- ROBOTICS
- VIBRATION ANALYSIS

## DESCRIPTION

The ADS8320 is a 16-bit, sampling analog-to-digital (A/D) converter with ensured specifications over a 2.7V to 5.25V supply range. It requires very little power even when operating at the full 100kHz data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode—the average power dissipation is less than 100μW at 10kHz data rate.

The ADS8320 also features operation from 2.0V to 5.25V, a synchronous serial (SPI/SSI compatible) interface, and a differential input. The reference voltage can be set to any level within the range of 500mV to  $V_{CC}$ .

Ultra-low power and small size make the ADS8320 ideal for portable and battery-operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multi-channel systems, and isolated data acquisition. The ADS8320 is available in an MSOP-8 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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# SPECIFICATIONS: +V<sub>CC</sub> = +5V

At -40°C to +85°C, V<sub>REF</sub> = +5V, -IN = GND, f<sub>SAMPLE</sub> = 100kHz, and f<sub>CLK</sub> = 24 • f<sub>SAMPLE</sub>, unless otherwise specified.

PARAMETER	CONDITIONS	ADS8320E			ADS8320EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>RESOLUTION</b>				16			*	Bits
<b>ANALOG INPUT</b>								
Full-Scale Input Span	+In – (-In)	0		V <sub>REF</sub>	*		*	V
Absolute Input Range	+In	-0.1		V <sub>CC</sub> + 0.1	*		*	V
	-In	-0.1		+1.0	*		*	V
Capacitance			45			*		pF
Leakage Current			1			*		nA
<b>SYSTEM PERFORMANCE</b>								
No Missing Codes		14			15			Bits
Integral Linearity Error			±0.008	±0.018		±0.006	±0.012	% of FSR
Offset Error			±1	±2		±0.5	±1	mV
Offset Temperature Drift			±3			*		µV/°C
Gain Error				±0.05			±0.024	%
Gain Temperature Drift			±0.3			*		ppm/°C
Noise			20			*		µVrms
Power-Supply Rejection Ratio	+4.7V < V <sub>CC</sub> < 5.25V		3			*		LSB <sup>(1)</sup>
<b>SAMPLING DYNAMICS</b>								
Conversion Time				16			*	Clk Cycles
Acquisition Time		4.5			*			Clk Cycles
Throughput Rate				100			*	kHz
Clock Frequency Range		0.024		2.4	*		*	MHz
<b>DYNAMIC CHARACTERISTICS</b>								
Total Harmonic Distortion	V <sub>IN</sub> = 5V <sub>PP</sub> at 10kHz		-84			-86		dB
SINAD	V <sub>IN</sub> = 5V <sub>PP</sub> at 10kHz		82			84		dB
Spurious-Free Dynamic Range	V <sub>IN</sub> = 5V <sub>PP</sub> at 10kHz		84			86		dB
SNR			90			92		dB
<b>REFERENCE INPUT</b>								
Voltage Range		0.5		V <sub>CC</sub>	*		*	V
Resistance	$\overline{CS} = \text{GND}$ , f <sub>SAMPLE</sub> = 0Hz $\overline{CS} = V_{CC}$		5			*		GΩ
			5			*		GΩ
Current Drain	f <sub>SAMPLE</sub> = 10kHz $\overline{CS} = V_{CC}$		40	80		*	*	µA
			0.8			*		µA
			0.1	3		*		µA
<b>DIGITAL INPUT/OUTPUT</b>								
Logic Family			CMOS			*		
Logic Levels:								
V <sub>IH</sub>	I <sub>IH</sub> = +5µA	3.0		V <sub>CC</sub> + 0.3	*		*	V
V <sub>IL</sub>	I <sub>IL</sub> = +5µA	-0.3		0.8	*		*	V
V <sub>OH</sub>	I <sub>OH</sub> = -250µA	4.0			*		*	V
V <sub>OL</sub>	I <sub>OL</sub> = 250µA			0.4			*	V
Data Format				Straight Binary		*		
<b>POWER-SUPPLY REQUIREMENTS</b>								
V <sub>CC</sub>	Specified Performance	4.75		5.25	*		*	V
V <sub>CC</sub> Range <sup>(2)</sup>		2.0		5.25	*		*	V
Quiescent Current			900	1700		*	*	µA
	f <sub>SAMPLE</sub> = 10kHz <sup>(3, 4)</sup>		200			*	*	µA
Power Dissipation			4.5	8.5		*	*	mW
Power-Down	$\overline{CS} = V_{CC}$		0.3	3		*	*	µA
<b>TEMPERATURE RANGE</b>								
Specified Performance		-40		+85	*		*	°C

\* Specifications same as ADS8320E.

NOTES: (1) LSB means Least Significant Bit. With V<sub>REF</sub> equal to +5.0V, one LSB is 0.076mV.

(2) See *Typical Performance Curves* for more information.

(3) f<sub>CLK</sub> = 2.4MHz,  $\overline{CS} = V_{CC}$  for 216 clock cycles out of every 240.

(4) See the Power Dissipation section for more information regarding lower sample rates.

# SPECIFICATIONS: +V<sub>CC</sub> = +2.7V

At -40°C to +85°C, V<sub>REF</sub> = 2.5V, -IN = GND, f<sub>SAMPLE</sub> = 100kHz, and f<sub>CLK</sub> = 24 • f<sub>SAMPLE</sub>, unless otherwise specified.

PARAMETER	CONDITIONS	ADS8320E			ADS8320EB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>RESOLUTION</b>				16			*	Bits
<b>ANALOG INPUT</b>								
Full-Scale Input Span	+In – (-In)	0		V <sub>REF</sub>	*		*	V
Absolute Input Range	+In	-0.1		V <sub>CC</sub> + 0.1	*		*	V
	-In	-0.1		+0.5	*		*	V
Capacitance			45			*		pF
Leakage Current			1			*		nA
<b>SYSTEM PERFORMANCE</b>								
No Missing Codes		14			15			Bits
Integral Linearity Error			±0.008	±0.018		±0.006	±0.012	% of FSR
Offset Error			±1	±2		±0.5	±1	mV
Offset Temperature Drift			±3			*		μV/°C
Gain Error				±0.05			±0.024	% of FSR
Gain Temperature Drift			±0.3			*		ppm/°C
Noise			20			*		μVrms
Power-Supply Rejection Ratio	+2.7V < V <sub>CC</sub> < +3.3V		3			*		LSB <sup>(1)</sup>
<b>SAMPLING DYNAMICS</b>								
Conversion Time				16			*	Clk Cycles
Acquisition Time		4.5			*			Clk Cycles
Throughput Rate				100			*	kHz
Clock Frequency Range		0.024		2.4	*		*	MHz
<b>DYNAMIC CHARACTERISTICS</b>								
Total Harmonic Distortion	V <sub>IN</sub> = 2.7Vp-p at 1kHz		-86			-88		dB
SINAD	V <sub>IN</sub> = 2.7Vp-p at 1kHz		84			86		dB
Spurious-Free Dynamic Range	V <sub>IN</sub> = 2.7Vp-p at 1kHz		86			88		dB
SNR			88			90		dB
<b>REFERENCE INPUT</b>								
Voltage Range		0.5		V <sub>CC</sub>	*		*	V
Resistance	$\overline{CS} = \text{GND}$ , f <sub>SAMPLE</sub> = 0Hz		5			*		GΩ
	$\overline{CS} = V_{CC}$		5			*		GΩ
Current Drain			20	50		*	*	μA
	$\overline{CS} = V_{CC}$		0.1	3		*	*	μA
<b>DIGITAL INPUT/OUTPUT</b>								
Logic Family			CMOS			*		
Logic Levels:								
V <sub>IH</sub>	I <sub>IH</sub> = +5μA	2.0		V <sub>CC</sub> + 0.3	*		*	V
V <sub>IL</sub>	I <sub>IL</sub> = +5μA	-0.3		0.8	*		*	V
V <sub>OH</sub>	I <sub>OH</sub> = -250μA	2.1			*		*	V
V <sub>OL</sub>	I <sub>OL</sub> = 250μA			0.4			*	V
Data Format				Straight Binary		*		
<b>POWER-SUPPLY REQUIREMENTS</b>								
V <sub>CC</sub>	Specified Performance	2.7		3.3	*		*	V
V <sub>CC</sub> Range <sup>(3)</sup>		2.0		5.25	*		*	V
	See Note 2	2.0		2.7	*		*	V
Quiescent Current			650	1300		*	*	μA
	f <sub>SAMPLE</sub> = 10kHz <sup>(4,5)</sup>		100			*	*	μA
Power Dissipation			1.8	3.8		*	*	mW
Power-Down	$\overline{CS} = V_{CC}$		0.3	3		*	*	μA
<b>TEMPERATURE RANGE</b>								
Specified Performance		-40		+85	*		*	°C

\* Specifications same as ADS8320E.

NOTES: (1) LSB means Least Significant Bit. With V<sub>REF</sub> equal to +2.5V, one LSB is 0.038mV.

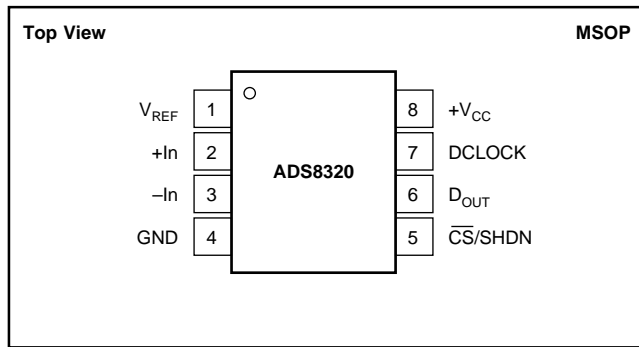
(2) The maximum clock rate of the ADS8320 is less than 2.4MHz in this power supply range.

(3) See the *Typical Performance Curves* for more information.

(4) f<sub>CLK</sub> = 2.4MHz,  $\overline{CS} = V_{CC}$  for 216 clock cycles out of every 240.

(5) See the Power Dissipation section for more information regarding lower sample rates.

## PIN CONFIGURATION



## ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Texas Instruments recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

## PIN ASSIGNMENTS

PIN	NAME	DESCRIPTION
1	V <sub>REF</sub>	Reference Input.
2	+In	Noninverting Input.
3	-In	Inverting Input. Connect to ground or to remote ground sense point.
4	GND	Ground.
5	CS/SHDN	Chip Select when LOW, Shutdown Mode when HIGH.
6	D <sub>OUT</sub>	The serial output data word is comprised of 16 bits of data. In operation the data is valid on the falling edge of DCLOCK. The second clock pulse after the falling edge of CS enables the serial output. After one null bit the data is valid for the next 16 edges.
7	DCLOCK	Data Clock synchronizes the serial data transfer and determines conversion speed.
8	+V <sub>CC</sub>	Power Supply.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

V <sub>CC</sub> .....	+6V
Analog Input .....	-0.3V to (V <sub>CC</sub> + 0.3V)
Logic Input .....	-0.3V to 6V
Case Temperature .....	+100°C
Junction Temperature .....	+150°C
Storage Temperature .....	+125°C
External Reference Voltage .....	+5.5V

NOTE: (1) Stresses above these ratings may permanently damage the device.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (%)	NO MISSING CODE ERROR (LSB)	PACKAGE	PACKAGE DESIGNATOR	SPECIFICATION TEMPERATURE RANGE	PACKAGE MARKING <sup>(2)</sup>	ORDERING NUMBER <sup>(3)</sup>	TRANSPORT MEDIA
ADS8320E	0.018	14	MSOP-8	DGK	-40°C to +85°C	A20	ADS8320E/250	Tape and Reel
ADS8320E	"	"	"	"	"	"	ADS8320E/2K5	Tape and Reel
ADS8320EB	0.012	15	MSOP-8	DGK	-40°C to +85°C	A20	ADS8320EB/250	Tape and Reel
ADS8320EB	"	"	"	"	"	"	ADS8320EB/2K5	Tape and Reel

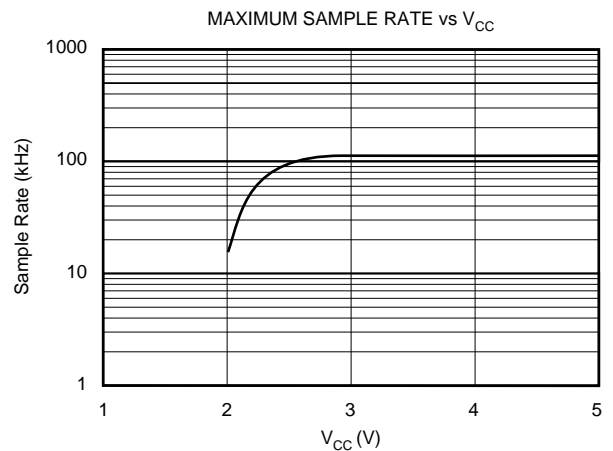
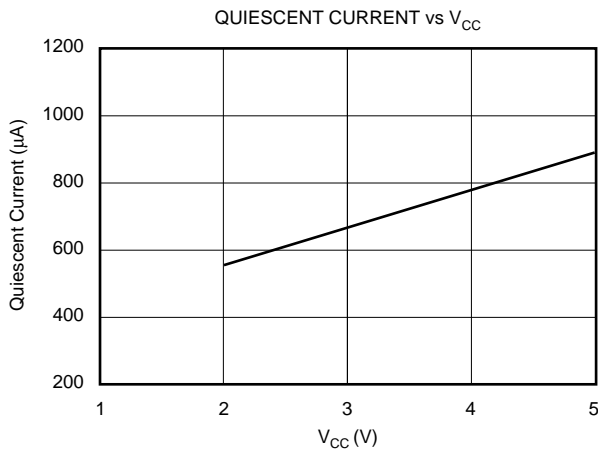
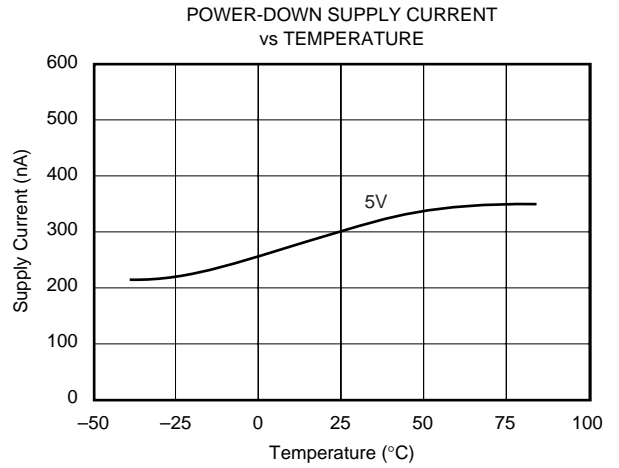
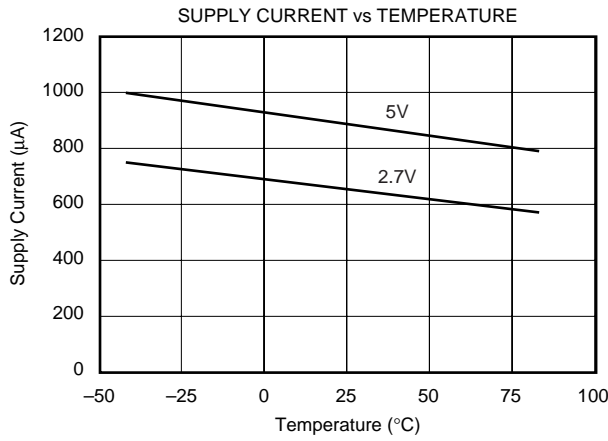
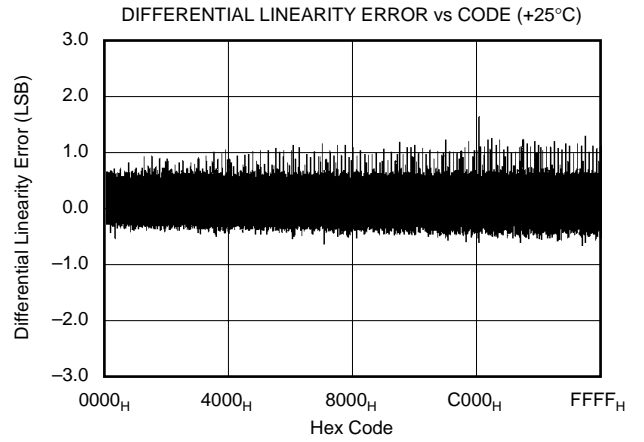
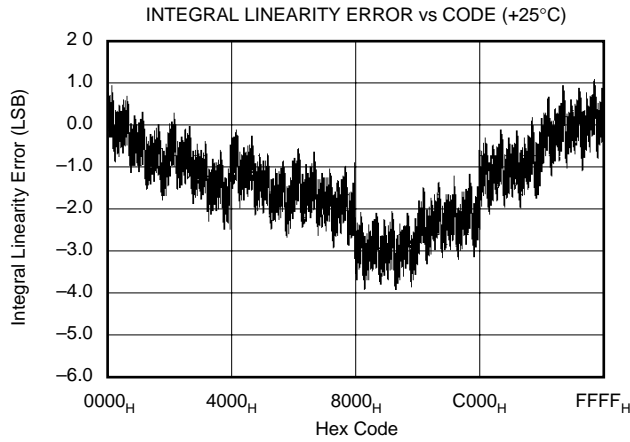
NOTES: (1) For the most current product and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Performance Grade information is marked on the reel.

(3) Models with a slash(/) are available only in tape and reel in quantities indicated (for example, /250 indicates 250 units per reel, /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of "ADS8320E/2K5" will get a single 2500-piece tape and reel.

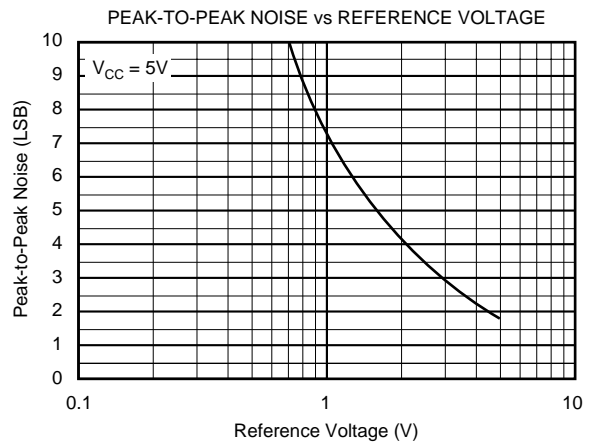
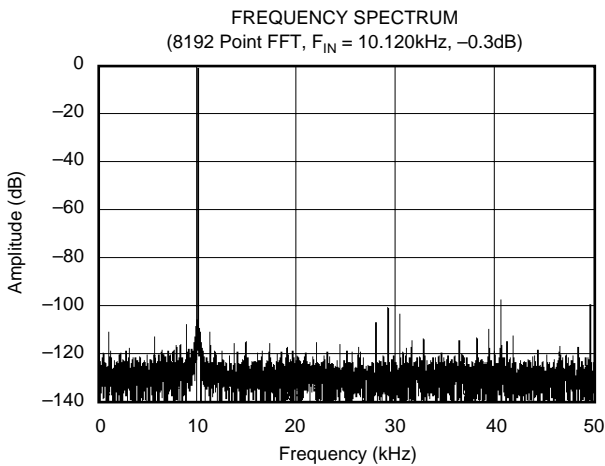
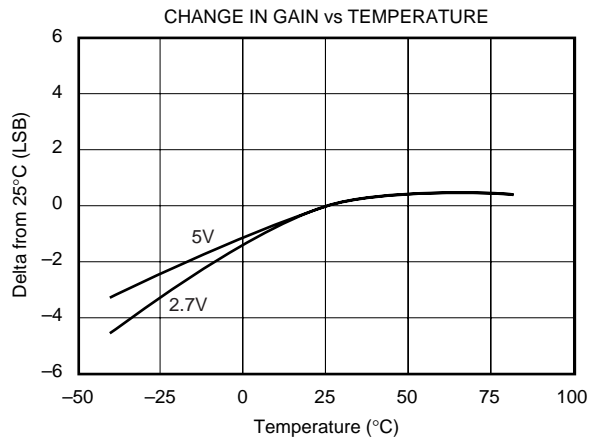
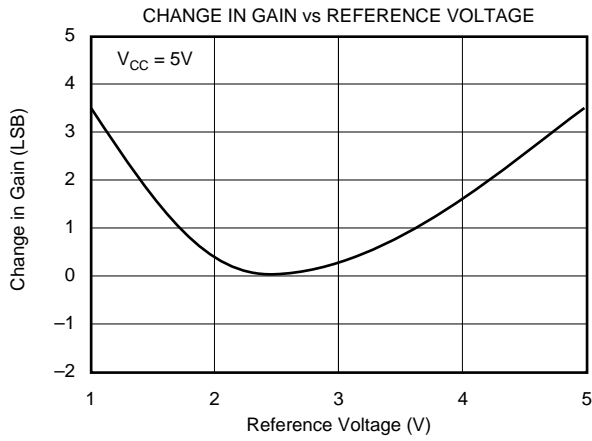
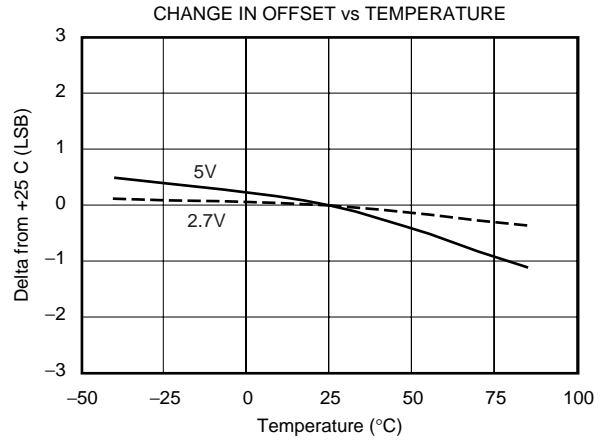
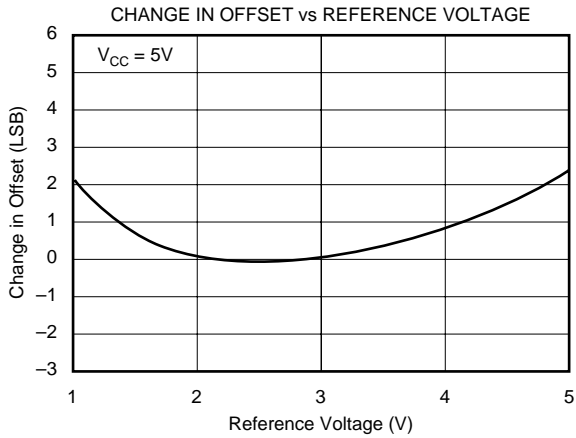
# TYPICAL PERFORMANCE CURVES

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$ ,  $V_{REF} = +5\text{V}$ ,  $f_{\text{SAMPLE}} = 100\text{kHz}$ , and  $f_{\text{CLK}} = 24 \cdot f_{\text{SAMPLE}}$ , unless otherwise specified.



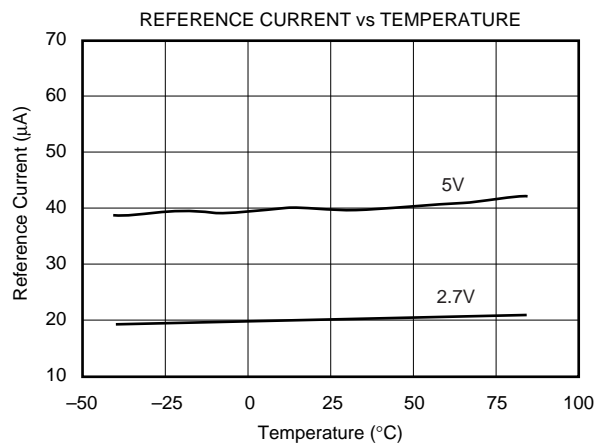
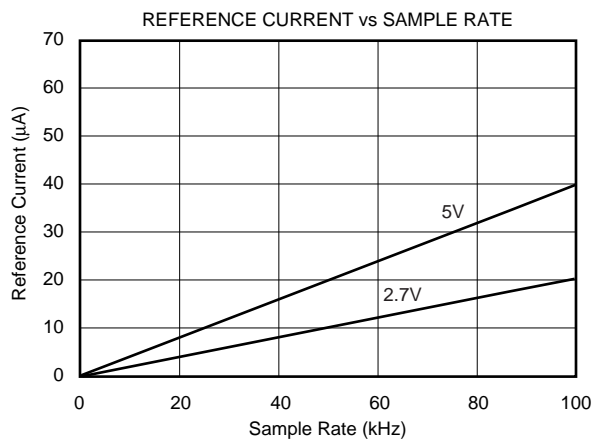
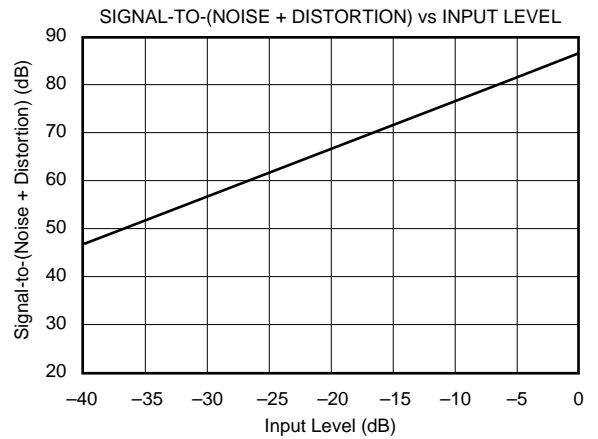
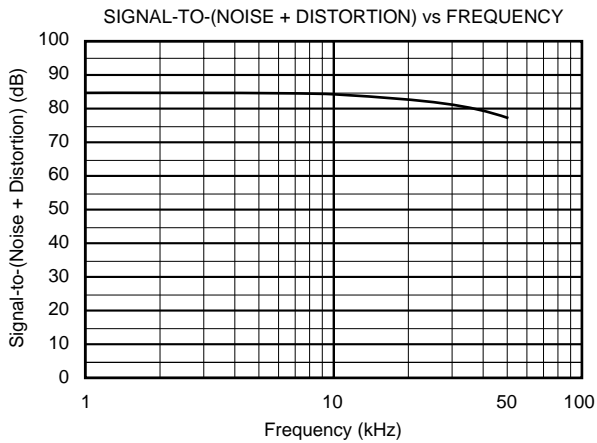
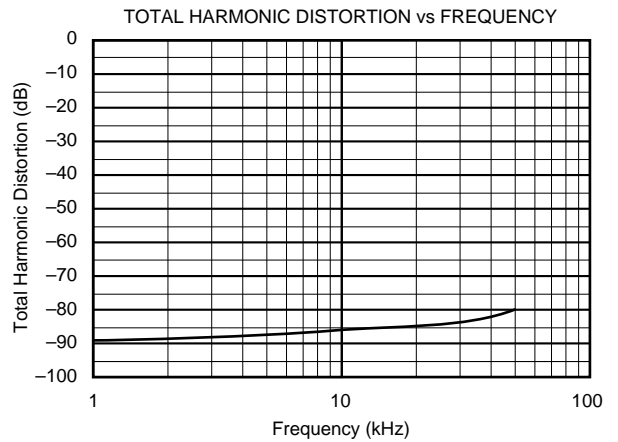
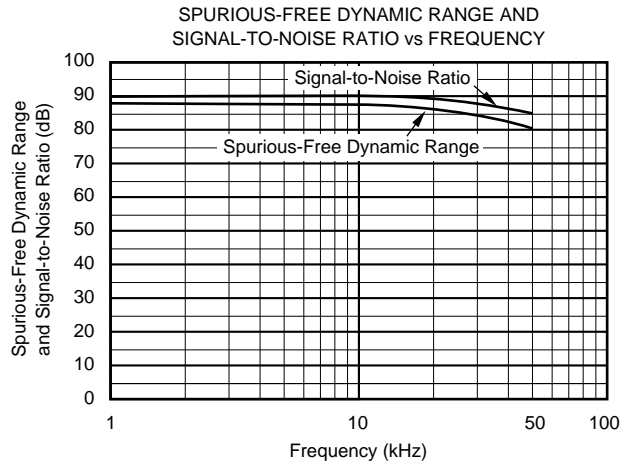
# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +2.7\text{V}$ ,  $V_{REF} = +2.5\text{V}$ ,  $f_{\text{SAMPLE}} = 100\text{kHz}$ , and  $f_{\text{CLK}} = 24 \cdot f_{\text{SAMPLE}}$ , unless otherwise specified.



# TYPICAL PERFORMANCE CURVES (Cont.)

At  $T_A = +25^\circ\text{C}$ ,  $V_{CC} = +5\text{V}$ ,  $V_{REF} = +5\text{V}$ ,  $f_{\text{SAMPLE}} = 100\text{kHz}$ , and  $f_{\text{CLK}} = 24 \cdot f_{\text{SAMPLE}}$ , unless otherwise specified.



# THEORY OF OPERATION

The ADS8320 is a classic successive approximation register (SAR) analog-to-digital (A/D) converter. The architecture is based on capacitive redistribution, which inherently includes a sample/hold function. The converter is fabricated on a 0.6 $\mu$ m CMOS process. The architecture and process allow the ADS8320 to acquire and convert an analog signal at up to 100,000 conversions per second while consuming less than 4.5mW from +V<sub>CC</sub>.

The ADS8320 requires an external reference, an external clock, and a single power source (V<sub>CC</sub>). The external reference can be any voltage between 500mV and V<sub>CC</sub>. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS8320.

The external clock can vary between 24kHz (1kHz throughput) and 2.4MHz (100kHz throughput). The duty cycle of the clock is essentially unimportant, as long as the minimum high and low times are at least 200ns (V<sub>CC</sub> = 2.7V or greater). The minimum clock frequency is set by the leakage on the capacitors internal to the ADS8320.

The analog input is provided to two input pins: +In and -In. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D<sub>OUT</sub> pin. The digital data that is provided on the D<sub>OUT</sub> pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS8320 after the conversion is complete and to obtain the serial data least significant bit first. See the digital timing section for more information.

## ANALOG INPUT

The +In and -In input pins allow for a differential input signal. Unlike some converters of this type, the -In input is not re-sampled later in the conversion cycle. When the converter goes into the hold mode, the voltage difference between +In and -In is captured on the internal capacitor array.

The range of the -In input is limited to -0.1V to +1V (-0.1V to +0.5V when using a 2.7V supply). Because of this, the differential input can be used to reject only small signals that are common to both inputs. Thus, the -In input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The input current on the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the ADS8320

charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45pF) to a 16-bit settling level within 4.5 clock cycles. When the converter goes into the hold mode or while it is in the power-down mode, the input impedance is greater than 1G $\Omega$ .

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the -In input should not drop below GND - 100mV or exceed GND + 1V. The +In input should always remain within the range of GND - 100mV to V<sub>CC</sub> + 100mV. Outside of these ranges, the converter linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used.

## REFERENCE INPUT

The external reference sets the analog input range. The ADS8320 operates with a reference in the range of 500mV to V<sub>CC</sub>. There are several important implications of this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the Least Significant Bit (LSB) size and is equal to the reference voltage divided by 65,536. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter also appears to increase with lower LSB size. With a +5V reference, the internal noise of the converter typically contributes only 1.5 LSB peak-to-peak of potential error to the output code. When the external reference is 500mV, the potential error contribution from the internal noise will be 10 times larger—15 LSBs. The errors due to the internal noise are gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult the typical performance curve “Peak-to-Peak Noise vs Reference Voltage.” Note that the Effective Number of Bits (ENOB) figure is calculated based on the converter’s signal-to-(noise + distortion) ratio with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows:

$$\text{SINAD} = 6.02 \cdot \text{ENOB} + 1.76$$

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter is also more sensitive to external sources of error such as nearby digital signals and electromagnetic interference.



## NOISE

The noise floor of the ADS8320 itself is extremely low, as can be seen from Figures 1 and 2, and is much lower than competing A/D converters. It was tested by applying a low-noise DC input and a 5.0V reference to the ADS8320 and initiating 5000 conversions. The digital output of the A/D

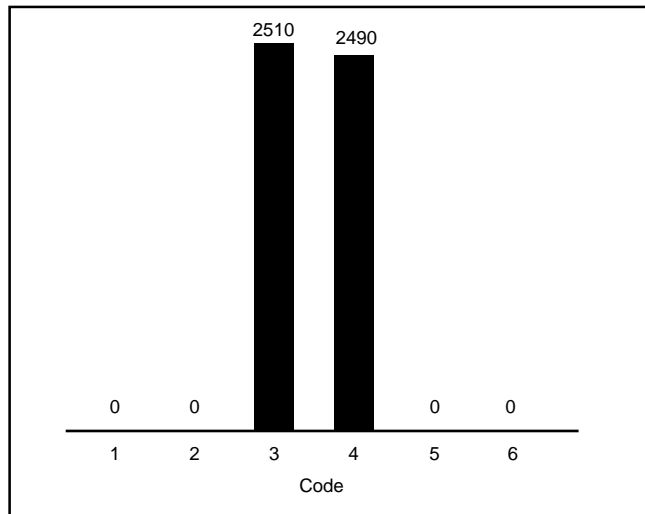


FIGURE 1. Histogram of 5000 Conversions of a DC Input at the Code Transition.

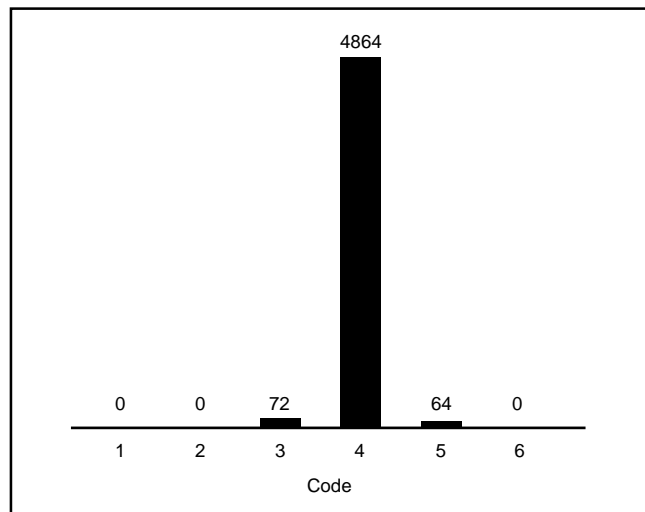


FIGURE 2. Histogram of 5000 Conversions of a DC Input at the Code Center.

converter varies in output code due to the internal noise of the ADS8320. This is true for all 16-bit SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The  $\pm 1\sigma$ ,  $\pm 2\sigma$ , and  $\pm 3\sigma$  distributions represents the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this yields the  $\pm 3\sigma$  distribution or 99.7% of all codes. Statistically, up to 3 codes could fall outside the distribution when executing 1000 conversions. The ADS8320, with  $< 3$  output codes for the  $\pm 3\sigma$  distribution, yields a  $< \pm 0.5$ LSB transition noise. Remember, to achieve this low noise performance, the peak-to-peak noise of the input signal and reference must be  $< 50\mu\text{V}$ .

## AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of  $1/\sqrt{n}$ , where  $n$  is the number of averages. For example, averaging four conversion results reduces the transition noise by 1/2 to  $\pm 0.25$  LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging; for every decimation by 2, the signal-to-noise ratio improves 3dB.

## DIGITAL INTERFACE

### SIGNAL LEVELS

The digital inputs of the ADS8320 can accommodate logic levels up to 5.5V regardless of the value of  $V_{CC}$ . Thus, the ADS8320 can be powered at 3V and still accept inputs from logic powered at 5V.

The CMOS digital output ( $D_{OUT}$ ) swings 0V to  $V_{CC}$ . If  $V_{CC}$  is 3V and this output is connected to a 5V CMOS logic input, then that IC may require more supply current than normal and may have a slightly longer propagation delay.

## SERIAL INTERFACE

The ADS8320 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface, as shown in Figure 3 and Table I. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for  $D_{OUT}$  is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

A falling  $\overline{CS}$  signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal. After the fifth falling DCLOCK edge,  $D_{OUT}$  is enabled and outputs a LOW value for one clock period. For the next 16 DCLOCK periods,  $D_{OUT}$  outputs the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks repeat the output data but in a least significant bit first format.

After the most significant bit (B15) has been repeated,  $D_{OUT}$  will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when  $\overline{CS}$  has been taken HIGH and returned LOW.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
$t_{SMPL}$	Analog Input Sample Time	4.5		5.0	Clk Cycles
$t_{CONV}$	Conversion Time		16		Clk Cycles
$t_{CYC}$	Throughput Rate			100	kHz
$t_{CSD}$	$\overline{CS}$ Falling to DCLOCK LOW			0	ns
$t_{SUCS}$	$\overline{CS}$ Falling to DCLOCK Rising	20			ns
$t_{hDO}$	DCLOCK Falling to Current $D_{OUT}$ Not Valid	5	15		ns
$t_{dDO}$	DCLOCK Falling to Next $D_{OUT}$ Valid		30	50	ns
$t_{dis}$	$\overline{CS}$ Rising to $D_{OUT}$ Tri-State		70	100	ns
$t_{en}$	DCLOCK Falling to $D_{OUT}$ Enabled		20	50	ns
$t_f$	$D_{OUT}$ Fall Time		5	25	ns
$t_r$	$D_{OUT}$ Rise Time		7	25	ns

TABLE I. Timing Specifications ( $V_{CC} = 2.7V$  and above,  $-40^{\circ}C$  to  $+85^{\circ}C$ ).

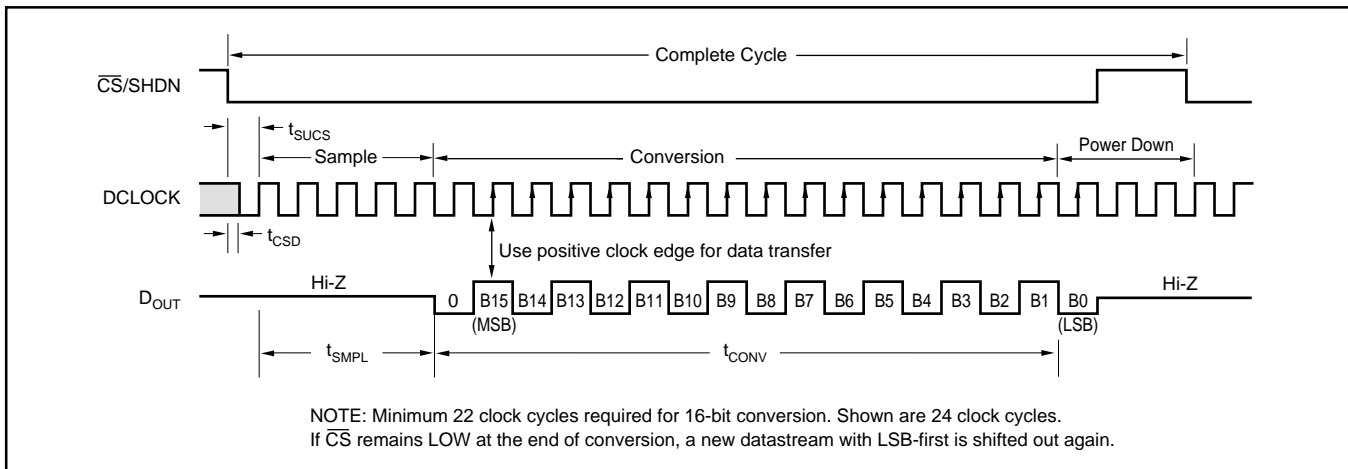


FIGURE 3. ADS8320 Basic Timing Diagrams.

## DATA FORMAT

The output data from the ADS8320 is in Straight Binary format, as shown in Table II. This table represents the ideal output code for the given input voltage and does not include the effects of offset, gain error, or noise.

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT STRAIGHT BINARY	
		BINARY CODE	HEX CODE
Full-Scale Range	$V_{REF}$		
Least Significant Bit (LSB)	$V_{REF}/65,536$		
Full-Scale	$V_{REF} - 1 \text{ LSB}$	1111 1111 1111 1111	FFFF
Midscale	$V_{REF}/2$	1000 0000 0000 0000	8000
Midscale - 1LSB	$V_{REF}/2 - 1 \text{ LSB}$	0111 1111 1111 1111	7FFF
Zero	0V	0000 0000 0000 0000	0000

TABLE II. Ideal Input Voltages and Output Codes.

## POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design allow the ADS8320 to convert at up to a 100kHz rate while requiring very little power. Still, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS8320 scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that satisfies the requirements of the system.

In addition, the ADS8320 is in power-down mode under two conditions: when the conversion is complete and whenever  $\overline{CS}$  is HIGH (as shown in Figure 3). Ideally, each conversion should occur as quickly as possible, preferably at a 2.4MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously, until the power-down mode is entered.

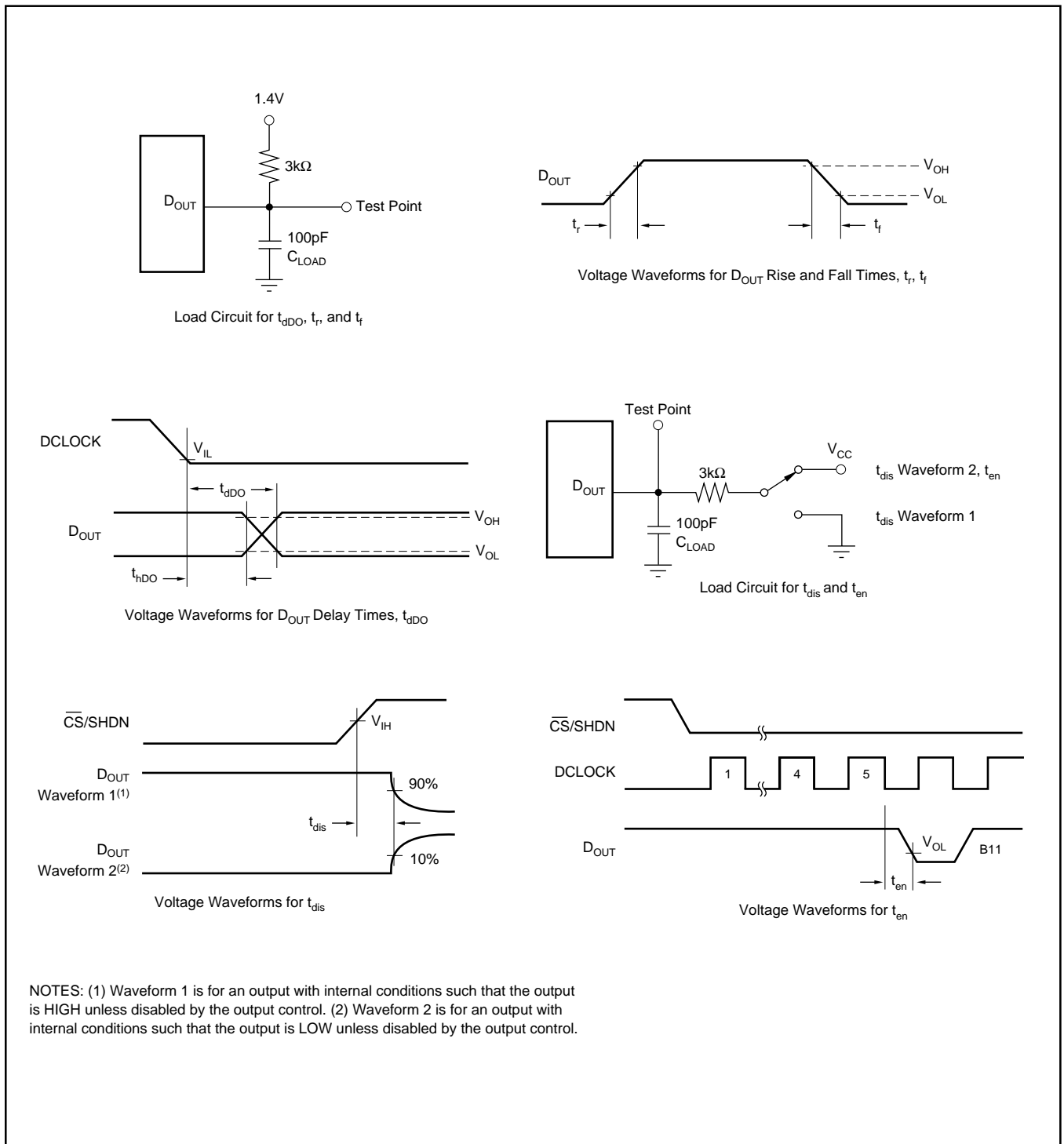


FIGURE 4. Timing Diagrams and Test Circuits for the Parameters in Table I.

Figure 5 shows the current consumption of the ADS8320 versus sample rate. For this graph, the converter is clocked at 2.4MHz regardless of the sample rate— $\overline{CS}$  is HIGH for the remaining sample period. Figure 6 also shows current consumption versus sample rate. However, in this case, the DCLOCK period is 1/24th of the sample period— $\overline{CS}$  is HIGH for one DCLOCK cycle out of every 16.

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode which is enabled when  $\overline{CS}$  is HIGH.  $\overline{CS}$  LOW will shut down only the analog section. The digital section is completely shut down only when  $\overline{CS}$  is HIGH. Thus, if  $\overline{CS}$  is left LOW at the end of a conversion and the converter is continually clocked, the power consumption will not be as low as when  $\overline{CS}$  is HIGH. Figure 7 shows more information.

Power dissipation can also be reduced by lowering the power-supply voltage and the reference voltage. The ADS8320 operates over a  $V_{CC}$  range of 2.0V to 5.25V. However, at voltages below 2.7V, the converter will not run at a 100kHz sample rate. See the typical performance curves for more information regarding power supply voltage and maximum sample rate.

### SHORT CYCLING

Another way of saving power is to utilize the  $\overline{CS}$  signal to short cycle the conversion. Because the ADS8320 places the latest data bit on the  $D_{OUT}$  line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 14 bits of the conversion result are needed, then the conversion can be terminated (by pulling  $\overline{CS}$  HIGH) after the 14th bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 16-bit conversion result may not be needed. If so, the conversion can be terminated after the first  $n$  bits, where  $n$  might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system, as they spend more time in the power-down mode.

### LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8320 circuitry. This is particularly true if the reference voltage is low and/or the conversion rate is high. At a 100kHz conversion rate, the ADS8320 makes a bit decision every 416ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 16-bit level all within one clock cycle.

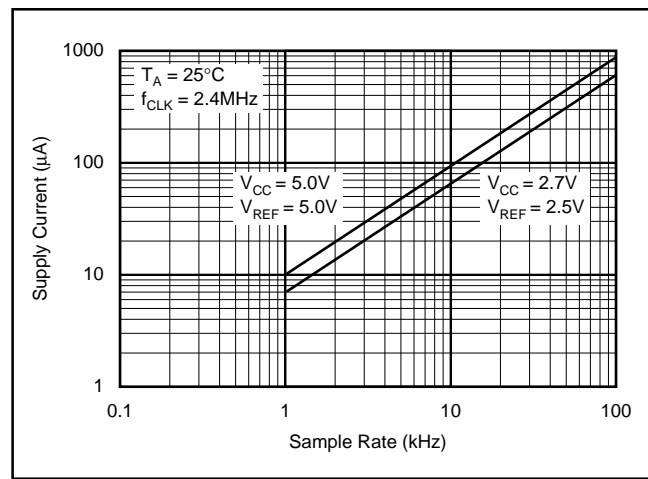


FIGURE 5. Maintaining  $f_{CLK}$  at the Highest Possible Rate Allows Supply Current to Drop Linearly with Sample Rate.

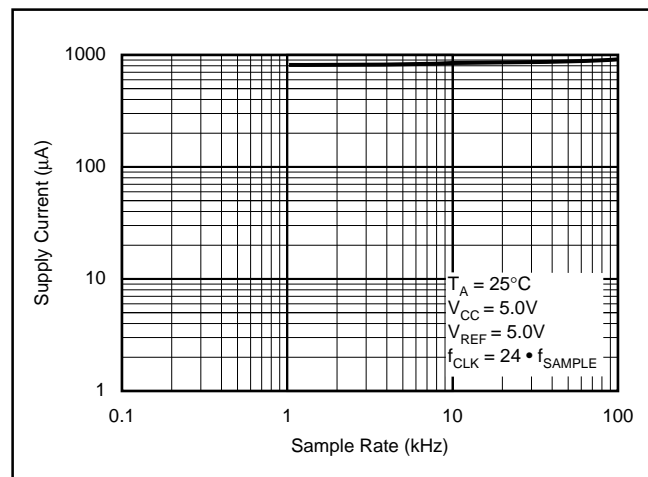


FIGURE 6. Scaling  $f_{CLK}$  Reduces Supply Current Only Slightly with Sample Rate.

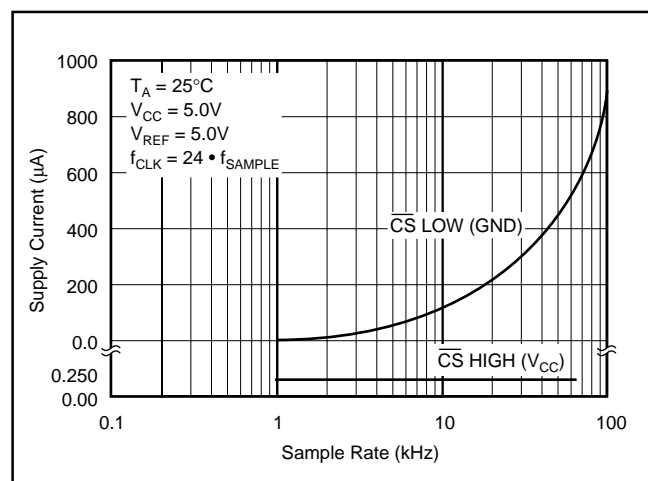


FIGURE 7. Shutdown Current with  $\overline{CS}$  HIGH is 50nA Typically, Regardless of the Clock. Shutdown Current with  $\overline{CS}$  LOW Varies with Sample Rate.

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter DCLOCK signal—as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS8320 should be clean and well bypassed. A 0.1 $\mu$ F ceramic bypass capacitor should be placed as close to the ADS8320 package as possible. In addition, a 1 $\mu$ F to 10 $\mu$ F capacitor and a 5 $\Omega$  or 10 $\Omega$  series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 0.1 $\mu$ F capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, be careful that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS8320 draws very little current from the reference on average, there are still instantaneous current demands placed on the external input and reference circuitry.

Texas Instruments' OPA627 op amp provides optimum performance for buffering both the signal and reference inputs. For low-cost, low-voltage, single-supply applications, the OPA2350 or OPA2340 dual op amps are recommended.

Also, keep in mind that the ADS8320 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50Hz or 60Hz), can be difficult to remove.

The GND pin on the ADS8320 should be placed on a clean ground point. In many cases, this will be the “analog” ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout includes an analog ground plane for the converter and associated analog circuitry.

## APPLICATION CIRCUITS

Figure 8 shows a basic data acquisition system. The ADS8320 input range is 0V to  $V_{CC}$ , as the reference input is connected directly to the power supply. The 5 $\Omega$  resistor and 1 $\mu$ F to 10 $\mu$ F capacitor filter the microcontroller “noise” on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of the noise.

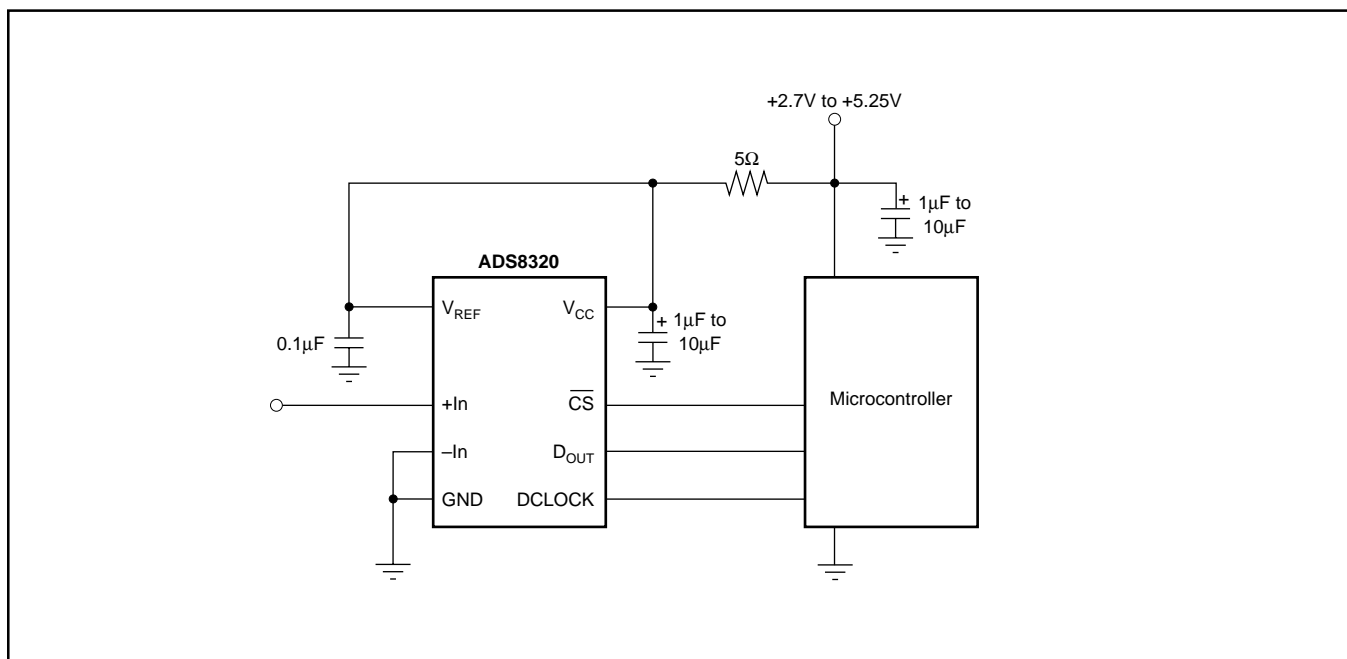


FIGURE 8. Basic Data Acquisition System.

## Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
7/21/06	C	6	Typ Performance Curves	Changed <i>CHANGE IN OFFSET</i> vs <i>TEMPERATURE</i> plot

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ADS8320E/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8320E/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8320E/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8320E/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8320EB/250	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8320EB/250G4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8320EB/2K5	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8320EB/2K5G4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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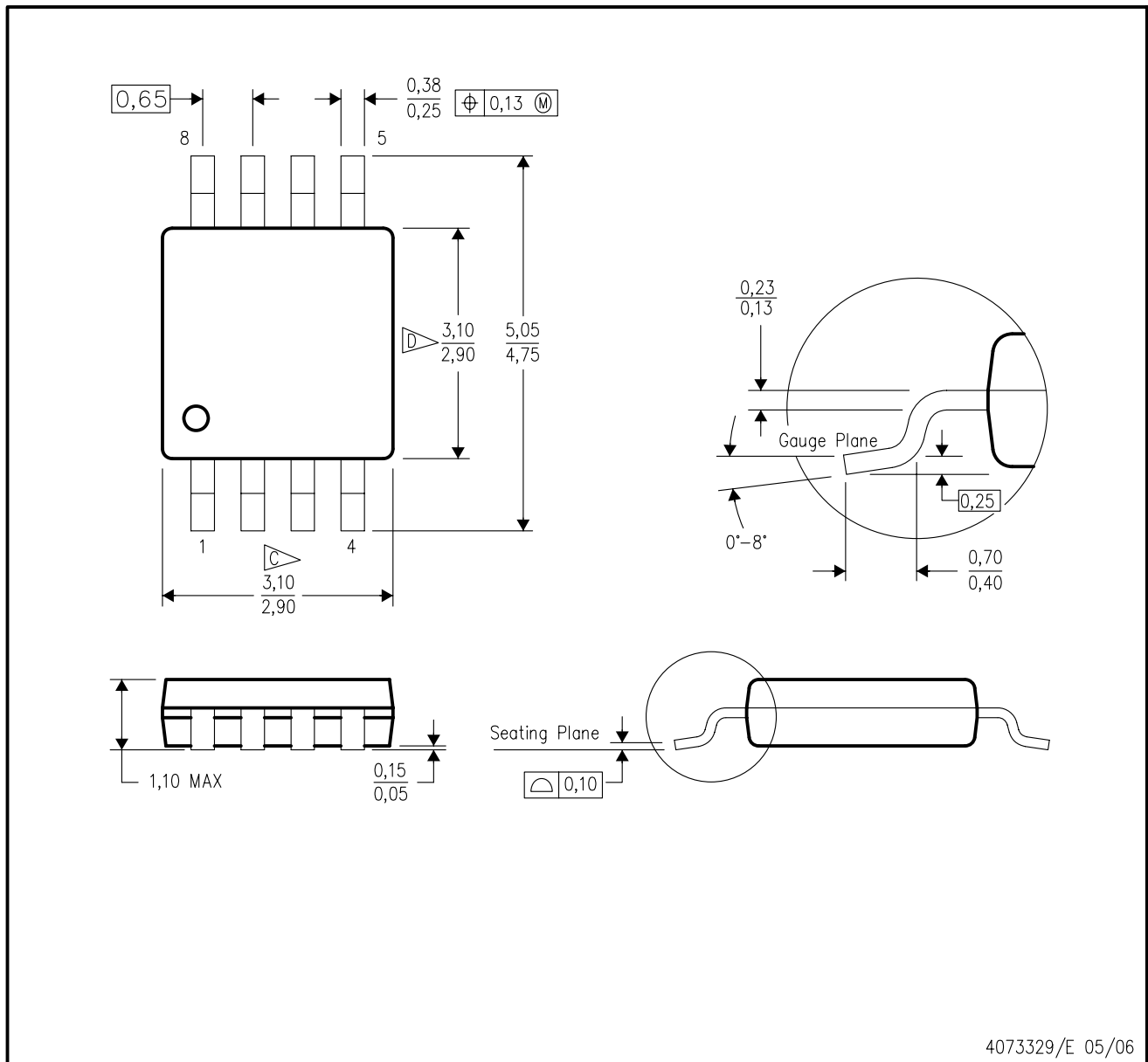
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DGK (S-PDSO-G8)

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