ADS7042 Ultra-Low Power, Ultra-Small Size, 12-Bit, 1-MSPS, SAR ADC

1 Features

- Industry's First SAR ADC with Nanowatt Power Consumption:
  - 234 µW at 1 MSPS with 1.8-V AVDD
  - 690 µW at 1 MSPS with 3-V AVDD
  - 69 µW at 100 kSPS with 3-V AVDD
  - Less than 1 µW at 1 kSPS with 3-V AVDD
- Industry's Smallest SAR ADC:
  - X2QFN-8 Package with 2.25-mm^2 Footprint
- 1-MSPS Throughput with Zero Data Latency
- Wide Operating Range:
  - AVDD: 1.8 V to 3.6 V
  - DVDD: 1.65 V to 3.6 V (Independent of AVDD)
  - Temperature Range: –40°C to 125°C
- Excellent Performance:
  - 12-Bit Resolution with NMC
  - ±1-LSB (Max) DNL and INL
  - 70-dB SNR with 3-V AVDD
  - –80-dB THD with 3-V AVDD
- Unipolar Input Range: 0 V to AVDD
- Integrated Offset Calibration
- SPI™-Compatible Serial Interface: 16 MHz
- JESD8-7A Compliant Digital I/O

2 Applications

- Low-Power Data Acquisition
- Battery-Powered Handheld Equipment
- Level Sensors
- Ultrasonic Flow Meters
- Motor Control
- Wearable Fitness
- Portable Medical Equipment
- Hard Drives
- Glucose Meters

3 Description

The ADS7042 is a 12-bit, 1-MSPS, analog-to-digital converter (ADC). The device supports a wide analog input voltage range (1.8 V to 3.6 V) and includes a capacitor-based, successive-approximation register (SAR) ADC with an inherent sample-and-hold circuit. The SPI-compatible serial interface is controlled by the $\overline{CS}$ and SCLK signals. The input signal is sampled with the $\overline{CS}$ falling edge and SCLK is used for conversion and serial data output. The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interface to a variety of host controllers. The ADS7042 complies with the JESD8-7A standard for normal DVDD range (1.65 V to 1.95 V).

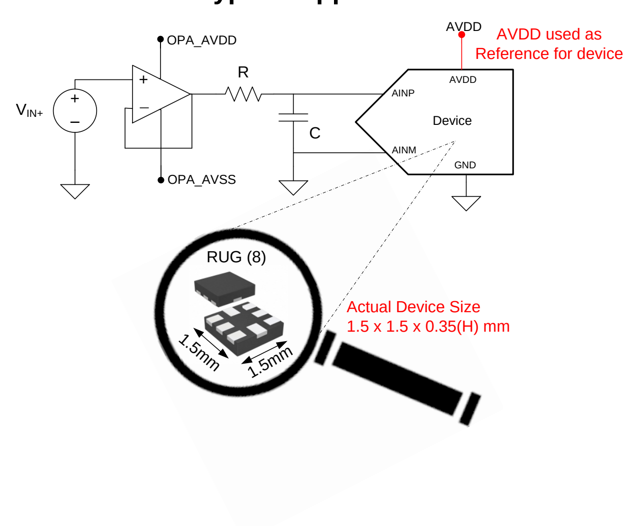
The ADS7042 is available in 8-pin, miniature, leaded, and X2QFN packages and is specified for operation from –40°C to 125°C. Miniature form-factor and extremely low-power consumption make this device suitable for space-constrained, battery-powered applications.

Device Information(1)

PART NAME	PACKAGE	BODY SIZE (NOM)
ADS7042	X2QFN (8)	1.50 mm × 1.50 mm
	VSSOP (8)	2.30 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



NOTE: The ADS7042 is smaller than a 0805 (2012 metric) SMD component.

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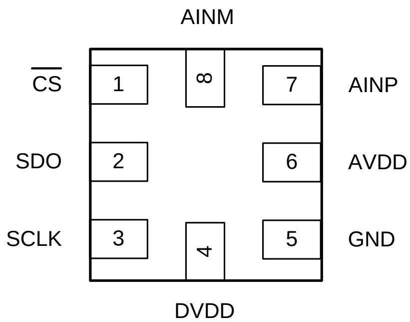
4 Revision History

Changes from Original (June 2014) to Revision A **Page**

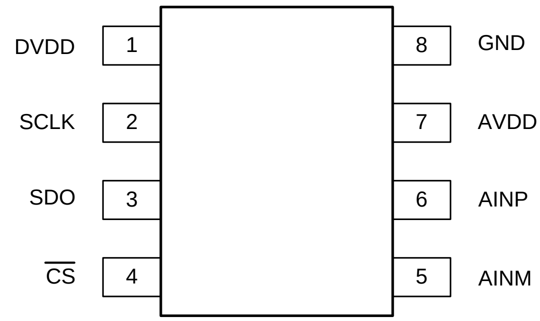
- Made changes to product preview data sheet 1

5 Pin Configurations and Functions

RUG Package
X2QFN-8
(Top View)



DCU Package
8-Pin Leaded VSSOP
(Top View)



Pin Functions

PIN			I/O	DESCRIPTION
	NO.			
NAME	RUG	DCU		
AINM	8	5	Analog input	Analog signal input, negative
AINP	7	6	Analog input	Analog signal input, positive
AVDD	6	7	Supply	Analog power-supply input, also provides the reference voltage to the ADC
$\overline{CS}$	1	4	Digital input	Chip-select signal, active low
DVDD	4	1	Supply	Digital I/O supply voltage
GND	5	8	Supply	Ground for power supply, all analog and digital signals are referred to this pin
SCLK	3	2	Digital input	Serial clock
SDO	2	3	Digital output	Serial data out

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	3.9	V
DVDD to GND	–0.3	3.9	V
AINP to GND	–0.3	AVDD + 0.3	V
AINM to GND	–0.3	0.3	V
Digital input voltage to GND	–0.3	DVDD + 0.3	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–60	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–1000	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
AVDD	Analog supply voltage range	1.8	3.6	V
DVDD	Digital supply voltage range	1.65	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS7042		UNIT
		RUG (X2QFN)	DCU (VSSOP)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.5	235.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	79.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	76.7	117.6	
ψ_{JT}	Junction-to-top characterization parameter	1.0	8.9	
ψ_{JB}	Junction-to-board characterization parameter	76.7	116.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_A = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 1 MSPS, and V_{AINM} = 0 V, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage span(1)			0		AVDD	V
	Absolute input voltage range	AINP to GND		–0.1		AVDD + 0.1	V
		AINM to GND		–0.1		0.1	V
C_S	Sampling capacitance				15		pF
SYSTEM PERFORMANCE							
	Resolution				12		Bits
NMC	No missing codes			12			Bits
INL	Integral nonlinearity		AVDD = 3 V	–1	±0.7	1	LSB(2)
			AVDD = 1.8 V	–2	±1	2	LSB
DNL	Differential nonlinearity		AVDD = 3 V	–0.99	±0.5	1	LSB
			AVDD = 1.8 V	–0.99	±0.7	2	LSB
E_O	Offset error	Uncalibrated	AVDD = 1.8 V to 3.6 V		±12		LSB
		Calibrated(3)	AVDD = 3 V	–3	±0.5	3	LSB
			AVDD = 1.8 V	–4	±1	4	LSB
dV_{OS}/dT	Offset error drift with temperature				5		ppm/°C
E_G	Gain error		AVDD = 3 V	–0.1	±0.05	0.1	%FS
			AVDD = 1.8 V	–0.2	±0.1	0.2	%FS
	Gain error drift with temperature				2		ppm/°C
SAMPLING DYNAMICS							
t_{ACQ}	Acquisition time			200			ns
	Maximum throughput rate		16-MHz SCLK, AVDD = 1.8 V to 3.6 V			1	MHz
DYNAMIC CHARACTERISTICS							
SNR	Signal-to-noise ratio(4)		f_{IN} = 2 kHz, AVDD = 3 V	69	70		dB
			f_{IN} = 2 kHz, AVDD = 1.8 V		68		dB
THD	Total harmonic distortion(4)(5)		f_{IN} = 2 kHz, AVDD = 3 V		–80		dB
SINAD	Signal-to-noise and distortion(4)		f_{IN} = 2 kHz, AVDD = 3 V	68	69.5		dB
			f_{IN} = 2 kHz, AVDD = 1.8 V		67.5		dB
SFDR	Spurious-free dynamic range(4)		f_{IN} = 2 kHz, AVDD = 3 V		80		dB
$BW_{(fp)}$	Full-power bandwidth		At –3 dB, AVDD = 3 V		25		MHz
DIGITAL INPUT/OUTPUT (CMOS Logic Family)							
V_{IH}	High-level input voltage(6)			0.65 DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage(6)			–0.3		0.35 DVDD	V
V_{OH}	High-level output voltage(6)		At I_{source} = 500 µA	0.8 DVDD		DVDD	V
			At I_{source} = 2 mA	DVDD – 0.45		DVDD	V
V_{OL}	Low-level output voltage(6)		At I_{sink} = 500 µA	0		0.2 DVDD	V
			At I_{sink} = 2 mA	0		0.45	V

(1) Ideal input span; does not include gain or offset error.
(2) LSB means least significant bit.
(3) Refer to the *Offset Calibration* section for more details.
(4) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified..
(5) Calculated on the first nine harmonics of the input frequency.
(6) Digital voltage levels comply with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. See the *Digital Voltage Levels* section for more details.

Electrical Characteristics (continued)

At T_A = –40°C to 125°C, AVDD = 3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 1 MSPS, and V_{AINM} = 0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		1.8	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
I_{AVDD}	Analog supply current	At 1 MSPS with AVDD = 3 V			230	µA
		At 100 kSPS with AVDD = 3 V			23	µA
		At 1 MSPS with AVDD = 1.8 V		130		µA
P_D	Power dissipation	At 1 MSPS with AVDD = 3 V			690	µW
		At 100 kSPS with AVDD = 3 V			69	µW
		At 1 MSPS with AVDD = 1.8 V		234		µW

6.6 Timing Characteristics

All specifications are at T_A = –40°C to 125°C, AVDD = 1.8 V to 3.6 V, and DVDD = 1.65 V to 3.6 V, unless otherwise specified.

PARAMETER		MIN	TYP	MAX	UNIT
TIMING SPECIFICATIONS					
$f_{THROUGHPUT}$	Throughput			1	MSPS
t_{CYCLE}	Cycle time	1			µs
t_{CONV}	Conversion time			$12.5 \times t_{SCLK} + t_{SU\_CSCK}$	ns
t_{DV_CSDO}	Delay time: $\overline{CS}$ falling to data enable			10	ns
t_{D_CKDO}	Delay time: SCLK falling to (next) data valid on DOUT			30	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to DOUT going to 3-state	5			ns
TIMING REQUIREMENTS					
t_{ACQ}	Acquisition time	200			ns
f_{SCLK}	SCLK frequency			16	MHz
t_{SCLK}	SCLK period	62.5			ns
t_{PH_CK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{PL_CK}	SCLK low time	0.45		0.55	t_{SCLK}
t_{PH_CS}	$\overline{CS}$ high time	60			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns

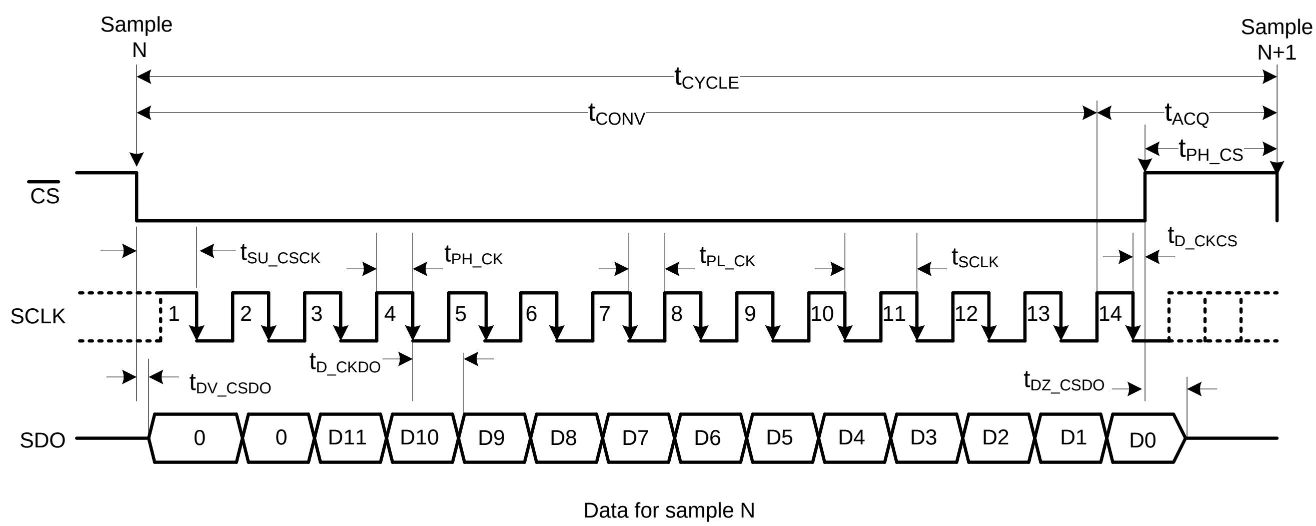
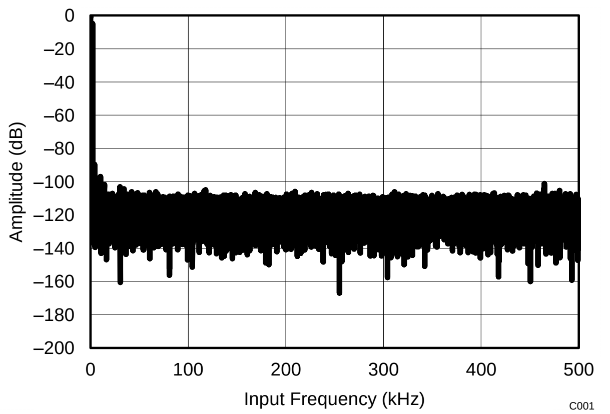


Figure 1. Timing Diagram

6.7 Typical Characteristics

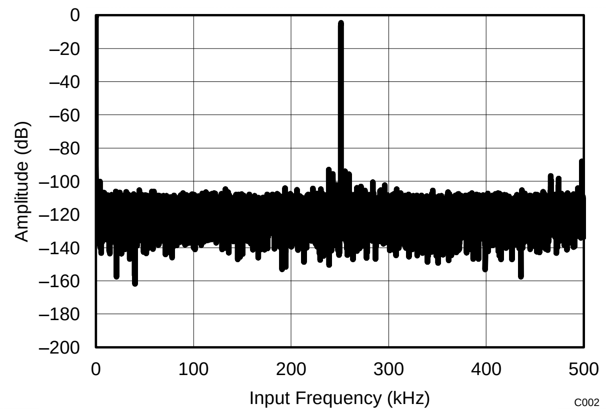
At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.



SNR = 70.62 dB THD = –83.96 dB f_{IN} = 2 kHz

Number of samples = 32768

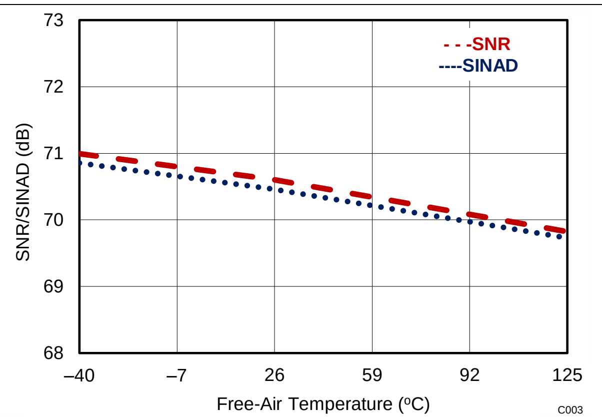
Figure 2. Typical FFT



SNR = 70.22 dB THD = –81.58 dB f_{IN} = 250 kHz

Number of samples = 32768

Figure 3. Typical FFT



f_{IN} = 2 kHz

Figure 4. SNR and SINAD vs Temperature

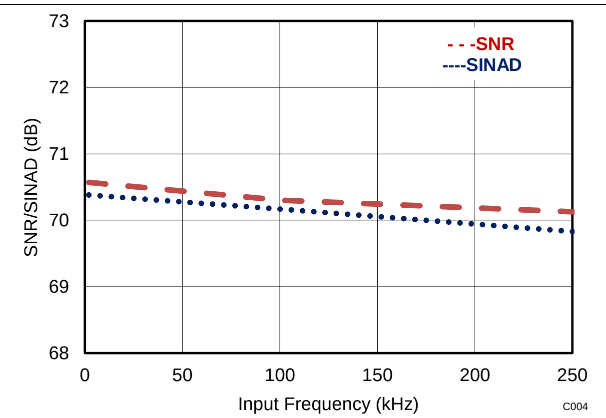


Figure 5. SNR and SINAD vs Input Frequency

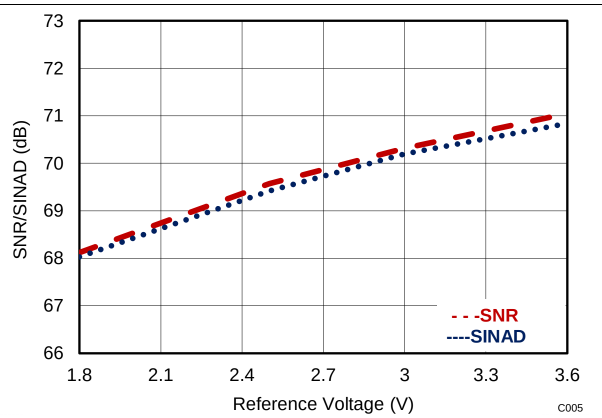


Figure 6. SNR and SINAD vs Reference Voltage (AVDD)

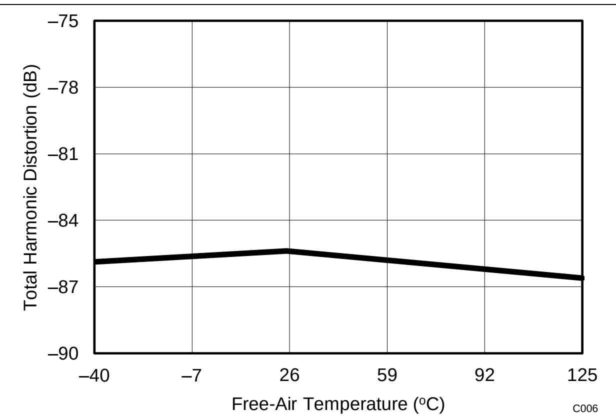


Figure 7. THD vs Free-Air Temperature

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

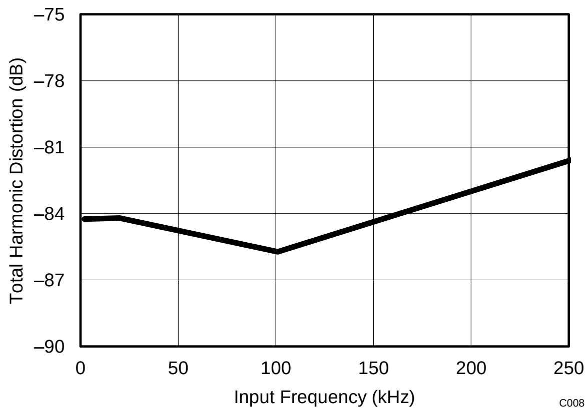


Figure 8. THD vs Input Frequency

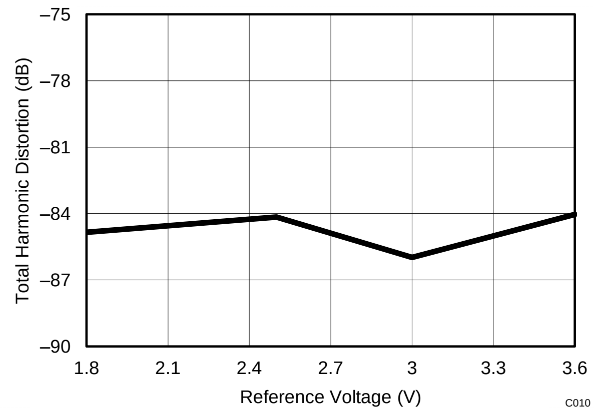


Figure 9. THD vs Reference Voltage (AVDD)

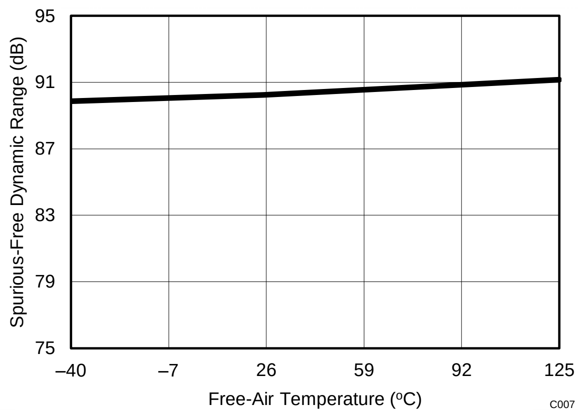


Figure 10. SFDR vs Free-Air Temperature

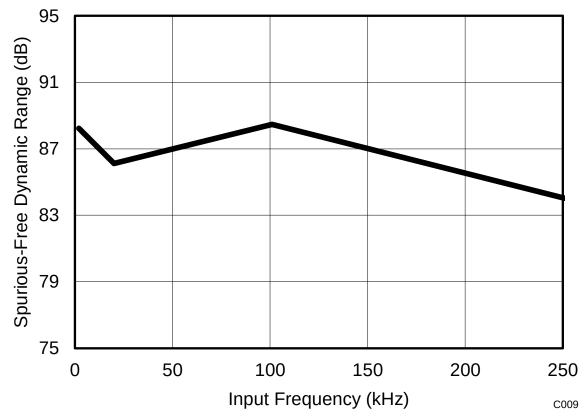


Figure 11. SFDR vs Input Frequency

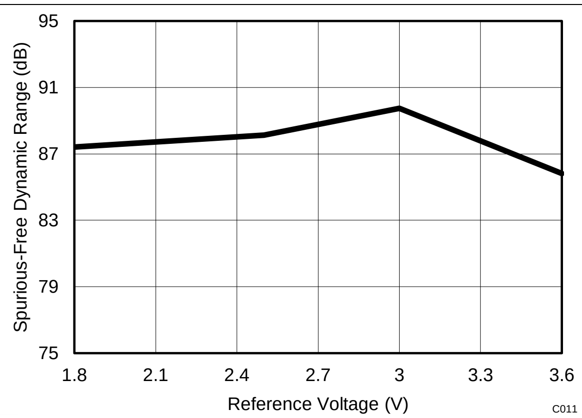
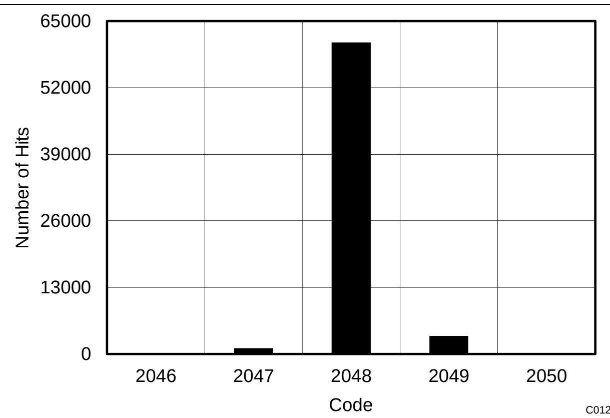


Figure 12. SFDR vs Reference Voltage (AVDD)



Mean code = 2048.04 Sigma = 0.27

Figure 13. DC Input Histogram

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.

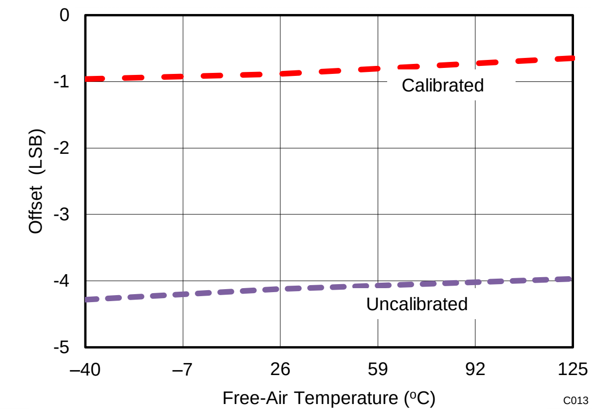


Figure 14. Offset vs Free-Air Temperature

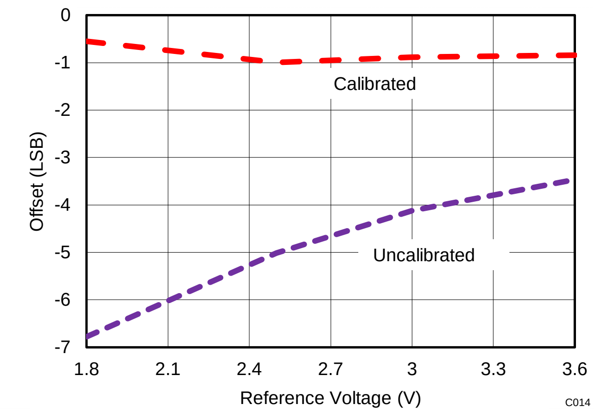


Figure 15. Offset vs Reference Voltage (AVDD)

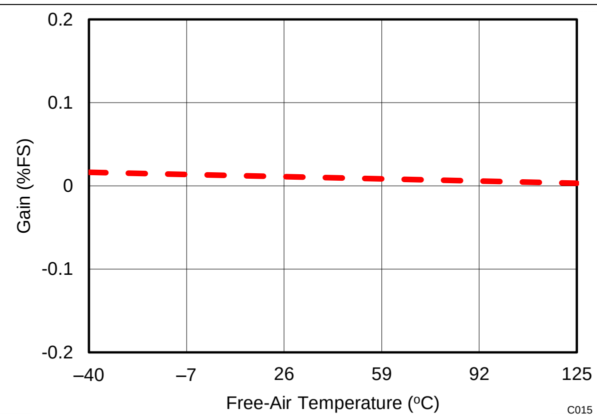


Figure 16. Gain Error vs Free-Air Temperature

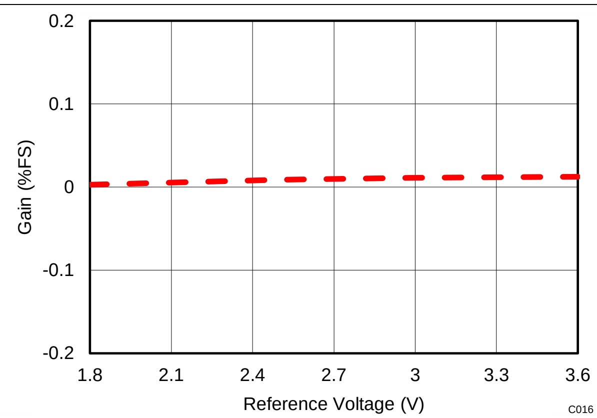
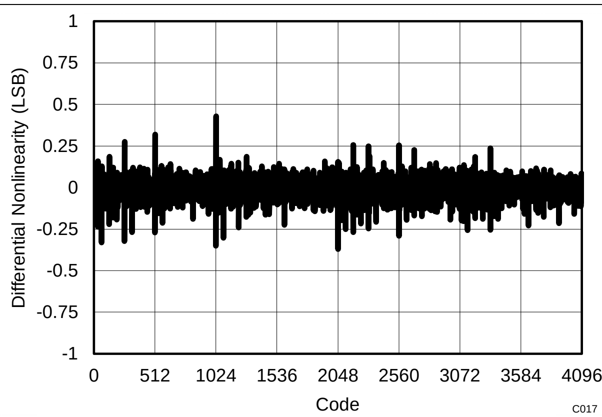
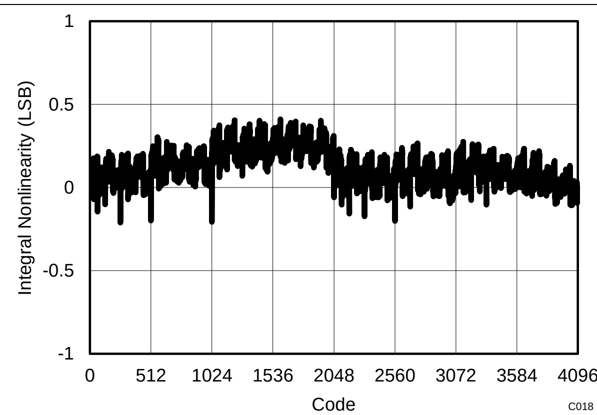


Figure 17. Gain Error vs Reference Voltage (AVDD)



AVDD = 3 V

Figure 18. Typical DNL

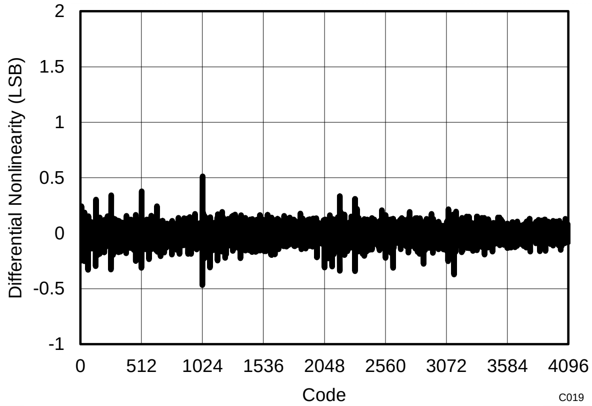


AVDD = 3 V

Figure 19. Typical INL

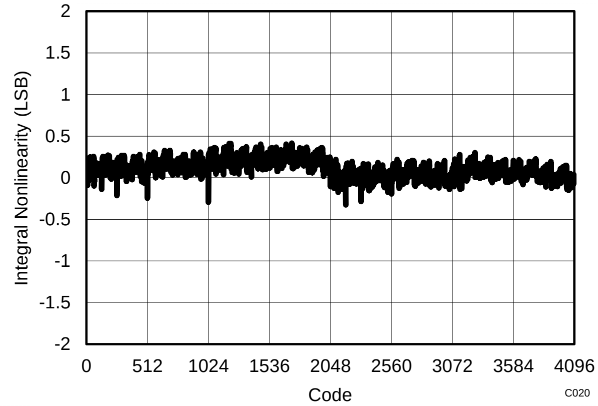
Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.



AVDD = 1.8 V

Figure 20. Typical DNL



AVDD = 1.8 V

Figure 21. Typical INL

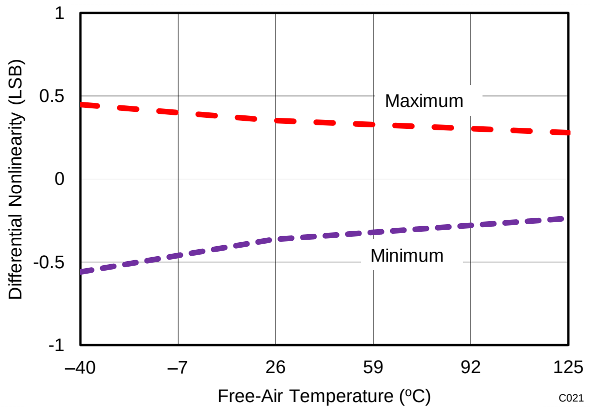


Figure 22. DNL vs Free-Air-Temperature

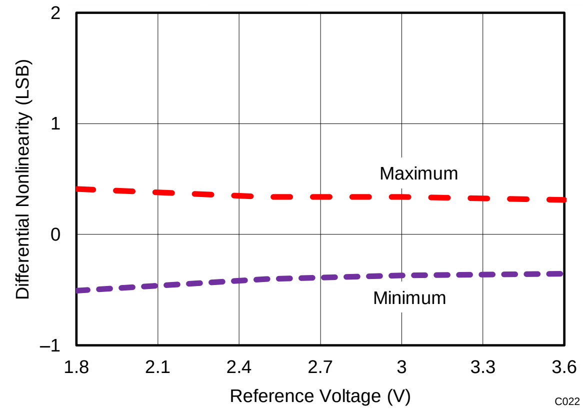


Figure 23. DNL vs Reference Voltage (AVDD)

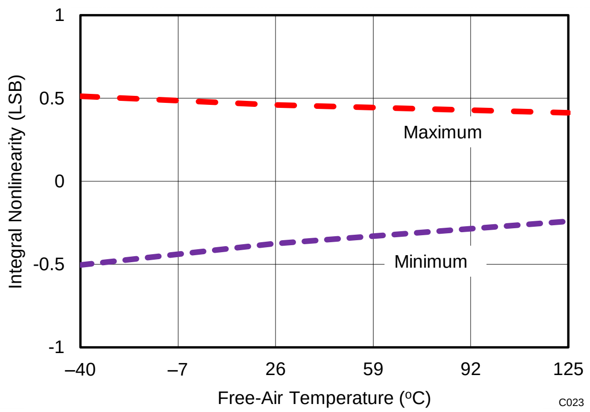


Figure 24. INL vs Free-Air-Temperature

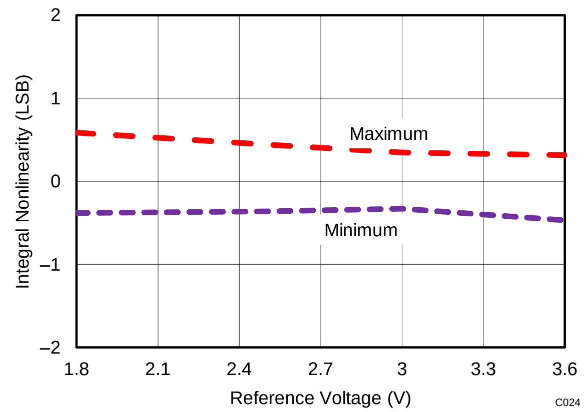
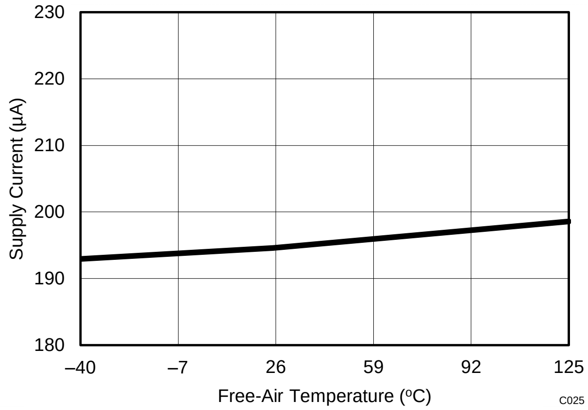


Figure 25. INL vs Reference Voltage (AVDD)

Typical Characteristics (continued)

At T_A = 25°C, AVDD = 3 V, DVDD = 1.8 V, and f_{SAMPLE} = 1 MSPS, unless otherwise noted.



f_{Sample} = 1 MSPS

Figure 26. Supply Current vs Free-Air Temperature

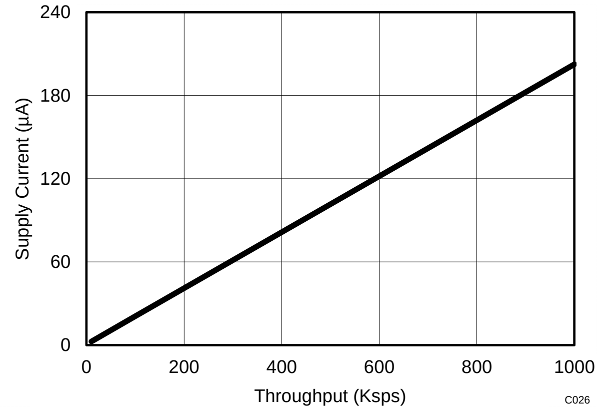


Figure 27. Supply Current vs Throughput

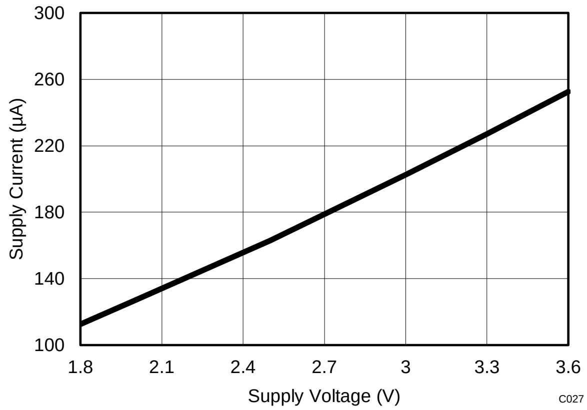


Figure 28. Supply Current vs AVDD

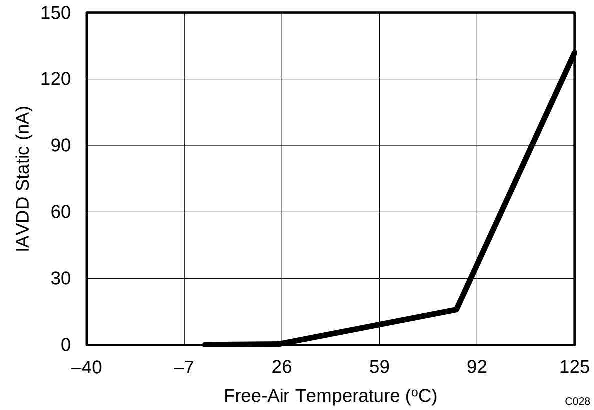


Figure 29. Static Current vs Free-Air Temperature

7 Parameter Measurement Information

7.1 Digital Voltage Levels

The device complies with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. Figure 30 shows voltage levels for the digital input and output pins.

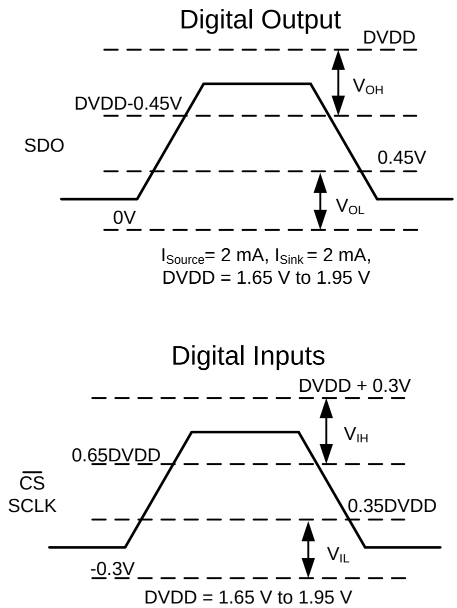


Figure 30. Digital Voltage Levels as per the JESD8-7A Standard

8 Detailed Description

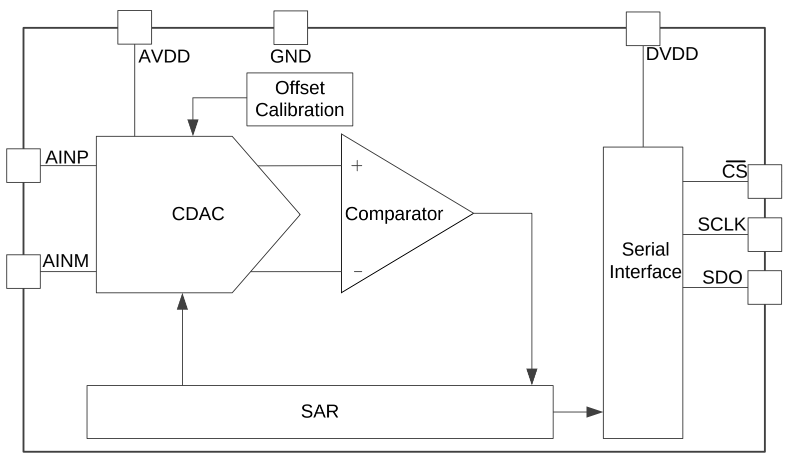
8.1 Overview

The ADS7042 is an ultralow-power, ultra-small analog-to-digital converter (ADC) that supports a wide analog input range. The analog input range for the device is defined by the AVDD supply voltage. The device samples the input voltage across the AINP and AINM pins on the $\overline{CS}$ falling edge and starts the conversion. The clock provided on the SCLK pin is used for conversion and data transfer. During conversions, both the AINP and AINM pins are disconnected from the sampling circuit. After the conversion completes, the sampling capacitors are reconnected across the AINP and AINM pins and the ADS7042 enters acquisition phase.

The device has an internal offset calibration. The offset calibration can be initiated by the user either on power-up or during normal operation; see the *Offset Calibration* section for more details.

The device also provides a simple serial interface to the host controller and operates over a wide range of digital power supplies. The ADS7042 requires only a 16-MHz SCLK for supporting a throughput of 1 MSPS. The digital interface also complies with the JESD8-7A (normal range) standard. The *Functional Block Diagram* section provides a block diagram of the device.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reference

The device uses the analog supply voltage (AVDD) as a reference. The AVDD pins must be decoupled with a 1-µF, low equivalent series resistance (ESR), ceramic capacitor, as shown in Figure 31. The AVDD pin functions as a switched capacitor load to the source powering AVDD. The decoupling capacitor provides the instantaneous charge required by the internal circuit and helps in maintaining a stable dc voltage on the AVDD pin. TI recommends powering the AVDD pin with a low output impedance and low-noise regulator (such as the TPS79101).

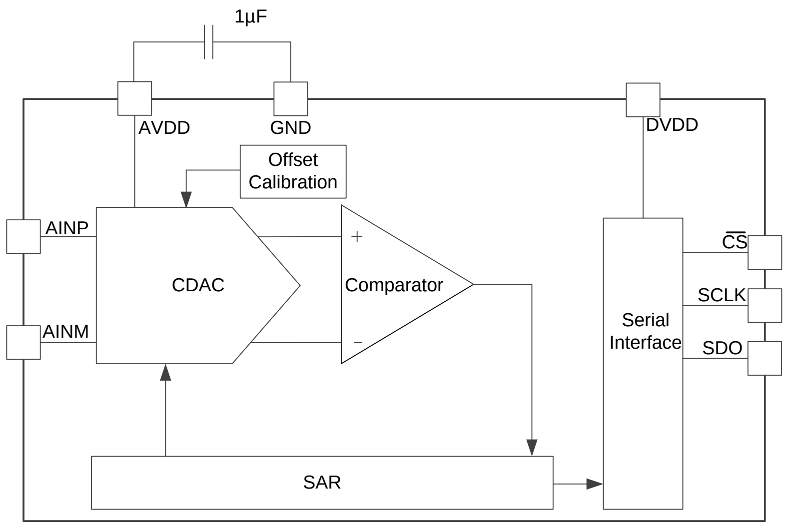


Figure 31. Reference for the Device

Feature Description (continued)

8.3.2 Analog Input

The device supports single-ended analog inputs. The ADC samples the difference between AINP and AINM and converts for this voltage. The device is capable of accepting a signal from –100 mV to 100 mV on the AINM input and is useful in systems where the sensor or signal-conditioning block is far from the ADC. In such a scenario, there can be a difference between the ground potential of the sensor or signal conditioner and the ADC ground. In such cases, use separate wires to connect the ground of the sensor or signal conditioner to the AINM pin. The AINP input is capable of accepting signals from 0 V to AVDD. Figure 32 represents the equivalent analog input circuits for the sampling stage. The device has a low-pass filter followed by the sampling switch and sampling capacitor. The sampling switch is represented by an R_S(typically 50 Ω) resistor in series with an ideal switch and C_S (typically 15 pF) is the sampling capacitor. The ESD diodes are connected from both analog inputs to AVDD and ground.

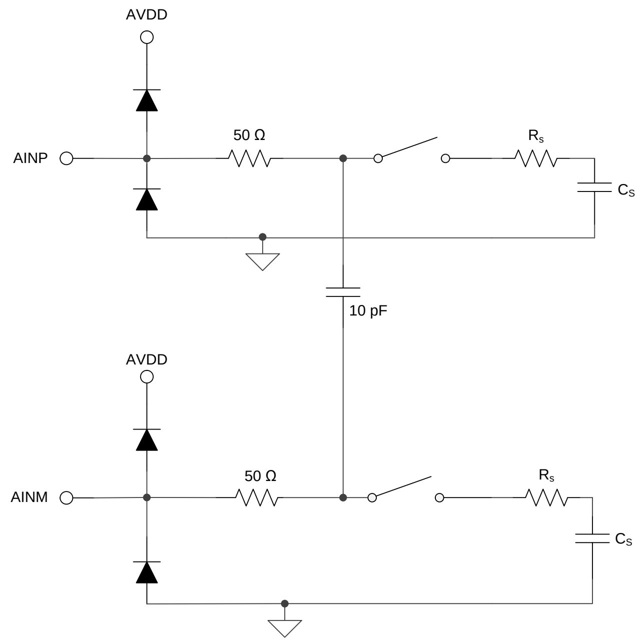


Figure 32. Equivalent Input Circuit for the Sampling Stage

The analog input full-scale range (FSR) is equal to the reference voltage of the ADC. The reference voltage for the device is equal to the analog supply voltage (AVDD). Thus, the device FSR can be determined by Equation 1:

$$FSR = V_{REF} = AVDD \tag{1}$$

8.3.3 ADC Transfer Function

The device output is in straight binary format. The device resolution for a single-ended input can be computed by Equation 2:

$$1\ LSB = V_{REF} / 2^N$$

where:

- V_{REF} = AVDD and
- N = 12 (2)

Feature Description (continued)

Figure 33 and Table 1 show the ideal transfer characteristics for the device.

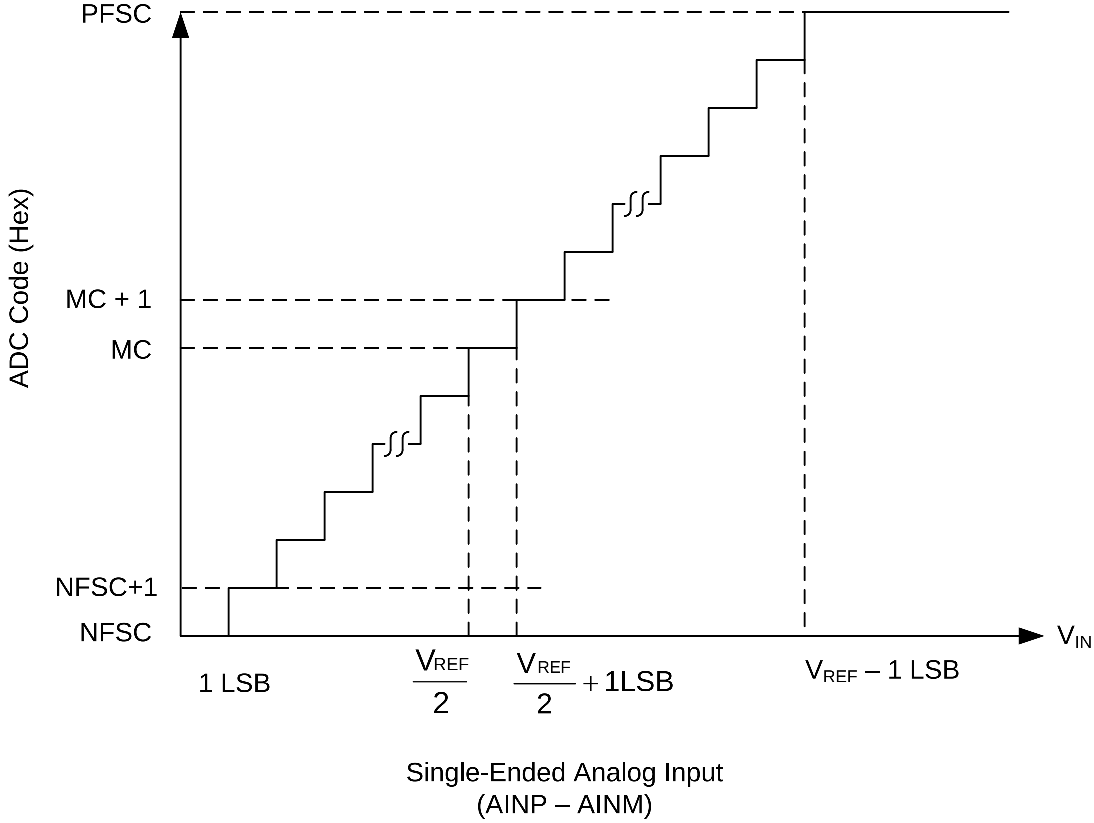


Figure 33. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINP – AINM)	CODE	DESCRIPTION	IDEAL OUTPUT CODE
≤1 LSB	NFSC	Negative full-scale code	000
1 LSB to 2 LSBs	NFSC + 1	—	001
(V_{REF} / 2) to (V_{REF} / 2) + 1 LSB	MC	Mid code	800
(V_{REF} / 2) + 1 LSB to (V_{REF} / 2) + 2 LSBs	MC + 1	—	801
≥ V_{REF} – 1 LSB	PFSC	Positive full-scale code	FFF

8.3.4 Serial Interface

The device supports a simple, SPI-compatible interface to the external host. The $\overline{CS}$ signal defines one conversion and serial transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO pin outputs the ADC conversion results. Figure 34 shows a detailed timing diagram for the serial interface. A minimum delay of t_{SU_CSCK} must elapse between the $\overline{CS}$ falling edge and the first SCLK falling edge. The device uses the clock provided on the SCLK pin for conversion and data transfer. The conversion result is available on the SDO pin with the first two bits set to 0, followed by 12 bits of the conversion result. The last bit (bit 0) is shifted out of SDO on the 14th SCLK falling edge. The SDO output remains low after the 14th SCLK falling edge if more than 14 SCLKs are provided in one serial transfer frame. A $\overline{CS}$ rising edge ends the frame and brings the serial data bus to 3-state. For the acquisition of the next sample, a minimum time of t_{ACQ} must be provided after the conversion of the current sample is completed.

The device initiates an offset calibration on the first $\overline{CS}$ falling edge after power-up and the SDO output remains low during the first serial transfer frame after power-up. For further details, refer to the *Offset Calibration* section.

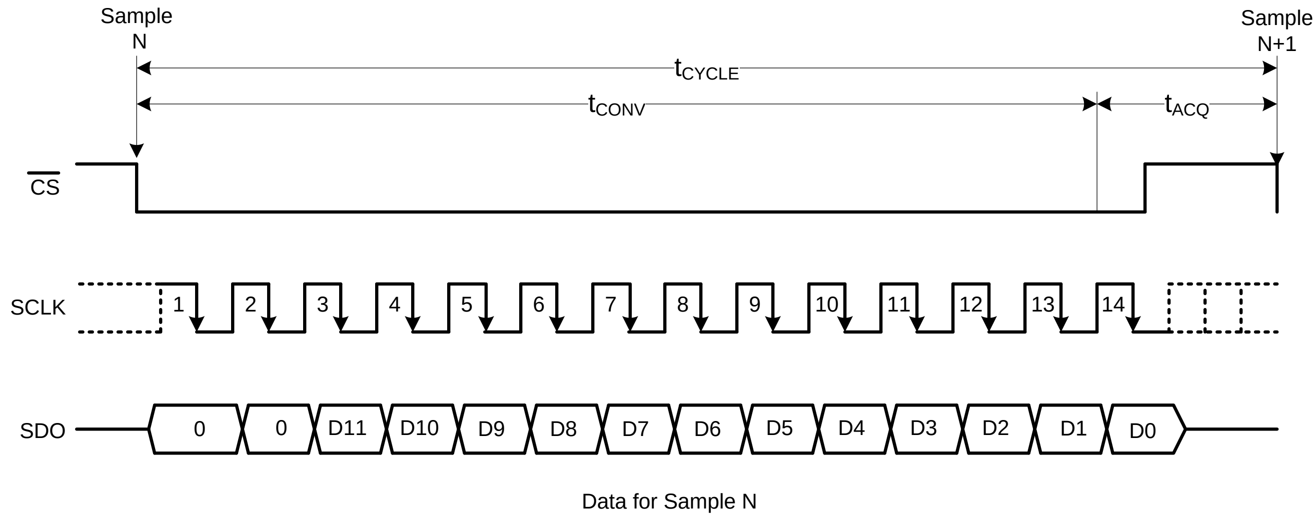
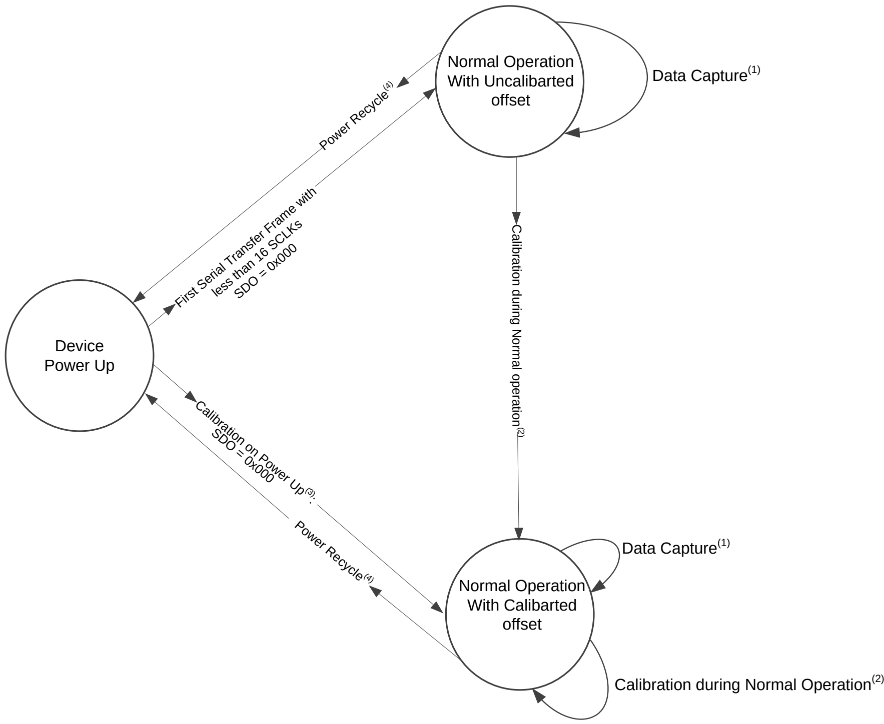


Figure 34. Serial Interface Timing Diagram

8.4 Device Functional Modes

8.4.1 Offset Calibration

The ADS7042 includes a feature to calibrate the device internal offset. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage. The device includes an internal offset calibration register (OCR) that stores the offset calibration result. The OCR is an internal register and cannot be accessed by the user through the serial interface. The OCR is reset to zero on power-up. Therefore, TI recommends calibrating the offset on power-up to bring the offset within the specified limits. If the operating temperature or analog supply voltage reflect a significant change, the offset can be recalibrated during normal operation. Figure 35 shows the offset calibration process.



(1) See the *Timing Characteristics* section for timing specifications.
(2) See the *Offset Calibration During Normal Operation* section for details.
(3) See the *Offset Calibration on Power-Up* section for details.
(4) The power recycle on the AVDD supply is required to reset the offset calibration and to bring the device to a power-up state.

Figure 35. Offset Calibration

Device Functional Modes (continued)

8.4.1.1 Offset Calibration on Power-Up

The device initiates offset calibration on the first $\overline{CS}$ falling edge after power-up and calibration completes if the $\overline{CS}$ pin remains low for at least 16 SCLK falling edges after the first $\overline{CS}$ falling edge. The SDO output remains low during calibration. The minimum acquisition time must be provided after calibration for acquiring the first sample. If the device is not provided with at least 16 SCLKs during the first serial transfer frame after power-up, the OCR is not updated. Table 2 provides the timing parameters for offset calibration on power-up.

For subsequent samples, the device adjusts the conversion results with the value stored in the OCR. The conversion result adjusted with the value stored in OCR is provided by the device on the SDO output. Figure 36 shows the timing diagram for offset calibration on power-up.

Table 2. Offset Calibration on Power-Up

PARAMETER		MIN	TYP	MAX	UNIT
$f_{CLK\text{-}CAL}$	SCLK frequency for calibration at 2.25 V < AVDD < 3.6 V			16	MHz
$f_{CLK\text{-}CAL}$	SCLK frequency for calibration at 1.8 V < AVDD < 2.25 V			12	MHz
$t_{POWERUP\text{-}CAL}$	Calibration time at power-up	15 t_{SCLK}			ns
t_{ACQ}	Acquisition time	200			ns
t_{PH_CS}	$\overline{CS}$ high time	t_{ACQ}			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns

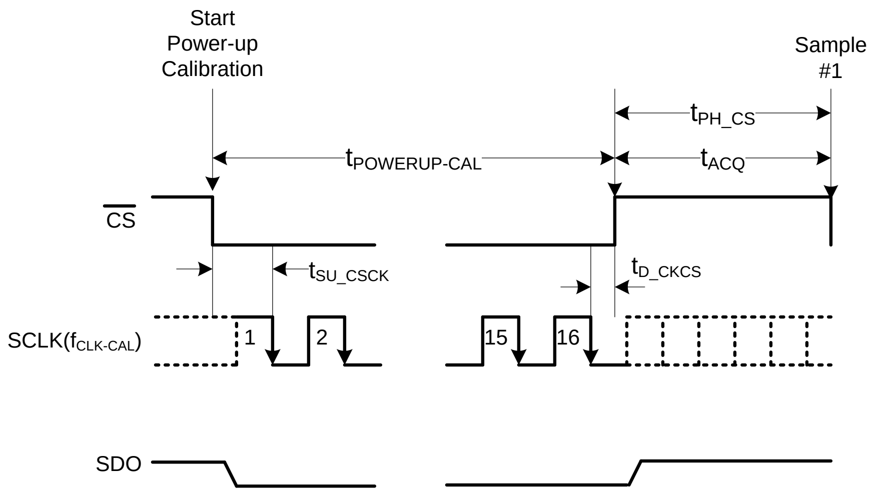


Figure 36. Offset Calibration on Power-Up Timing Diagram

8.4.1.2 Offset Calibration During Normal Operation

Offset calibration can be done during normal device operation if at least 32 SCLK falling edges are provided in one serial transfer frame. During the first 14 SCLKs, the device converts the sample acquired on the $\overline{CS}$ falling edge and provides data on the SDO output. The device initiates the offset calibration on the 17th SCLK falling edge and calibration completes on the 32nd SCLK falling edge. The SDO output remains low after the 14th SCLK falling edge and SDO goes to tri-state after $\overline{CS}$ goes high. If the device is provided with less than 32 SCLKs during a serial transfer frame, the OCR is not updated. Table 3 provides the timing parameters for offset calibration during normal operation.

For subsequent samples, the device adjusts the conversion results with the value stored in the OCR. The conversion result adjusted with the value stored in the OCR is provided by the device on the SDO output. Figure 37 shows the timing diagram for offset calibration during normal operation.

Table 3. Offset Calibration During Normal Operation

PARAMETER		MIN	TYP	MAX	UNIT
$f_{CLK-CAL}$	SCLK frequency for calibration for 2.25 V < AVDD < 3.6 V			16	MHz
$f_{CLK-CAL}$	SCLK frequency for calibration for 1.8 V < AVDD < 2.25 V			12	MHz
t_{CAL}	Calibration time during normal operation	15 t_{SCLK}			ns
t_{ACQ}	Acquisition time	200			ns
t_{PH_CS}	$\overline{CS}$ high time	t_{ACQ}			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to SCLK falling	15			ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	10			ns

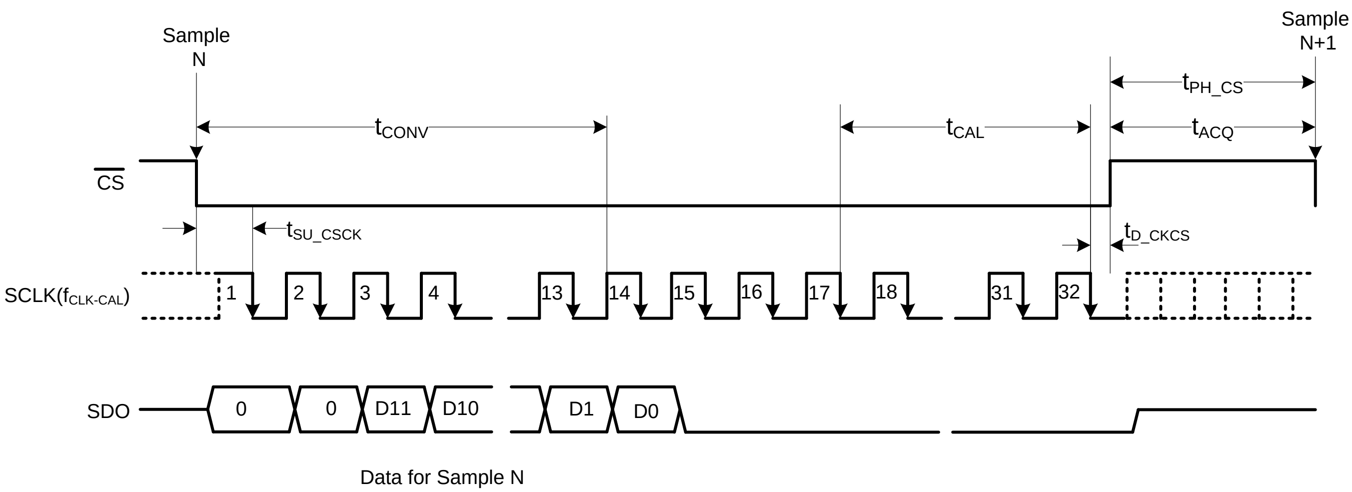


Figure 37. Offset Calibration During Normal Operation Timing Diagram

9 Applications and Implementation

9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides some application circuits designed for the ADS7042.

9.2 Typical Applications

9.2.1 Single-Supply DAQ with the ADS7042

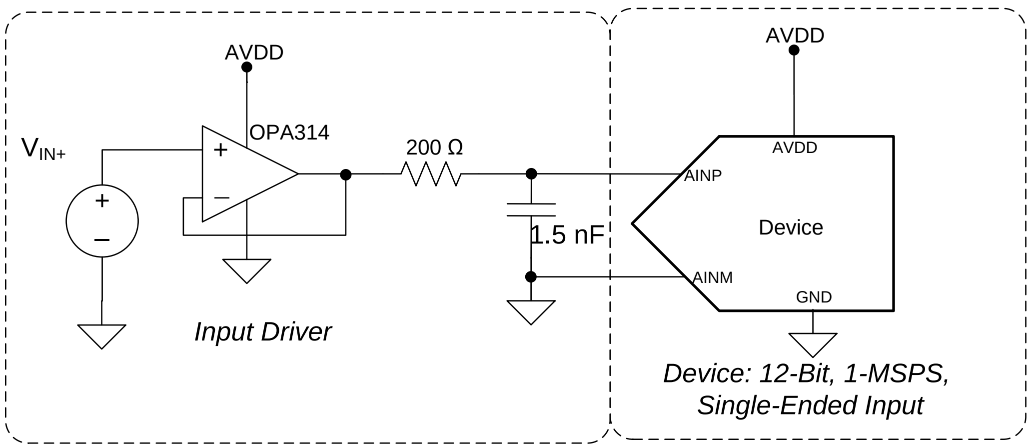


Figure 38. DAQ Circuit: Single-Supply DAQ

9.2.1.1 Design Requirements

The goal of this application is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7042 with SNR greater than 68 dB and THD less than –80 dB for input frequencies of 2.5 kHz at a throughput of 1 MSPS.

9.2.1.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and an antialiasing filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

Typical Applications (continued)

9.2.1.2.1 Antialiasing Filter

Converting analog-to-digital signals requires sampling an input signal at a rate greater than or equal to the Nyquist rate. Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. This process is called *aliasing*. Therefore, an external, antialiasing filter must be used to remove the harmonic content from the input signal before being sampled by the ADC. An antialiasing filter is designed as a low-pass RC filter, for which the 3-dB bandwidth is optimized for noise, response time, and throughput. For dc signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurately settling the signal at the ADC inputs during the small acquisition time window. Figure 39 provides the equation for determining the bandwidth of the antialiasing filter.

$$f_{-3dB} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}}$$

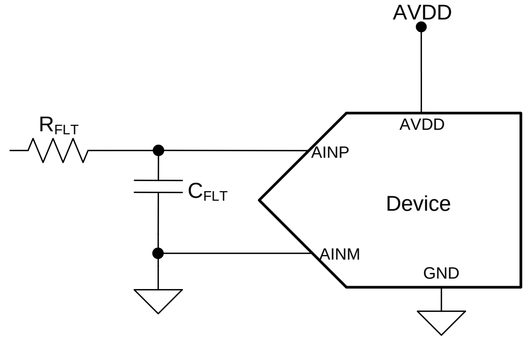


Figure 39. Antialiasing Filter

For ac signals, the filter bandwidth must be kept low to band limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor is at least 20 times the specified value of the ADC sampling capacitance. For this device, the input sampling capacitance is equal to 15 pF. Thus, the value of C_{FLT} is greater than 300 pF. Select a COG- or NPO-type capacitor because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Note that driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design.

The input amplifier bandwidth is typically much higher than the cutoff frequency of the antialiasing filter. Thus, TI strongly recommends performing a SPICE simulation to confirm that the amplifier has more than 40° phase margin with the selected filter. Simulation is critical because even with high-bandwidth amplifiers, some amplifiers can require more bandwidth than others to drive similar filters.

Typical Applications (continued)

9.2.1.2.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type and the performance goals of the data acquisition system. Some key amplifier specifications to consider while selecting an appropriate amplifier to drive the inputs of the ADC are:

- Small-signal bandwidth: Select the small-signal bandwidth of the input amplifiers to be high enough to settle the input signal in the acquisition time of the ADC. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter at the ADC inputs. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, the select the amplifier bandwidth as described in Equation 3.

$$GBW \geq 4 \times \frac{1}{2\pi \times R_{FLT} \times C_{FLT}}$$

where:

  - GBW = unity gain bandwidth (3)

- Noise: Noise contribution of the front-end amplifiers must be low enough to prevent any degradation in SNR performance of the system. As a rule of thumb, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, keep the total noise contribution from the front-end circuit below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band limited by designing a low cutoff frequency RC filter, as explained in Equation 4.

$$N_G \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e^2_{n\_RMS} \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{2\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)}$$

where:

  - V_{1/f_AMP_PP} is the peak-to-peak flicker noise in µVRMS,
  - e_{n_RMS} is the amplifier broadband noise,
  - f_{-3dB} is the –3-dB bandwidth of the RC filter, and
  - N_G is the noise gain of the front-end circuit, which is equal to 1 in the buffer configuration. (4)

- Settling time: For dc signals with fast transients that are common in a multiplexed application, the input signal must settle to the desired accuracy at the inputs of the ADC during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired accuracy. Therefore, always verify the settling behavior of the input driver with TINA™-SPICE simulations before selecting the amplifier.

The OPA314 is selected for this application for its rail-to-rail input and output swing, low-noise (14 nV/√Hz), and low-power (150 µA) performance to support a single-supply data acquisition circuit.

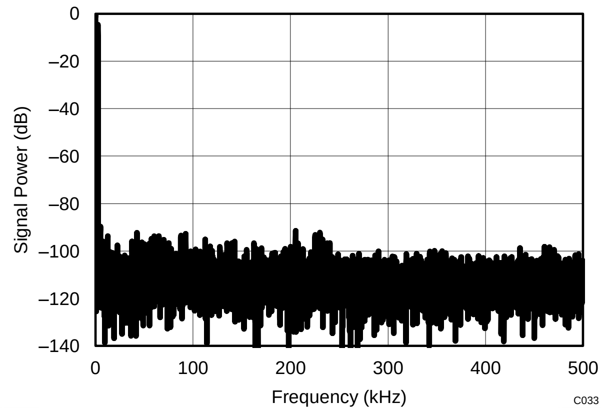
9.2.1.2.3 Reference Circuit

The analog supply voltage of the device is also used as a voltage reference for conversion. Therefore, the AVDD pins must be decoupled with a 1-µF, low-ESR ceramic capacitor close to the device pins.

Typical Applications (continued)

9.2.1.3 Application Curve

Figure 40 shows the FFT plot for the ADS7042 with a 2.5-kHz input frequency used for the circuit in Figure 38.



SNR = 69 dB THD = –80 dB SINAD = 68.6 dB
Number of samples = 32768

Figure 40. Test Results for the ADS7042 and OPA314 for a 2.5-kHz Input

Typical Applications (continued)

9.2.2 DAQ Circuit with the ADS7042 for Maximum SINAD

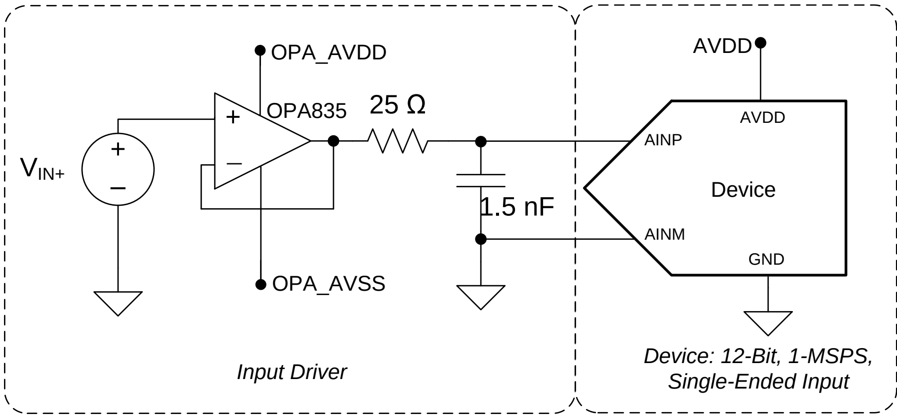


Figure 41. ADS7042 DAQ Circuit: Maximum SINAD for Input Frequencies up to 250 kHz

9.2.2.1 Design Requirements

The goal of this application is to design a data acquisition circuit based on the ADS7042 with SINAD greater than 69.5 dB for input frequencies up to 250 kHz.

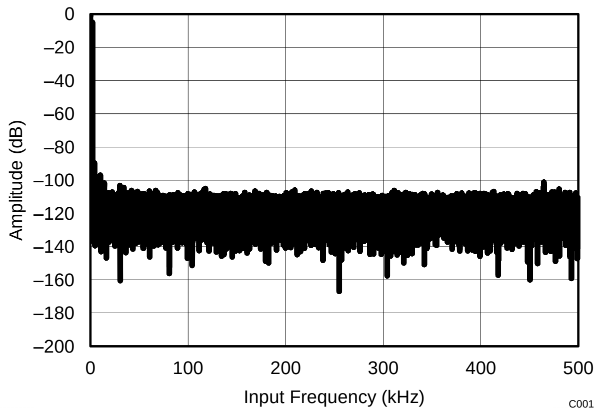
9.2.2.2 Detailed Design Procedure

To achieve a SINAD of 69.5 dB, the operational amplifier must have high bandwidth in order to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in Figure 41, the OPA835 is selected for its high bandwidth (56 MHz) and low noise (9.3 nV/$\sqrt{\text{Hz}}$).

TI Precision Designs	For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD168, *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor* (TIDU390).

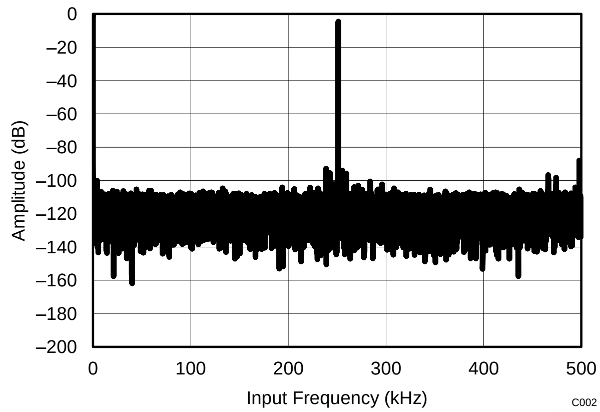
9.2.2.3 Application Curves

Figure 42 shows the FFT plot for the ADS7042 with a 2-kHz input frequency used for the circuit shown in Figure 41. Figure 43 shows the FFT plot for the ADS7042 with a 250-kHz input frequency used for the circuit shown in Figure 41.



SNR = 70.62 dB THD = –83.96 dB SINAD = 70.3 dB
Number of samples = 32768

Figure 42. Test Results for the ADS7042 and OPA835 for a 2-kHz Input



SNR = 70.22 dB THD = –81.58 dB SINAD = 69.8 dB
Number of samples = 32768

Figure 43. Test Results for the ADS7042 and OPA835 for a 250-kHz Input

9.2.3 12-Bit, 10-kSPS DAQ Circuit Optimized for DC Sensor Measurements

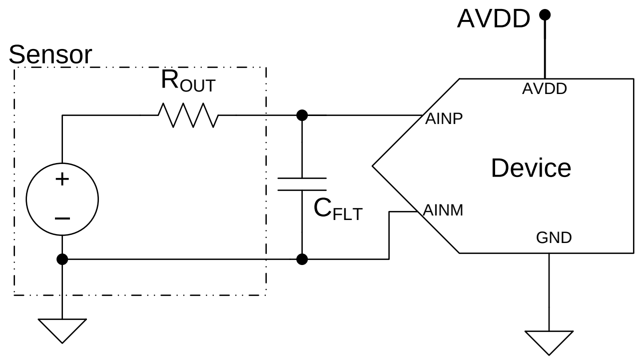


Figure 44. Interfacing the Device Directly with Sensors

In applications where the input is very slow moving and the overall system ENOB is not a critical parameter, a DAQ circuit can be designed without the input driver for the ADC . This type of a use case is of particular interest for applications in which the primary goal is to achieve the absolute lowest power possible. Typical applications that fall into this category are low-power sensor applications (such as temperature, pressure, humidity, gas, and chemical).

9.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	GOAL VALUE
Throughput	10 kSPS
SNR at 100Hz	70 dB
THD at 100Hz	75 dB
SINAD at 100 Hz	69 dB
ENOB	11
Power	10 µW

9.2.3.2 Detailed Design Procedure

The ADS7042 can be directly interfaced with sensors at lower throughputs without the need of an amplifier buffer. The analog input source drive must be capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal within the acquisition time of the SAR ADC. However, the output impedance of the sensor must be taken into account while interfacing a SAR ADC directly with sensors. Drive the analog input of the SAR ADC with a low impedance source. The input signal requires more acquisition time to settle to the desired accuracy because of the higher output impedance of the sensor. The simplified circuit for a sensor as a voltage source with output impedance (R_{OUT}) is shown in Figure 44.

The acquisition time of a SAR ADC (such as the ADS7042) can be increased by reducing throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput, or
2. Keeping the SCLK fixed at the highest permissible value (that is, 16 MHz for the device) and increasing the $\overline{\text{CS}}$ high time.

Table 5 lists the acquisition time for the above two cases for a throughput of 100 kSPS. Clearly, case 2 provides more acquisition time for the input signal to settle.

Table 5. Acquisition Time with Different SCLK Frequencies

CASE	SCLK	t_{cycle}	CONVERSION TIME (= 12.5 × t_{SCLK} + t_{SU_CSCK})	ACQUISITION TIME (= t_{cycle} – t_{conv})
1	1.6 MHz	10 µs	7.8125 µs	2.1875 µs
2	16 MHz	10 µs	0.78125 µs	9.21875 µs

TI Precision Designs	For a step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIPD168, *Three 12-Bit Data Acquisition Reference Designs Optimized for Low Power and Ultra-Small Form Factor* (TIDU390).

9.2.3.3 Application Curves

When the output impedance of the sensor increases, the time required for the input signal to settle increases and the performance of the SAR ADC starts degrading if the input signal does not settle within the acquisition time of the ADC. The performance of the SAR ADC can be improved by reducing the throughput to provide enough time for the input signal to settle. Figure 45 provides the results for ENOB achieved from the ADS7042 for case 2 at different throughputs with different input impedances at the device input.

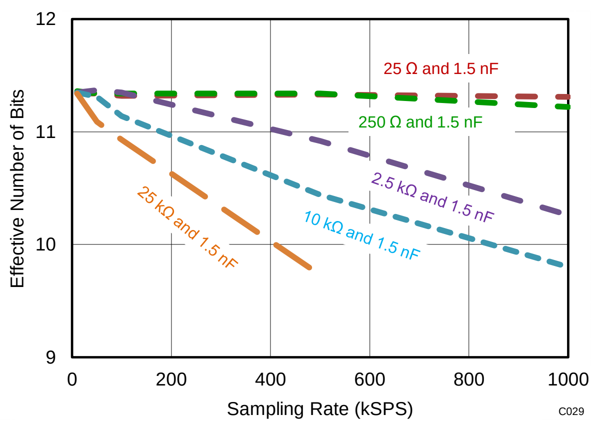


Figure 45. ENOB (Effective Number of Bits) Achieved from the ADS7042 at Different Throughputs

Table 6 shows the results and performance summary for this 12-Bit, 10-kSPS DAQ circuit application.

Table 6. Results and Performance Summary for 12-Bit, 10-kSPS DAQ Circuit for DC Sensor Measurements

DESIGN PARAMETER	GOAL VALUE	ACHIEVED RESULT
Throughput	10 kSPS	10 kSPS
SNR at 100 Hz	70 dB	70.6 dB
THD at 100 Hz	75 dB	83.5 dB
SINAD at 100 Hz	69 dB	70.4 dB
ENOB	11	11.4
Power	10 µW	7 µW

10 Power-Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The ADS7042 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. The AVDD supply also defines the full-scale input range of the device. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes. Decouple the AVDD and DVDD pins individually with 1-µF ceramic decoupling capacitors, as shown in Figure 46.

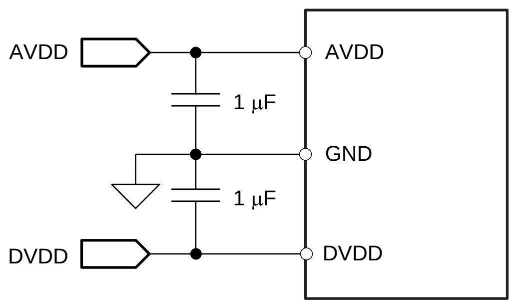


Figure 46. Power-Supply Decoupling

10.2 Estimating Digital Power Consumption

The current consumption from the DVDD supply depends on the DVDD voltage, load capacitance on the SDO line, and the output code. The load capacitance on the SDO line is charged by the current from the SDO pin on every rising edge of the data output and is discharged on every falling edge of the data output. The current consumed by the device from the DVDD supply can be calculated by Equation 5:

$$I_{DVDD} = C \times V \times f$$

where:

- C = Load capacitance on the SDO line,
- V = DVDD supply voltage, and
- f = Number of transitions on the SDO output. (5)

The number of transitions on the SDO output depends on the output code, and thus changes with the analog input. The maximum value of f occurs when data output on the SDO change on every SCLK. SDO changing on every SCLK results in an output code of AAAh or 555h. For an output code of AAAh or 555h at a 1-MSPS throughput, the frequency of transitions on the SDO output is 6 MHz.

For the current consumption to remain at the lowest possible value, keep the DVDD supply at the lowest permissible value and keep the capacitance on the SDO line as low as possible.

10.3 Optimizing Power Consumed by the Device

- Keep the analog supply voltage (AVDD) as close as possible to the analog input voltage. Set AVDD to be greater than or equal to the analog input voltage of the device.
- Keep the digital supply voltage (DVDD) at the lowest permissible value.
- Reduce the load capacitance on the SDO output.
- Run the device at the optimum throughput. Power consumption reduces with throughput.

11 Layout

11.1 Layout Guidelines

Figure 47 shows a board layout example for the ADS7042. Use a ground plane underneath the device and partition the PCB into analog and digital sections. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources. In Figure 47, the analog input and reference signals are routed on the top and left side of the device and the digital connections are routed on the bottom and right side of the device.

The power sources to the device must be clean and well-bypassed. Use 1-μF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths. The AVDD supply voltage for the ADS7042 also functions as a reference for the device. Place the decoupling capacitor (C_{REF}) for AVDD close to the device AVDD and GND pins and connect C_{REF} to the device pins with thick copper tracks, as shown in Figure 47.

The fly-wheel RC filters are placed close to the device. Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG (NPO) ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

11.2 Layout Example

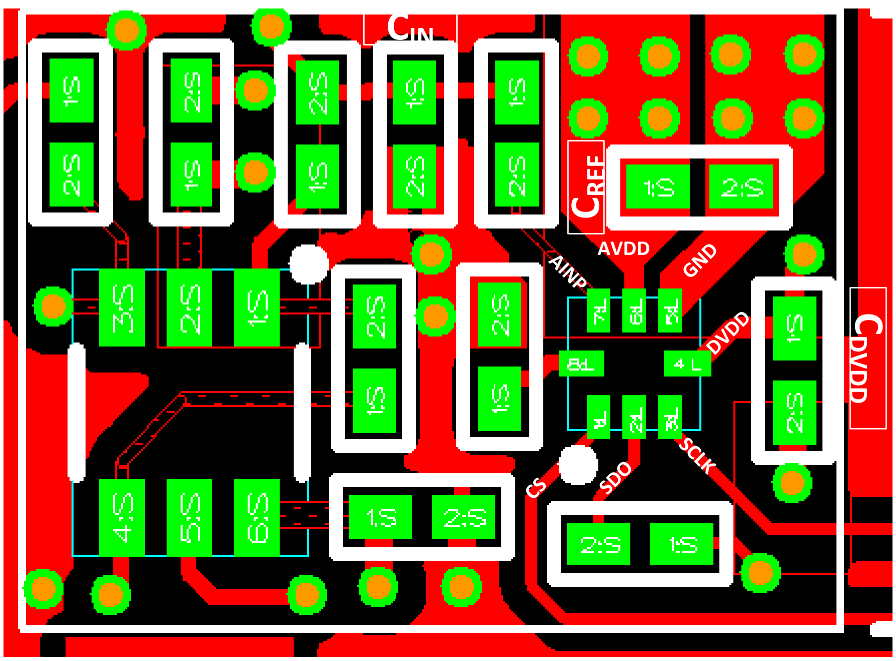


Figure 47. Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- OPA314 Data Sheet, SBOS563
- OPA835 Data Sheet, SLOS713
- TPS79101 Data Sheet, SLVS325
- TIPD168 Reference Guide, TIDU390

12.2 Trademarks

TINA is a trademark of Texas Instruments, Inc.
SPI is a trademark of Motorola.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7042IDCUR	PREVIEW	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042	
ADS7042IDCUT	PREVIEW	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	7042	
ADS7042IRUGR	PREVIEW	X2QFN	RUG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	FV	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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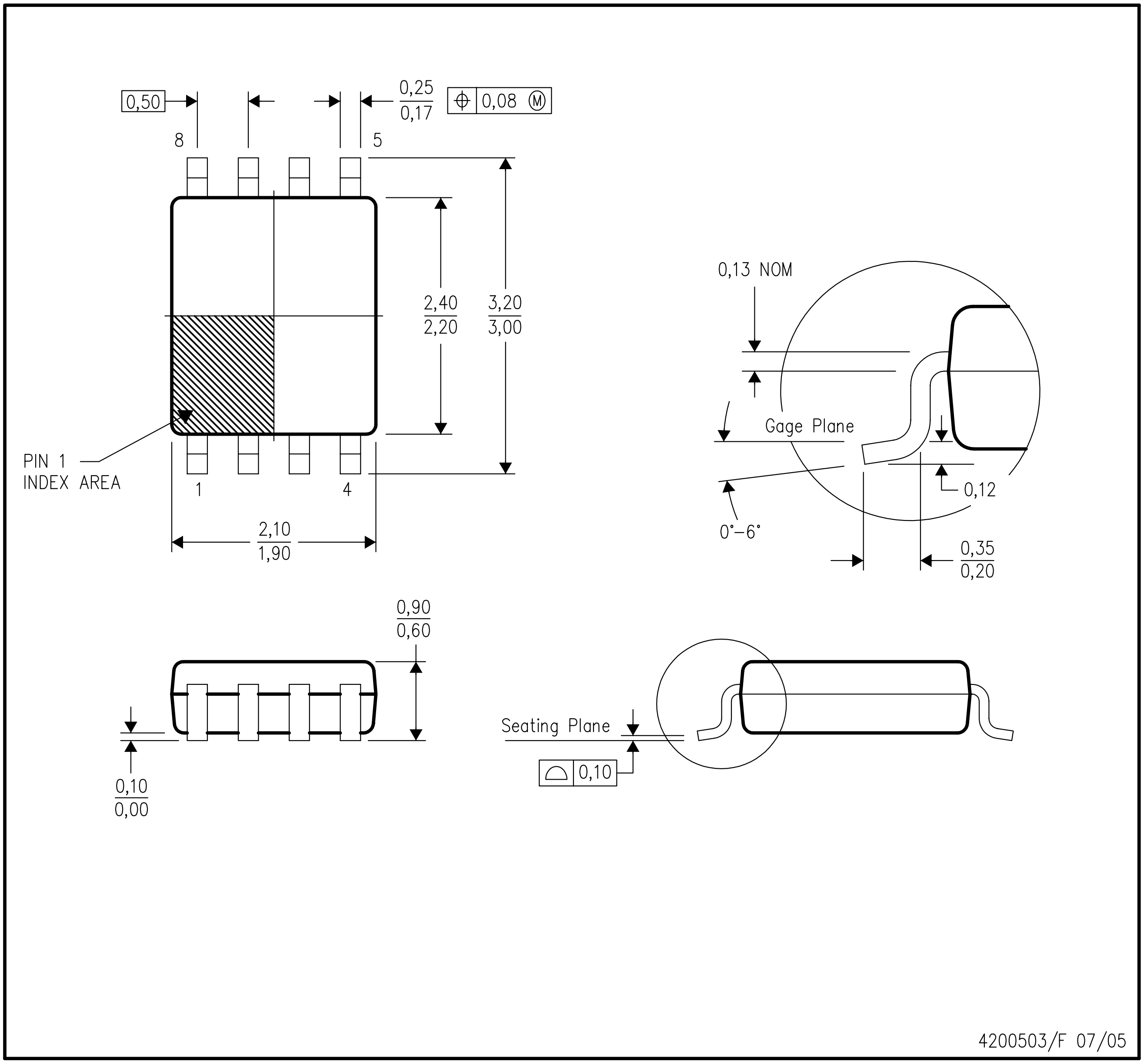
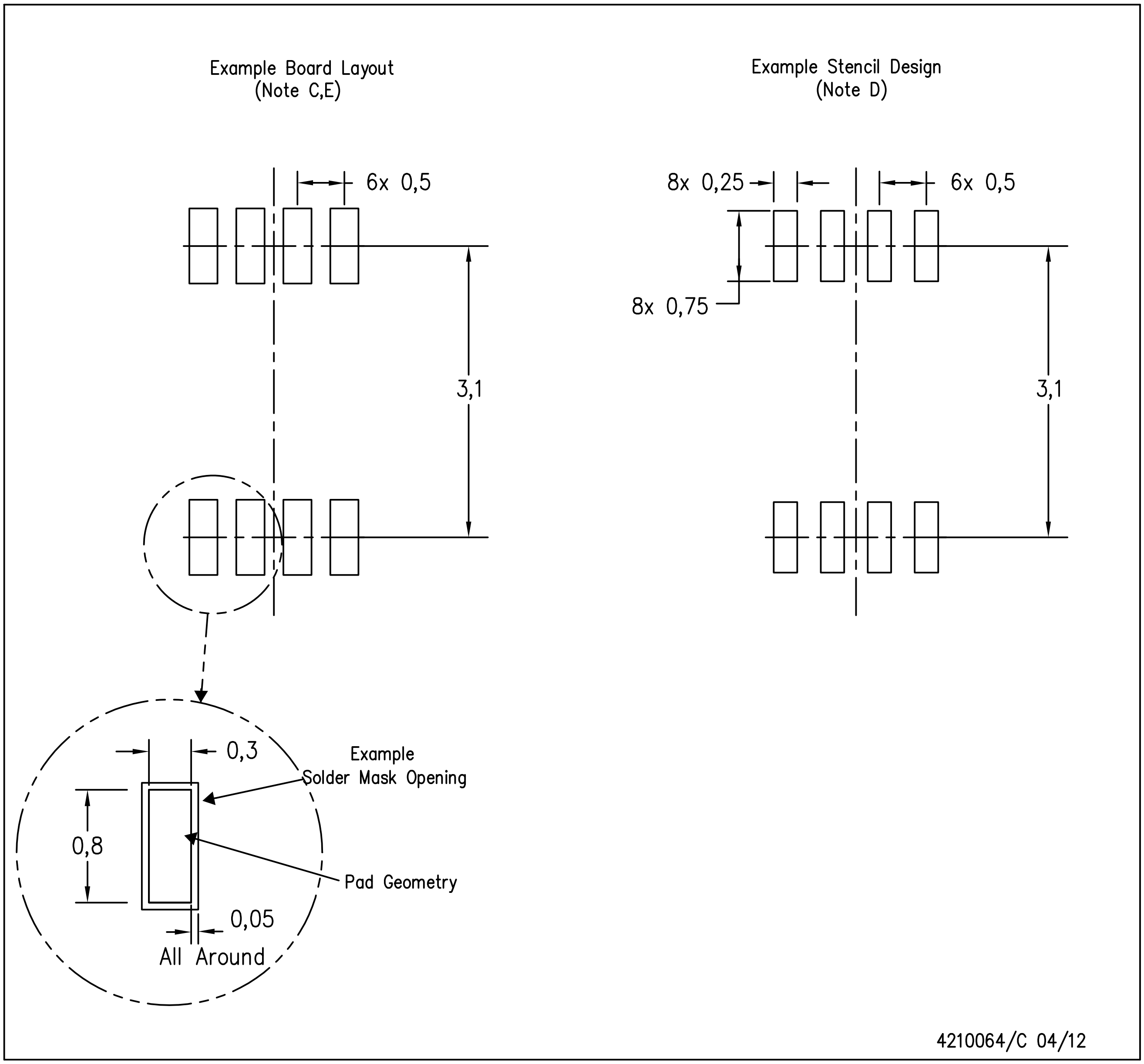
DCU (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE (DIE DOWN)



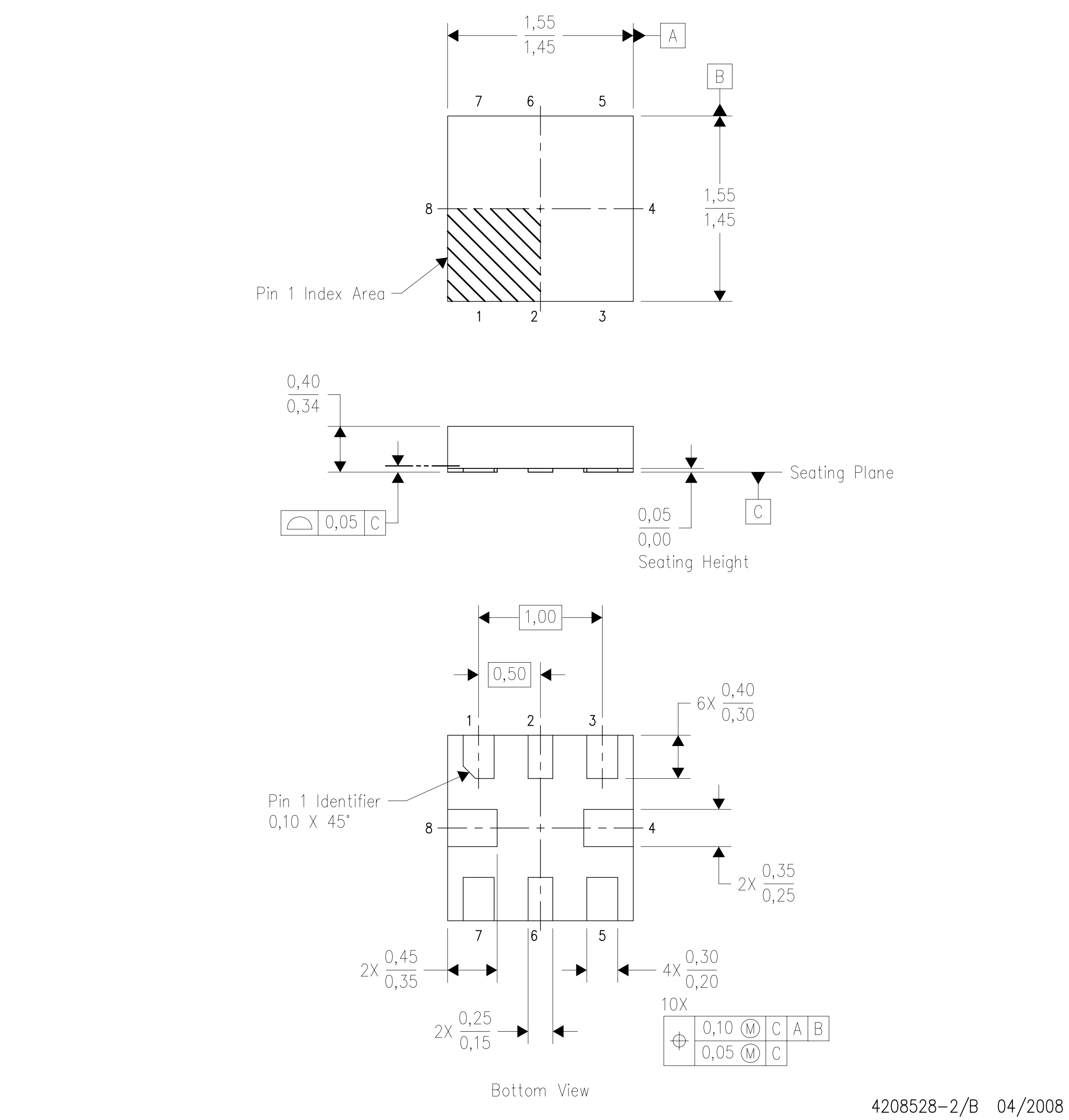
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–187 variation CA.

DCU (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE (DIE DOWN)



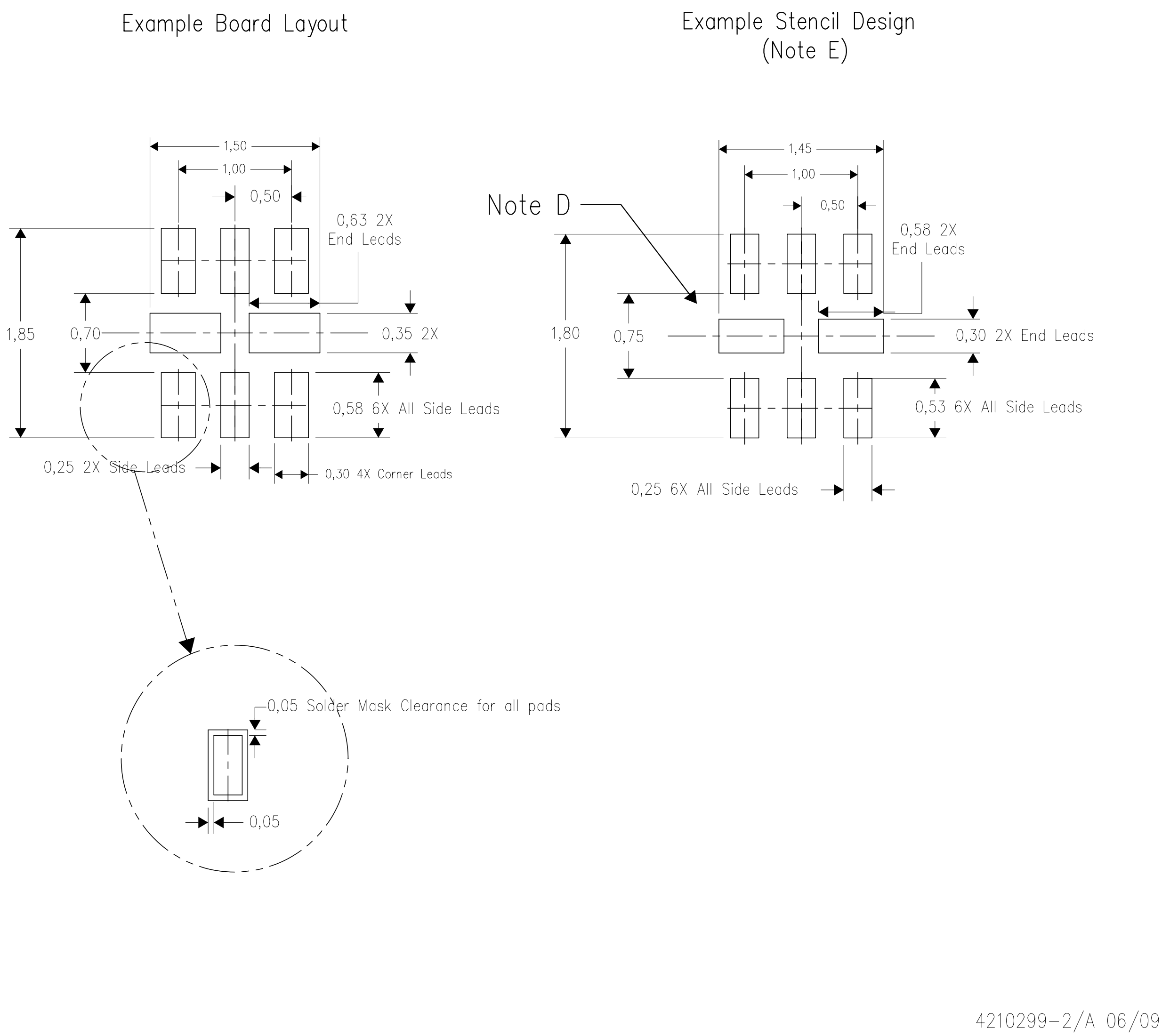
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (S–PQFP–N8) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2ECD.

RUG (R–PQFP–N8)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

IMPORTANT NOTICE

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
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