

FEATURES

Dual 10-bit, 40 MSPS, 65 MSPS, 80 MSPS, and 105 MSPS ADC
Low power: 275 mW at 105 MSPS per channel
On-chip reference and track-and-hold
300 MHz analog bandwidth each channel
SNR = 57 dB @ 41 MHz, Encode = 80 MSPS
1 V p-p or 2 V p-p analog input range each channel
3.0 V single-supply operation (2.7 V to 3.6 V)
Power-down mode for single-channel operation
Twos complement or offset binary output mode
Output data alignment mode
Pin compatible with 8-bit AD9288
-75 dBc crosstalk between channels

APPLICATIONS

Battery-powered instruments
Hand-held scopemeters
Low cost digital oscilloscopes
I and Q communications
Ultrasound equipment

GENERAL DESCRIPTION

The AD9218 is a dual 10-bit monolithic sampling analog-to-digital converter with on-chip track-and-hold circuits. The product is low cost, uses low power, is small and is easy to use. The AD9218 operates at a 105 MSPS conversion rate with outstanding dynamic performance over its full operating range. Each channel can be operated independently.

The ADC requires only a single 3.0 V (2.7 V to 3.6 V) power supply and a clock for full operation. No external reference or driver components are required for many applications. The digital outputs are TTL/CMOS compatible and a separate output power supply pin supports interfacing with 3.3 V or 2.5 V logic.

The clock input is TTL/CMOS compatible and the 10-bit digital outputs can be operated from 3.0 V (2.5 V to 3.6 V) supplies. User-selectable options offer a combination of power-down modes, digital data formats, and digital data timing schemes. In power-down mode, the digital outputs are driven to a high impedance state.

Rev. B

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FUNCTIONAL BLOCK DIAGRAM

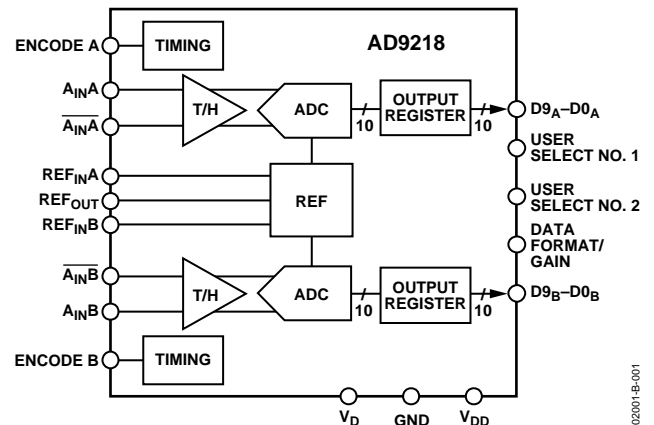


Figure 1.

PRODUCT HIGHLIGHTS

- Low power.**
 Just 275 mW power dissipation per channel at 105 MSPS. Other speed grades proportionally scaled down while maintaining high ac performance.
- Pin compatibility upgrade.**
 Allows easy migration from 8-bit to 10-bit devices. Pin compatible with the 8-bit AD9288 dual ADC.
- Easy to use.**
 On-chip reference and user controls provide flexibility in system design.
- High performance.**
 Maintains 54 dB SNR at 105 MSPS with a Nyquist input.
- Channel crosstalk.**
 Very low at -75 dBc.
- Fabricated on an advanced CMOS process.**
 Available in a 48-lead low profile quad flat package (7 mm × 7 mm LQFP) specified over the industrial temperature range (-40°C to +85°C).

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REVISION HISTORY

Revision B:

1/04—Data sheet changed from REV. A. to REV. B

| | |
|---|-----------|
| Updated format..... | Universal |
| Changes to General Description | 1 |
| Changes to DC Specifications..... | 3 |
| Changes to Switching Specifications..... | 6 |
| Added AD9218/AD9288 Customer PCB BOM section..... | 20 |
| Added Evaluation Board section..... | 21 |

Revision A:

7/03—Data Sheet changed from REV. 0 to REV. A.

| | |
|--------------------------------------|----|
| Updated Ordering Guide..... | 6 |
| Changes to Terminology section | 8 |
| Changes to Figure 17b..... | 19 |
| Updated Outline Dimensions | 24 |

SPECIFICATIONS

DC SPECIFICATIONS

Table 1. $V_{DD} = 3.0\text{ V}$, $V_D = 3.0\text{ V}$; external reference, unless otherwise noted.

| Parameter | Temp | Test Level | AD9218BST-40/-65 | | | AD9218BST-80/-105 | | | Unit |
|--|------|------------|------------------------|-------------------|---------|------------------------|-------------------|-----------|------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| RESOLUTION | | | 10 | | | 10 | | | Bits |
| ACCURACY | | | Guaranteed, not tested | | | Guaranteed, not tested | | | |
| No Missing Codes ¹ | Full | VI | Guaranteed, not tested | | | Guaranteed, not tested | | | |
| Offset Error ² | 25°C | I | -18 | 2 | 18 | -18 | 2 | 18 | LSB |
| Gain Error ² | 25°C | I | -2 | 3 | 8 | -2 | 3.5 | 8 | % FS |
| Differential Nonlinearity (DNL) | 25°C | I | -1 | $\pm 0.3/\pm 0.6$ | 1/1.3 | -1 | $\pm 0.5/\pm 0.8$ | 1.2/1.7 | LSB |
| Integral Nonlinearity (INL) | Full | VI | | ± 0.8 | | | $\pm 0.6/\pm 0.9$ | | LSB |
| | 25°C | I | -1/-1.6 | $\pm 0.3/\pm 1$ | 1/1.6 | -1.35/-2.7 | $\pm 0.75/\pm 2$ | +1.35/2.7 | LSB |
| | Full | VI | | ± 1 | | | $\pm 1/\pm 2.3$ | | LSB |
| TEMPERATURE DRIFT | | | | | | | | | |
| Offset Error | Full | V | | 10 | | | 4 | | ppm/°C |
| Gain Error ² | Full | V | | 80 | | | 100 | | ppm/°C |
| Reference | Full | V | | 40 | | | 40 | | ppm/°C |
| REFERENCE | | | | | | | | | |
| Internal Reference Voltage (REFOUT) | 25°C | I | 1.18 | 1.24 | 1.28 | 1.18 | 1.24 | 1.28 | V |
| Input Resistance (REFIN A, B) | Full | VI | 9 | 11 | 13 | 9 | 11 | 13 | k Ω |
| ANALOG INPUTS | | | | | | | | | |
| Differential Input Voltage Range (A_{IN} , $\overline{A_{IN}}$) ³ | Full | V | | 1 or 2 | | | 1 | | V |
| Common-Mode Voltage ³ | Full | V | | $V_D/3$ | | | $V_D/3$ | | V |
| Input Resistance | Full | VI | 8 | 10 | 14 | 8 | 10 | 14 | k Ω |
| Input Capacitance | 25°C | V | | 3 | | | 3 | | pF |
| POWER SUPPLY | | | | | | | | | |
| V_D | Full | IV | 2.7 | 3 | 3.6 | 2.7 | 3 | 3.6 | V |
| V_{DD} | Full | IV | 2.7 | 3 | 3.6 | 2.7 | 3 | 3.6 | V |
| Supply Currents | | | | | | | | | |
| I_{V_D} ($V_D = 3.0\text{ V}$) ⁴ | Full | VI | | 108/117 | 113/122 | | 172/183 | 175/188 | mA |
| $I_{V_{DD}}$ ($V_{DD} = 3.0\text{ V}$) ⁴ | 25°C | V | | 7/11 | | | 13/17 | | mA |
| Power Dissipation DC ⁵ | Full | VI | | 325/350 | 340/365 | | 515/550 | 525/565 | mW |
| I_{V_D} Power-Down Current ⁶ | Full | VI | | 20 | | | 22 | | mA |
| Power Supply Rejection Ratio | 25°C | I | | ± 1 | | | ± 1 | | mV/V |

¹ No missing codes across industrial temperature range guaranteed for 40 MSPS, 65 MSPS, and 80 MSPS grades. No missing codes at room temperature guaranteed for 105 MSPS grade.

² Gain error and gain temperature coefficients are based on the ADC only (with a fixed 1.25 V external reference) -65 Grade in 2 V p-p range, -40, -85, -105 grades in 1 V p-p range.

³ ($A_{IN} - \overline{A_{IN}}$) = $\pm 0.5\text{ V}$ in 1 V range (full scale), ($A_{IN} - \overline{A_{IN}}$) = $\pm 1\text{ V}$ in 2 V range (full scale). The analog inputs will self-bias to $V_D/3$. This common mode voltage can be overdriven externally by a low impedance source by $\pm 300\text{ mV}$ (differential drive, gain=1) or $\pm 150\text{ mV}$ (differential drive, gain= 2).

⁴ AC power dissipation measured with rated encode and a 10.3 MHz analog input @ 0.5 dBFS, $C_{LOAD} = 5\text{ pF}$.

⁵ DC power dissipation measured with rated encode and a dc analog input (outputs static, $I_{V_{DD}} = 0$).

⁶ In power-down state $I_{V_{DD}} = \pm 10\text{ }\mu\text{A}$ typical (all grades).

AD9218

DIGITAL SPECIFICATIONS

Table 2. $V_{DD} = 3.0\text{ V}$, $V_D = 3.0\text{ V}$; external reference, unless otherwise noted.

| Parameter | Temp | Test Level | AD9218BST-40/-65 | | | AD9218BST-80/-105 | | | Unit |
|---|------|------------|----------------------------------|---------|------|----------------------------------|---------|------|---------------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| DIGITAL INPUTS | | | | | | | | | |
| Encode Input Common Mode | Full | V | | $V_D/2$ | | | $V_D/2$ | | V |
| Encode 1 Voltage | Full | VI | 2 | | | 2 | | | V |
| Encode 0 Voltage | Full | VI | | | 0.8 | | | 0.8 | V |
| Encode Input Resistance | Full | VI | 1.8 | 2.0 | 2.3 | 1.8 | 2.0 | 2.3 | k Ω |
| Logic 1 Voltage—S1, S2, DFS | Full | VI | 2 | | | 2 | | | V |
| Logic 0 Voltage—S1, S2, DFS | Full | VI | | | 0.8 | | | 0.8 | V |
| Logic 1 Current—S1 | Full | VI | -50 | ± 0 | 50 | -50 | ± 0 | 50 | μA |
| Logic 0 Current—S1 | Full | VI | -400 | -230 | -50 | -400 | -230 | -50 | μA |
| Logic 1 Current—S2 | Full | VI | 50 | 230 | 400 | 50 | 230 | 400 | μA |
| Logic 0 Current—S2 | Full | VI | -50 | ± 0 | 50 | -50 | ± 0 | 50 | μA |
| Logic 1 Current—DFS | Full | VI | 30 | 100 | 200 | 30 | 100 | 200 | μA |
| Logic 0 Current—DFS | Full | VI | -400 | -230 | -50 | -400 | -230 | -50 | μA |
| Input Capacitance—S1, S2, Encode Inputs | 25°C | V | | 2 | | | 2 | | pF |
| Input Capacitance DFS | 25°C | V | | 4.5 | | | 4.5 | | pF |
| DIGITAL OUTPUTS | | | | | | | | | |
| Logic 1 Voltage | Full | VI | 2.45 | | | 2.45 | | | V |
| Logic 0 Voltage | Full | VI | | | 0.05 | | | 0.05 | V |
| Output Coding | | | Twos Complement or Offset Binary | | | Twos Complement or Offset Binary | | | |

AC SPECIFICATIONS

Table 3. $V_{DD} = 3.0\text{ V}$, $V_D = 3.0\text{ V}$; external reference, unless otherwise noted.

| Parameter | Temp | Test Level | AD9218BST-40/-65 | | | AD9218BST-80/-105 | | | Unit |
|---|------|------------|------------------|---------|-----|-------------------|---------|------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| DYNAMIC PERFORMANCE ¹ | | | | | | | | | |
| Signal-to-Noise Ratio (SNR) (Without Harmonics) | | | | | | | | | |
| $f_{IN} = 10.3\text{ MHz}$ | 25°C | I | 58/55 | 59/57 | | 57/53 | 58/55 | dB | |
| $f_{IN} = \text{Nyquist}^2$ | 25°C | I | -/54 | 59/56 | | 55/52 | 57/54 | dB | |
| Signal-to-Noise Ratio (SINAD) (With Harmonics) | | | | | | | | | |
| $f_{IN} = 10.3\text{ MHz}$ | 25°C | I | 58/54 | 59/56 | | 56/52 | 58/53 | dB | |
| $f_{IN} = \text{Nyquist}^2$ | 25°C | I | -/53 | 59/55 | | 55/51 | 57/53 | dB | |
| Effective Number of Bits | | | | | | | | | |
| $f_{IN} = 10.3\text{ MHz}$ | 25°C | I | 9.4/8.8 | 9.6/9.1 | | 9.1/8.4 | 9.4/8.6 | Bits | |
| $f_{IN} = \text{Nyquist}^2$ | 25°C | I | -/8.6 | 9.6/8.9 | | 9/8.3 | 9.3/8.6 | Bits | |
| Second Harmonic Distortion | | | | | | | | | |
| $f_{IN} = 10.3\text{ MHz}$ | 25°C | I | -72/-66 | -89/-77 | | -69/-60 | -77/-68 | dBc | |
| $f_{IN} = \text{Nyquist}^2$ | 25°C | I | -/-63 | -89/-72 | | -65/-57 | -76/-66 | dBc | |
| Third Harmonic Distortion | | | | | | | | | |
| $f_{IN} = 10.3\text{ MHz}$ | 25°C | I | -68/-62 | -79/-68 | | -62/-57 | -71/-63 | dBc | |
| $f_{IN} = \text{Nyquist}^2$ | 25°C | I | -/-60 | -78/-64 | | -63/-57 | -73/-69 | dBc | |
| Spurious Free Dynamic Range SFDR | | | | | | | | | |
| $f_{IN} = 10.3\text{ MHz}$ | 25°C | I | -68/-62 | -79/-67 | | -62/-57 | -69/-62 | dBc | |
| $f_{IN} = \text{Nyquist}^2$ | 25°C | I | -/-60 | -78/-64 | | -63/-57 | -70/-63 | dBc | |
| Two-Tone Intermod Distortion (IMD) | | | | | | | | | |
| $f_{IN1} = 10\text{ MHz}$, $f_{IN2} = 11\text{ MHz}$ at -7 dBFS | 25°C | V | | -74/-73 | | | | dBc | |
| $f_{IN1} = 30\text{ MHz}$, $f_{IN2} = 31\text{ MHz}$ at -7 dBFS | 25°C | V | | -73/-73 | | | -77/-67 | dBc | |
| Analog Bandwidth, Full Power | 25°C | V | | 300 | | | 300 | MHz | |
| Crosstalk | 25°C | V | | -75 | | | -75 | dBc | |

¹ AC specifications based on an analog input voltage of -0.5 dBFS at 10.3 MHz unless otherwise noted. AC specifications for -40, -80, -105 grades are tested in 1 V p-p range and driven differentially. AC specifications for -65 grade are tested in 2 V p-p range and driven differentially.

² The -65, -80, and -105 grades are tested close to Nyquist for that grade: 31 MHz, 39 MHz, and 51 MHz for the -65, -80, and -105 grades, respectively.

AD9218

SWITCHING SPECIFICATIONS

Table 4. $V_{DD} = 3.0\text{ V}$, $V_D = 3.0\text{ V}$; external reference, unless otherwise noted.

| Parameter | Temp | Test Level | AD9218BST-40/-65 | | | AD9218BST-80/-105 | | | Unit |
|--|------|------------|------------------|-----|-----|-------------------|-----|-----|--------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| ENCODE INPUT PARAMETERS | | | | | | | | | |
| Maximum Encode Rate | Full | VI | 40/65 | | | 80/105 | | | MSPS |
| Minimum Encode Rate | Full | IV | | | | 20/20 | | | MSPS |
| Encode Pulsewidth High (t_{EH}) | Full | IV | 7/6 | | | 5/3.8 | | | ns |
| Encode Pulsewidth Low (t_{EL}) | Full | IV | 7/6 | | | 5/3.8 | | | ns |
| Aperture Delay (t_A) | 25°C | V | 2 | | | 2 | | | ns |
| Aperture Uncertainty (Jitter) | 25°C | V | 3 | | | 3 | | | ps rms |
| DIGITAL OUTPUT PARAMETERS | | | | | | | | | |
| Output Valid Time (t_V) ¹ | Full | VI | 2.5 | | | 2.5 | | | ns |
| Output Propagation Delay (t_{PD}) ¹ | Full | VI | 4.5 | | | 7 | | | ns |
| Output Rise Time (t_R) | 25°C | V | 1 | | | 1.0 | | | ns |
| Output Fall Time (t_F) | 25°C | V | 1.2 | | | 1.2 | | | ns |
| Out of Range Recovery Time | 25°C | V | 5 | | | 5 | | | ns |
| Transient Response Time | 25°C | V | 5 | | | 5 | | | ns |
| Recovery Time from Power Down | 25°C | V | 10 | | | 10 | | | Cycles |
| Pipeline Delay | Full | IV | 5 | | | 5 | | | Cycles |

¹ t_V and t_{PD} are measured from the 1.5 level of the ENCODE input to the 50%/50% levels of the digital outputs swing. The digital output load during test is not to exceed an ac load of 5 pF or a dc current of $\pm 40\ \mu\text{A}$. Rise and fall times measured from 10% to 90%.

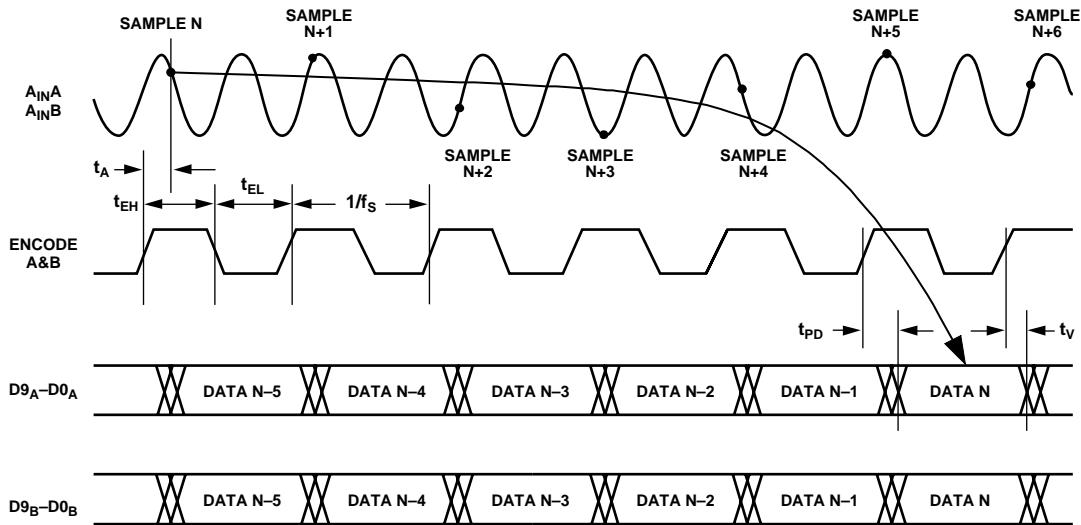
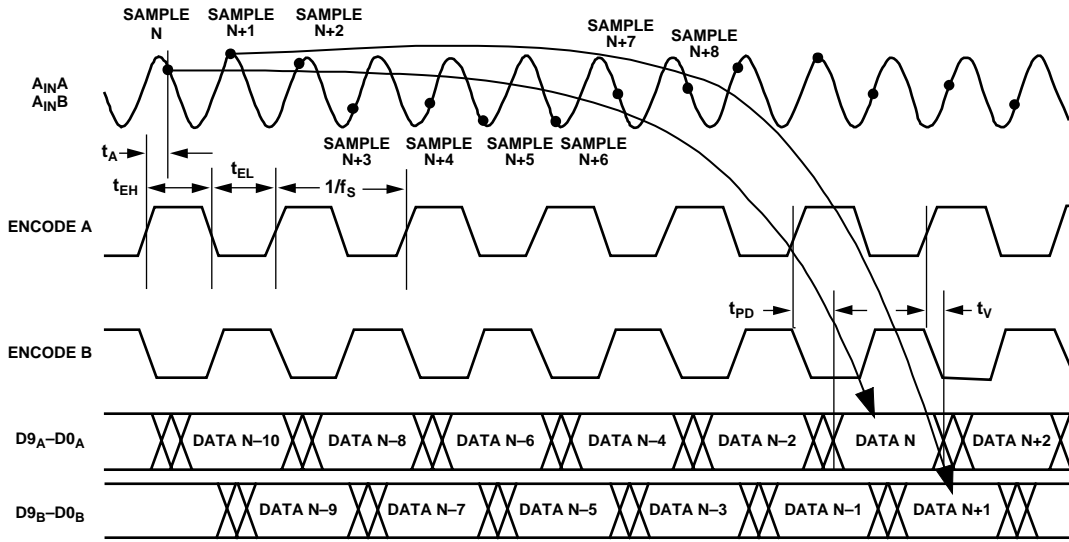


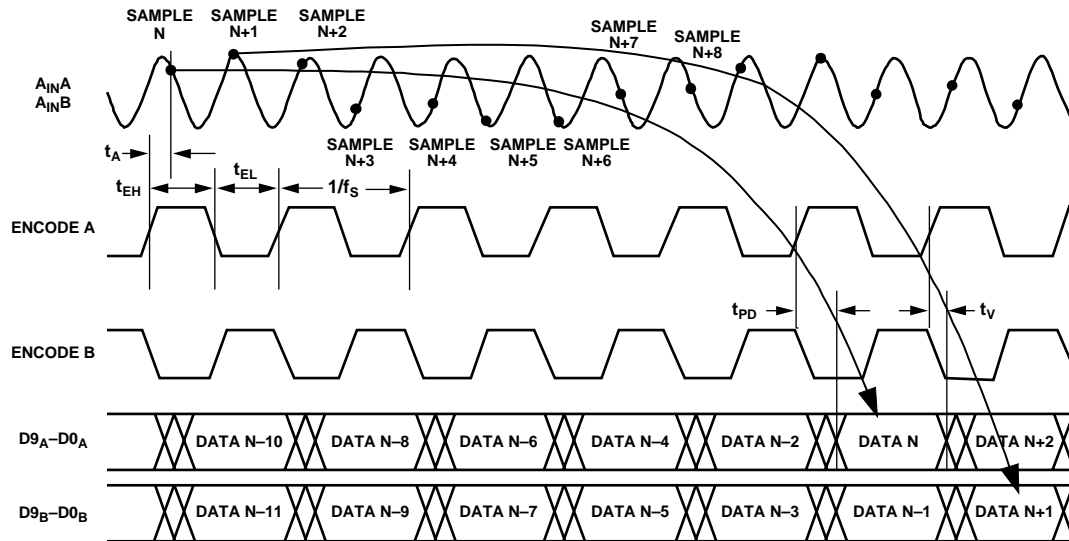
Figure 2. Normal Operation, Same Clock ($S1 = 1$, $S2 = 0$) Channel Timing

02001-B-002



02001-B-003

Figure 3. Normal Operation with Two Clock Sources (S1 = 1, S2 = 0) Channel Timing



02001-B-004

Figure 4. Data Align with Two Clock Sources (S1 = 1, S2 = 1) Channel Timing

ABSOLUTE MAXIMUM RATINGS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 5. Stress Ratings

| Parameter | Rating |
|--|-----------------------------------|
| V _D , V _{DD} | 4 V |
| Analog inputs | -0.5 V to V _D + 0.5 V |
| Digital inputs | -0.5 V to V _{DD} + 0.5 V |
| REF _{IN} inputs | -0.5 V to V _D + 0.5 V |
| Digital output current | 20 mA |
| Operating temperature | -55°C to +125°C |
| Storage temperature | -65°C to +150°C |
| Maximum junction temperature | 150°C |
| Maximum case temperature | 150°C |
| θ _A (measured on a 4-layer board with solid ground plane) | 57°C/W |

Table 6. Test Levels

| Test Level | Description |
|------------|---|
| I | 100% production tested. |
| II | 100% production tested at 25°C and sample tested at specified temperatures. |
| III | Sample tested only. |
| IV | Parameter is guaranteed by design and characterization testing. |
| V | Parameter is a typical value only. |
| VI | 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range. 100% production tested at temperature extremes for military devices. |

Table 7. User Select Modes

| S1 | S2 | Power-Down and Data Alignment Settings |
|----|----|---|
| 0 | 0 | Power down both channel A and B. |
| 0 | 1 | Power down channel B only. |
| 1 | 0 | Normal operation (data align disabled). |
| 1 | 1 | Data align enabled (data from both channels available on rising edge of Clock A. Channel B data is delayed by a 1/2 clock cycle.) |

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

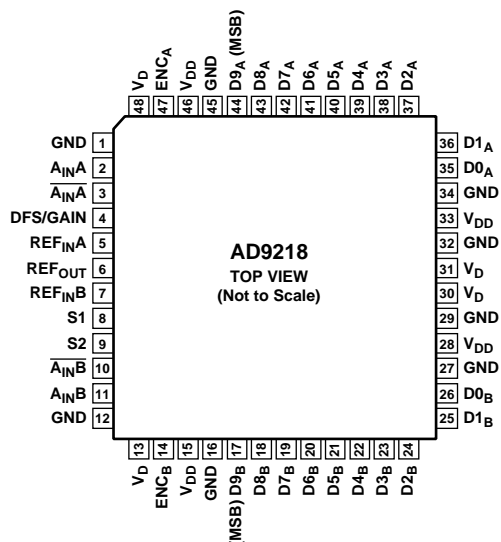


Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

| Pin Number | Mnemonic | Description |
|-------------------------------|----------------------------------|--|
| 1, 12, 16, 27, 29, 32, 34, 45 | GND | Ground. |
| 2 | A _{IN} A | Analog Input for Channel A. |
| 3 | $\overline{A}_{IN}A$ | Analog Input for Channel A (complementary). |
| 4 | DFS/GAIN | Data Format Select and Analog Input Gain Mode. Low = offset binary output available, 1 V p-p supported; high = twos complement output available, 1 V p-p supported; floating = offset binary output available, 2 V p-p supported; set to V _{REF} = twos complement output available, 2 V p-p supported. |
| 5 | REF _{IN} A | Reference Voltage Input for Channel A. |
| 6 | REF _{OUT} | Internal Reference Voltage. |
| 7 | REF _{IN} B | Reference Voltage Input for Channel B. |
| 8 | S1 | User Select No. 1. Refer to Table 7. |
| 9 | S2 | User Select No. 2. Refer to Table 7. |
| 10 | $\overline{A}_{IN}B$ | Analog Input for Channel B (complementary). |
| 11 | A _{IN} B | Analog Input for Channel B. |
| 13, 30, 31, 48 | V _D | Analog Supply (3 V). |
| 14 | ENC _B | Clock Input for Channel B. |
| 15, 28, 33, 46 | V _{DD} | Digital Supply (2.5 V to 3.6 V). |
| 17–26 | D9 _B –D0 _B | Digital Output for Channel B (D9 _B = MSB). |
| 35–44 | D0 _A –D9 _A | Digital Output for Channel A (D9 _A = MSB). |
| 47 | ENC _A | Clock Input for Channel A. |

TERMINOLOGY

Analog Bandwidth

The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay

The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

Crosstalk

Coupling onto one channel being driven by a low level signal (–40 dBFS) when the adjacent interfering channel is driven by a full-scale signal.

Differential Analog Input Resistance, Differential Analog Input Capacitance, Differential Analog Input Impedance

The real and complex impedances measured at each analog input port. The resistance is measured statically and the capacitance and differential input impedances are measured with a network analyzer.

Differential Analog Input Voltage Range

The peak-to-peak differential voltage that must be applied to the converter to generate a full-scale response. Peak differential voltage is computed by observing the voltage on a single pin and subtracting the voltage from the other pin, which is 180 degrees out of phase. Peak-to-peak differential is computed by rotating the input phase 180 degrees and again taking the peak measurement. The difference is then computed between both peak measurements.

Differential Nonlinearity

The deviation of any code width from an ideal 1 LSB step.

Effective Number of Bits (ENOB)

The effective number of bits is calculated from the measured SNR based on the equation

$$ENOB = \frac{SNR_{MEASURED} - 1.76 \text{ dB}}{6.02}$$

ENCODE Pulse Width/Duty Cycle

Pulse width high is the minimum amount of time that the ENCODE pulse should be left in Logic 1 state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. See timing implications of changing t_{ENCH} in text. At a given clock rate, these specifications define an acceptable ENCODE duty cycle.

Full-Scale Input Power

Expressed in dbm. Computed using the following equation:

$$Power_{Full-Scale} = 10 \log \left(\frac{V_{Full-Scale \text{ rms}}^2}{Z_{INPUT} \cdot 0.001} \right)$$

Gain Error

Gain error is the difference between the measured and ideal full-scale input voltage range of the ADC.

Harmonic Distortion, Second

The ratio of the rms signal amplitude to the rms value of the second harmonic component, reported in dBc.

Harmonic Distortion, Third

The ratio of the rms signal amplitude to the rms value of the third harmonic component, reported in dBc.

Integral Nonlinearity

The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a “best straight line” determined by a least-square curve fit.

Minimum Conversion Rate

The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate

The encode rate at which parametric testing is performed.

Output Propagation Delay

The delay between the 50% level crossing of ENCODE A or ENCODE B and the 50% level crossing of the respective channel's output data bit.

Noise (for Any Range within the ADC)

$$V_{NOISE} = \sqrt{Z \times 0.001 \times 10 \left(\frac{FS_{dBm} - SNR_{dBc} - Signal_{dBFS}}{10} \right)}$$

where Z is the input impedance, FS is the full scale of the device for the frequency in question, SNR is the value for the particular input level, and $Signal$ is the signal level within the ADC reported in dB below full scale. This value includes both thermal and quantization noise.

Power Supply Rejection Ratio

The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)

The ratio of the rms signal amplitude (set 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)

The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range (SFDR)

The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (that is, degrades as signal level is lowered) or dBFS (always related back to converter full scale).

Two-Tone Intermodulation Distortion Rejection

The ratio of the rms value of either input tone to the rms value of the worst third-order intermodulation product; reported in dBc.

Two-Tone SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (that is, degrades as signal level is lowered) or in dBFS (always related back to converter full scale).

Worst Other Spur

The ratio of the rms signal amplitude to the rms value of the worst spurious component (excluding the second and third harmonics) reported in dBc.

Transient Response Time

Transient response is defined as the time it takes for the ADC to reacquire the analog input after a transient from 10% above negative full scale to 10% below positive full scale.

Out-of-Range Recovery Time

Out-of-range recovery time is the time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale or from 10% below negative full scale to 10% below positive full scale.

EQUIVALENT CIRCUITS

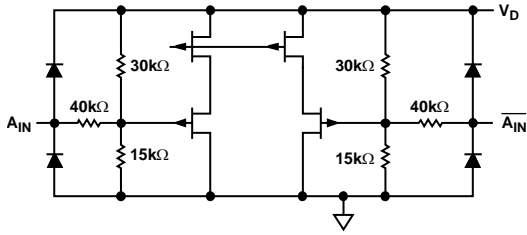


Figure 6. Analog Input Stage

02001-B-006

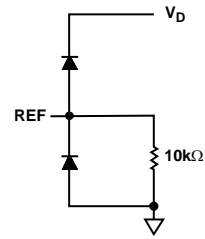


Figure 10. Reference Inputs

02001-B-010

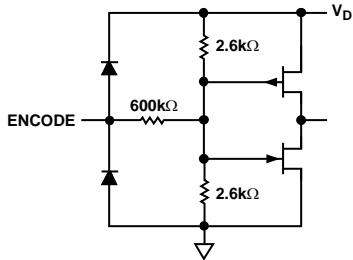


Figure 7. Encode Inputs

02001-B-007

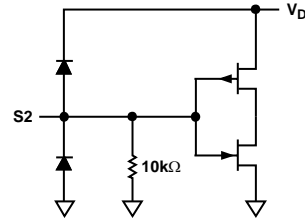


Figure 11. S2 Input

02001-B-011

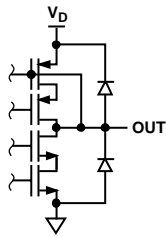


Figure 8. Reference Output Stage

02001-B-008

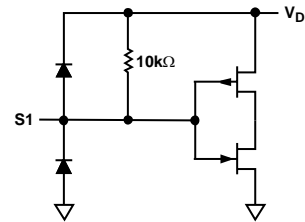


Figure 12. S1 Input

02001-B-012

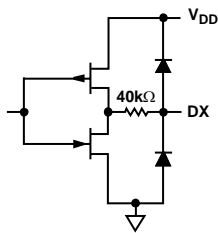


Figure 9. Digital Output Stage

02001-B-009

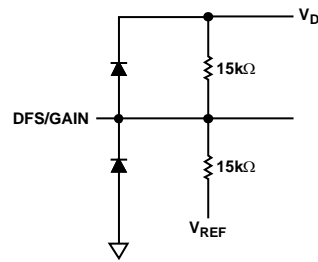


Figure 13. DFS/Gain Input

02001-B-013

TYPICAL PERFORMANCE CHARACTERISTICS

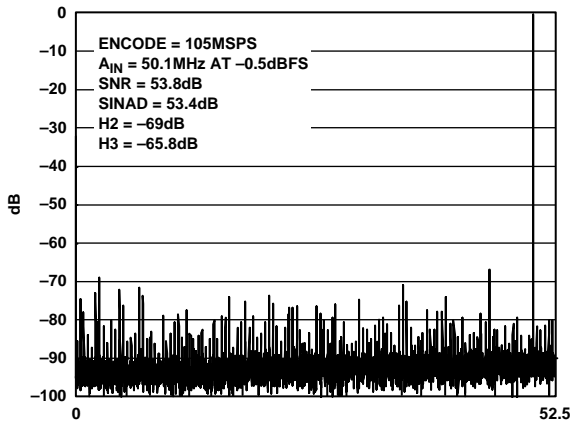


Figure 14. FFT: FS = 105 MSPS, A_{IN} = 50.1 MHz @ -0.5 dBFS, Differential, 1 V p-p Input Range

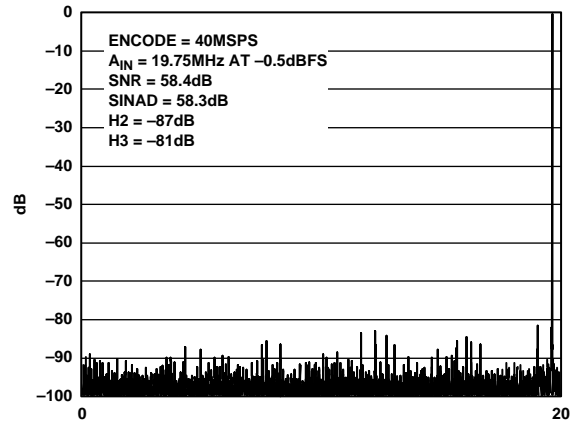


Figure 17. FFT: FS = 40 MSPS, A_{IN} = 19.75 MHz @ -0.5 dBFS, Differential, 1 V p-p Input Range

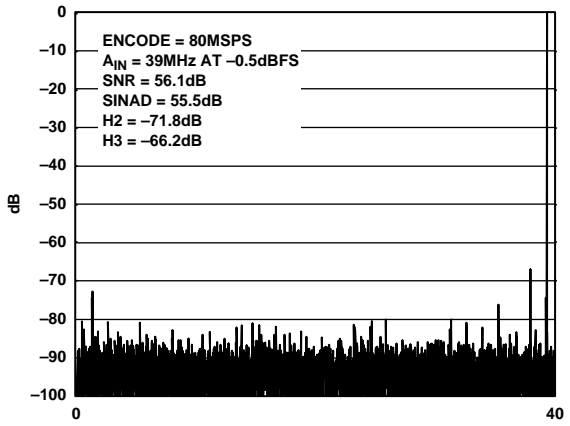


Figure 15. FFT: FS = 80 MSPS, A_{IN} = 39 MHz @ -0.5 dBFS, Differential, 1 V p-p Input Range

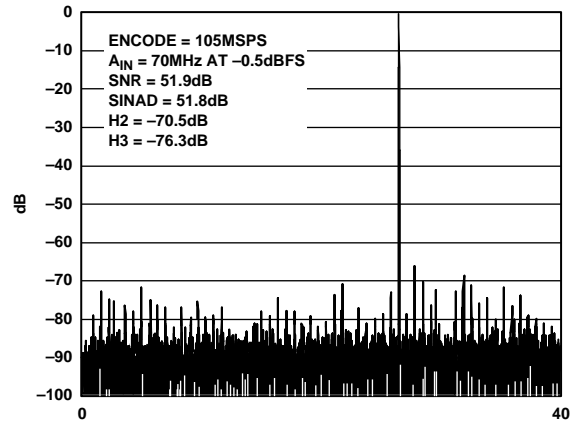


Figure 18. FFT: FS = 105 MSPS A_{IN} = 70 MHz @ -0.5 dBFS, Differential, 1 V p-p Input Range

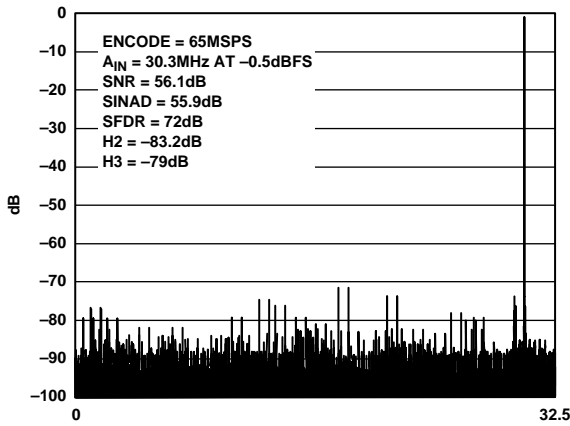


Figure 16. FFT: FS = 65 MSPS, A_{IN} = 30.3 MHz @ -0.5 dBFS, Differential, 2 V p-p Input Range

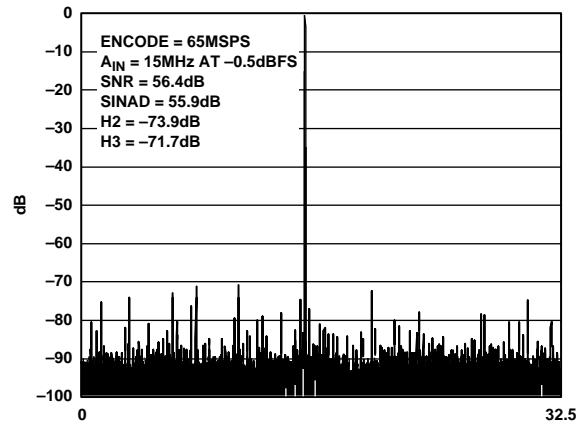


Figure 19. FFT: FS = 65 MSPS, A_{IN} = 15 MHz @ -0.5 dBFS; with AD8138 Driving ADC Inputs, 1 V p-p Input Range

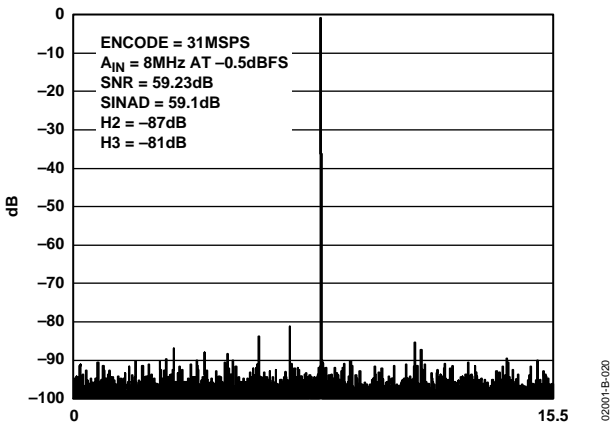


Figure 20. FFT: $FS=31\text{ MSPS}$, $A_{IN} = 8\text{ MHz @ } -0.5\text{ dBFS}$, Differential, 1 V p-p Input Range

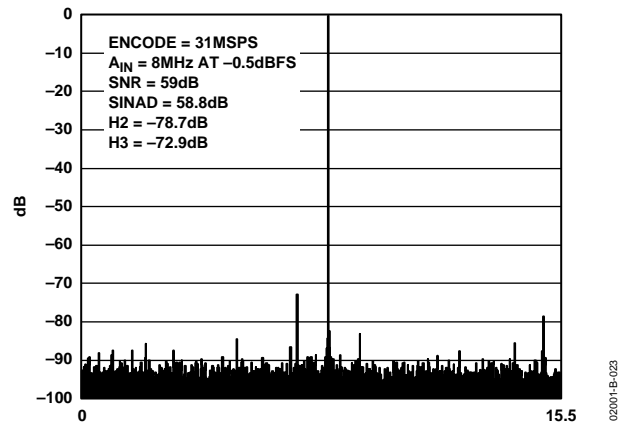


Figure 23. FFT: $FS=31\text{ MSPS}$, $A_{IN} = 8\text{ MHz @ } -0.5\text{ dBFS}$, Differential, with AD8138 Driving ADC Inputs, 1 V p-p Input Range

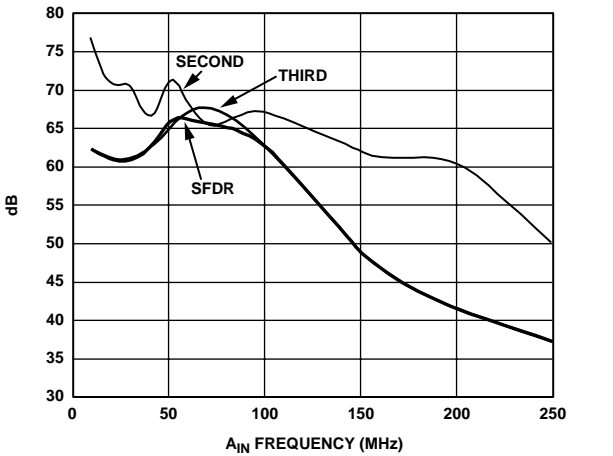


Figure 21. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, $FS = 105\text{ MSPS}$)

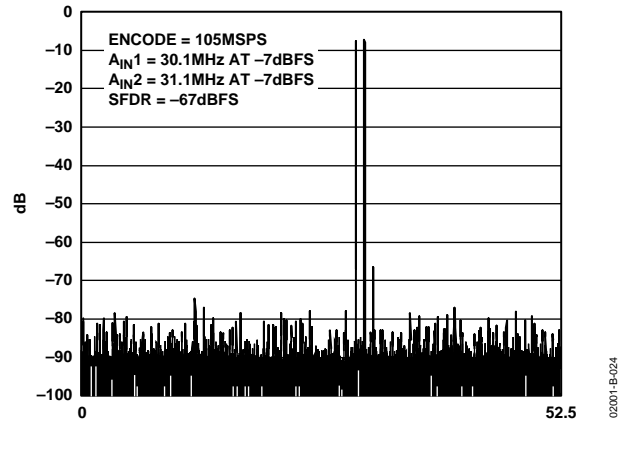


Figure 24. Two-Tone Intermodulation Distortion (30 MHz and 31 MHz; 1 V p-p, $FS = 105\text{ MSPS}$)

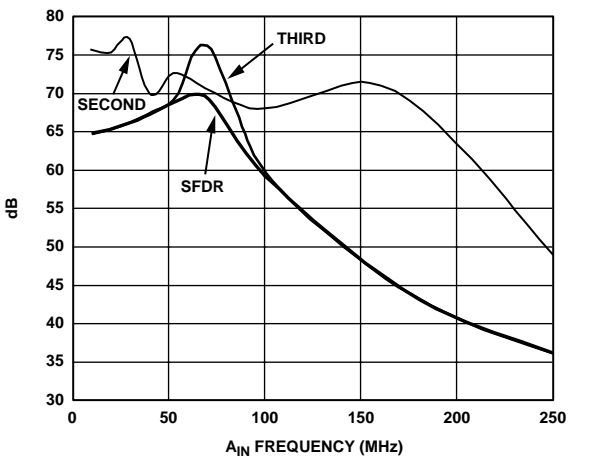


Figure 22. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, $FS = 80\text{ MSPS}$)

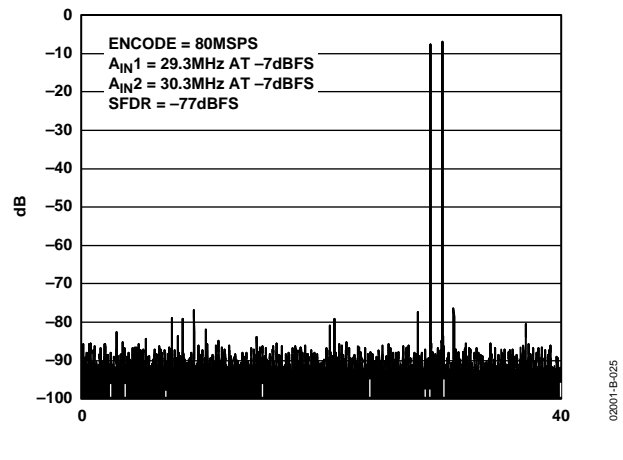


Figure 25. Two-Tone Intermodulation Distortion (29.3 MHz and 30.3 MHz; 1 V p-p, $FS = 80\text{ MSPS}$)

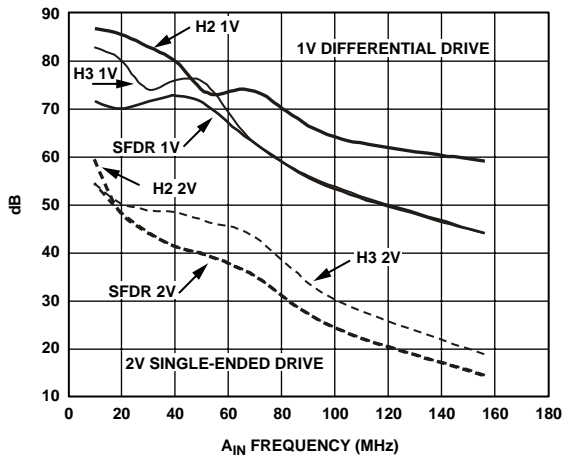


Figure 26. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency ($F_S = 65$ MSPS)

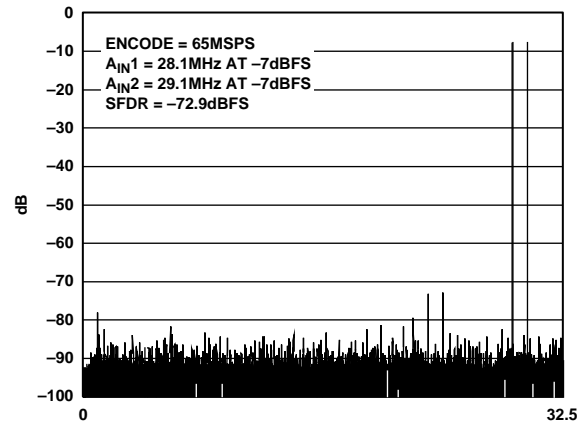


Figure 29. Two-Tone Intermodulation Distortion (28 MHz, 29 MHz; 1 V p-p, $F_S = 65$ MSPS)

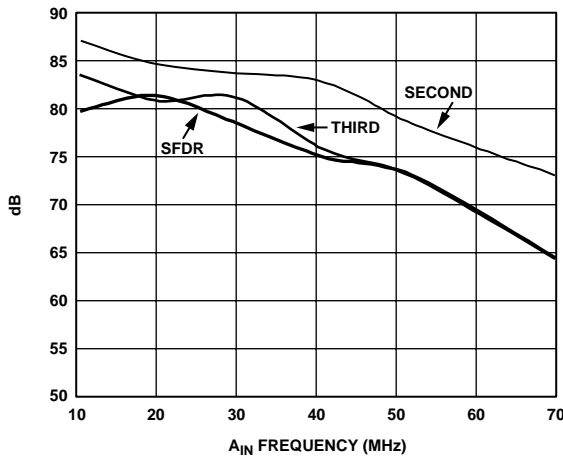


Figure 27. Harmonic Distortion (Second and Third) and SFDR vs. A_{IN} Frequency (1 V p-p, $F_S = 40$ MSPS)

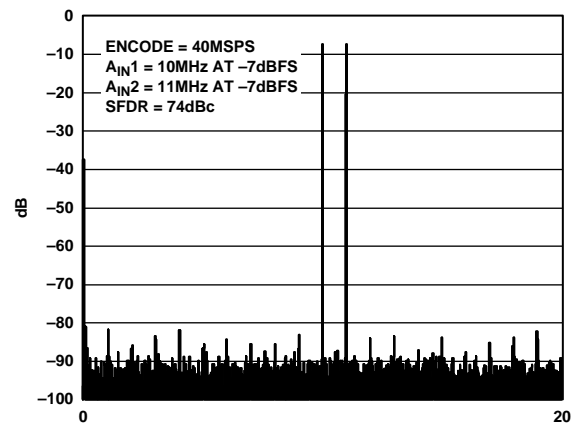


Figure 30. Two-Tone Intermodulation Distortion (10 MHz, 11 MHz; 1 V p-p, $F_S = 40$ MSPS)

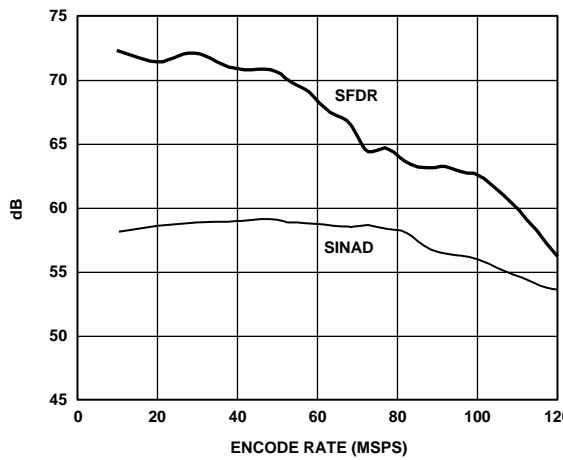


Figure 28. SINAD and SFDR vs. Encode Rate ($f_{IN} = 10.3$ MHz, 105 MSPS Grade) $A_{IN} = -0.5$ dBFS Differential, 1 V p-p Analog Input Range)

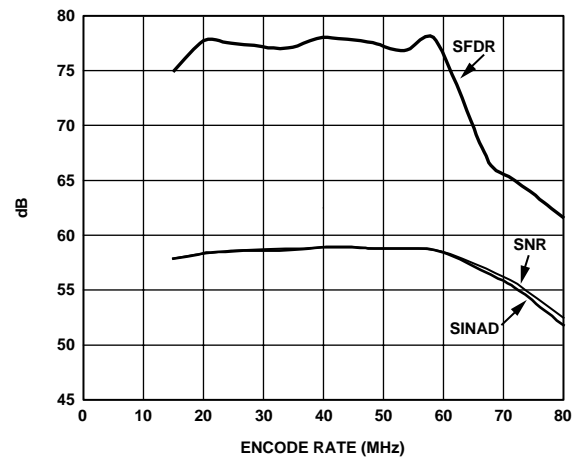
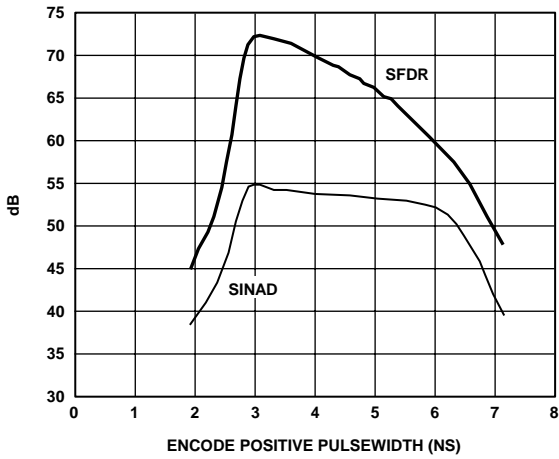
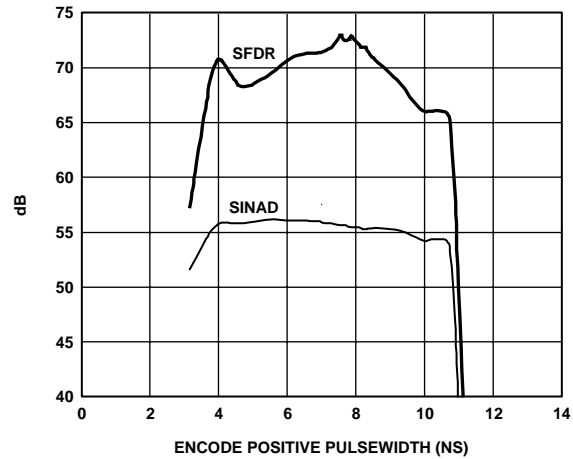


Figure 31. SINAD and SFDR vs. Encode Rate ($A_{IN} = 10.3$ MHz, 65 MSPS Grade) $A_{IN} = -0.5$ dBFS Differential, 1 V p-p Analog Input Range)



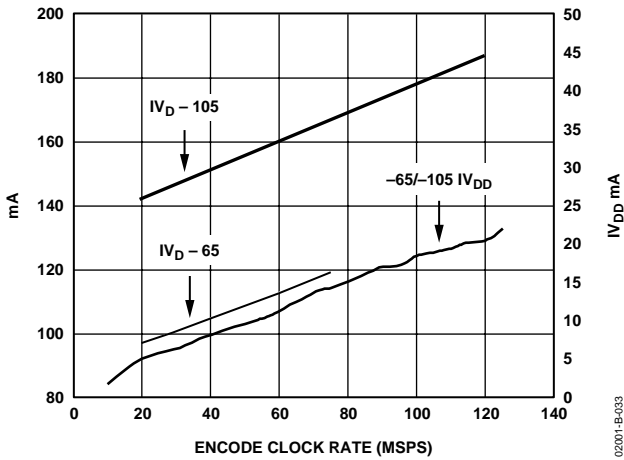
02001-B-032

Figure 32. SINAD and SFDR vs. Encode Pulse Width High, $A_{IN} = -0.5$ dBFS Single-Ended, 1 V p-p Analog Input Range 105 MSPS



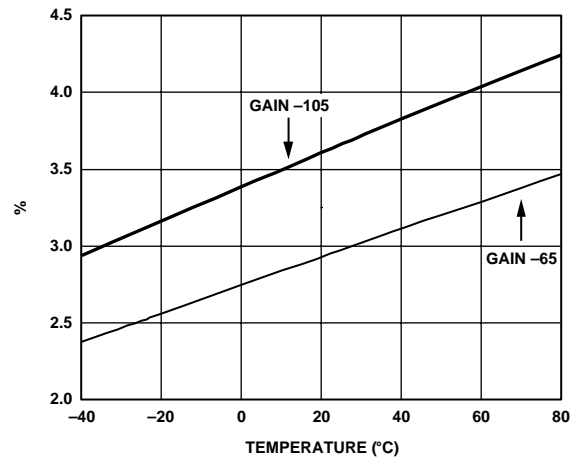
02001-B-035

Figure 35. SINAD and SFDR vs. Encode Pulse Width High, $A_{IN} = -0.5$ dBFS Single-Ended, 1 V p-p Analog Input Range 65 MSPS



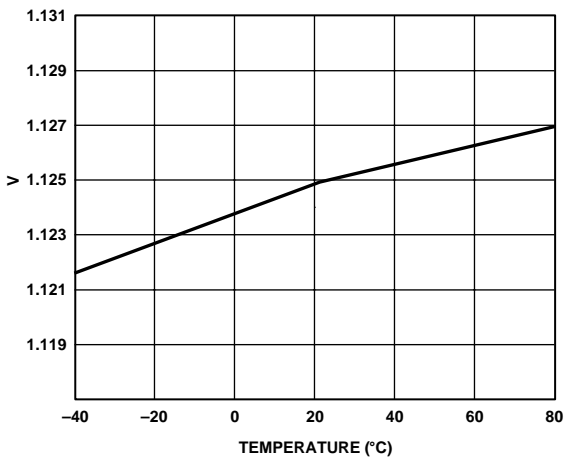
02001-B-033

Figure 33. I_{VD} and I_{VDD} vs. Encode Rate ($A_{IN} = 10.3$ MHz, @ -0.5 dBFS), -65 MSPS/ -105 MSPS Grade CI = 5 pF



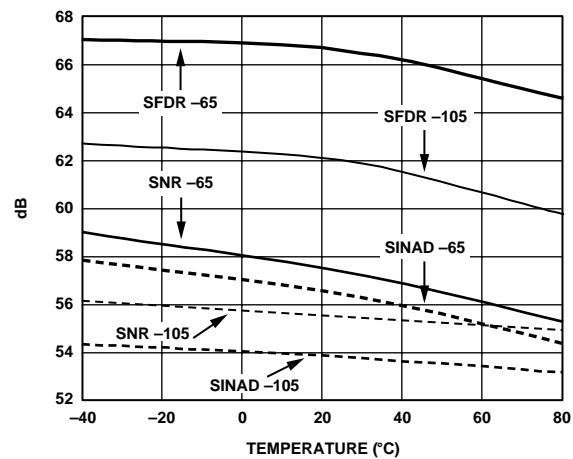
02001-B-036

Figure 36. Gain Error vs. Temperature, $A_{IN} = 10.3$ MHz, -65 MSPS Grade, -105 MSPS Grade, 1 V p-p



02001-B-034

Figure 34. V_{REF} Output Voltage vs. Temperature ($I_{LOAD} = 300$ μ A)



02001-B-037

Figure 37. SNR, SINAD, SFDR vs. Temperature, $A_{IN} = 10.3$ MHz, -65 MSPS Grade, -105 MSPS Grade, 1 V p-p

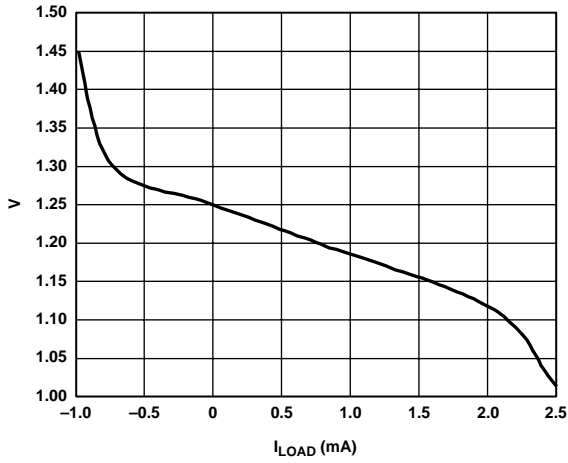


Figure 38. V_{REF} vs. I_{LOAD}

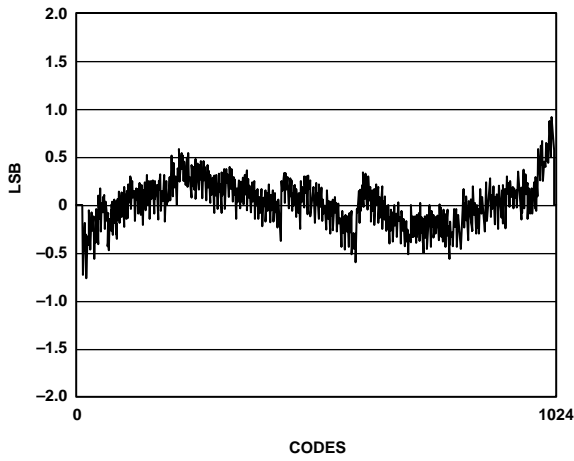


Figure 39. Typical INL Plot, 10.3 MHz A_{IN} @ 80 MSPS

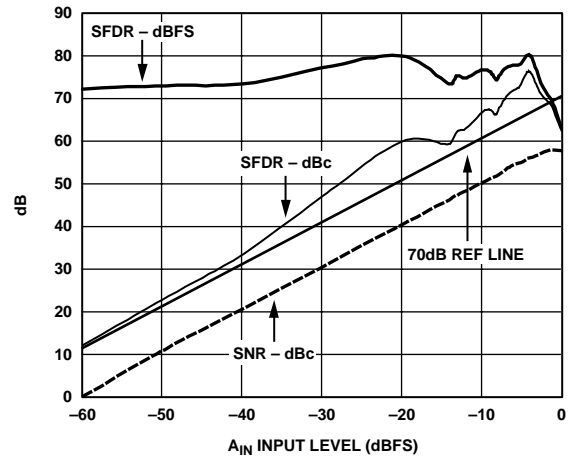


Figure 40. SFDR vs. A_{IN} Input Level, 10.3 MHz A_{IN} @ 80 MSPS

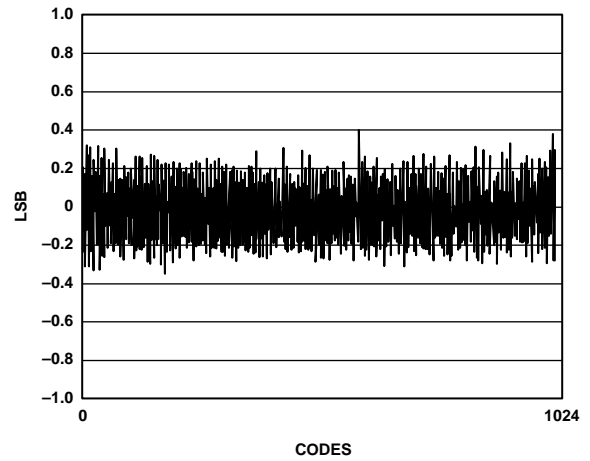


Figure 41. Typical DNL Plot, 10.3 MHz A_{IN} @ 80 MSPS

THEORY OF OPERATION

The AD9218 ADC architecture is a bit-per-stage pipeline-type converter utilizing switch capacitor techniques. These stages determine the 7 MSBs and drive a 3-bit flash. Each stage provides sufficient overlap and error correction, allowing optimization of comparator accuracy. The input buffers are differential, and both sets of inputs are internally biased. This allows the most flexible use of ac-coupled or dc-coupled and differential or single-ended input modes. The output staging block aligns the data, carries out the error correction, and feeds the data to output buffers. The set of output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. There is no discernible difference in performance between the two channels.

USING THE AD9218 ENCODE INPUT

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A track-and-hold circuit is essentially a mixer. Any noise, distortion, or timing jitter on the clock is combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9218, and the user is advised to give commensurate thought to the clock source. The ENCODE input is fully TTL/CMOS compatible.

Digital Outputs

The digital outputs are TTL/CMOS compatible for lower power consumption. During power-down, the output buffers transition to a high impedance state. A data format selection option supports either twos complement (set high) or offset binary output (set low) formats.

Analog Input

The analog input to the AD9218 is a differential buffer. For best dynamic performance, impedance at A_{IN} and \overline{A}_{IN} should match. Special care was taken in the design of the analog input section of the AD9218 to prevent damage and data corruption when the input is overdriven. The nominal input range is 1.024 V p-p. Optimum performance is obtained when the part is driven differentially where common-mode noise is minimized and even-order harmonics are reduced. Figure 42 shows an example of the AD9218 being driven differentially via a wideband RF transformer for ac-coupled applications. As shown in Figure 43, applications that require dc-coupled differential drives can be accommodated using the AD8138 differential output op amp.

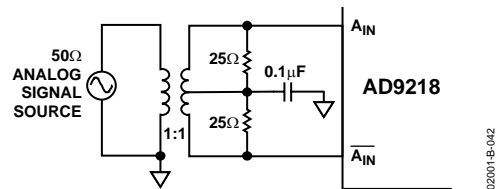


Figure 42. Using a Wideband Transformer to Drive the AD9218

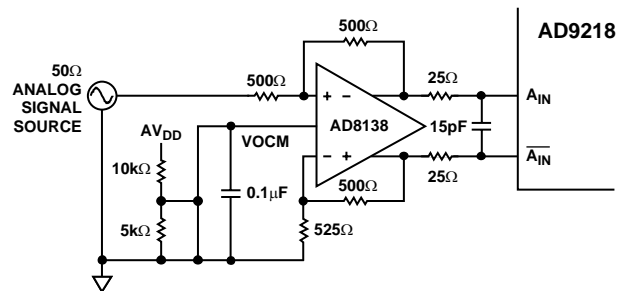


Figure 43. Using the AD8138 to Drive the AD9218

Voltage Reference

A stable and accurate 1.25 V voltage reference is built into the AD9218 (VREF OUT). Typically, the internal reference is used by strapping Pin 5 (REF_{INA}) and Pin 7 (REF_{INB}) to Pin 6 (REF_{OUT}). The input range for each channel can be adjusted independently by varying the reference voltage inputs applied to the AD9218. No appreciable degradation in performance occurs when the reference is adjusted $\pm 5\%$. The full-scale range of the ADC tracks reference voltage, which changes linearly. (A +5% change in VREF results in a +5% change in full-scale.)

Timing

The AD9218 provides latched data outputs, with five pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (see timing diagrams). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9218. These transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate is 20 MSPS. At clock rates below 20 MSPS, dynamic performance degrades.

User Select Options

Two pins are available for a combination of operational modes, enabling the user to power down both channels, excluding the reference, or just the B channel. Both modes place the output buffers in a high impedance state. Recovery from a power-down state is accomplished in 10 clock cycles following power-on.

The other option allows the user to skew the B channel output data by one-half a clock cycle. In other words, if two clocks are fed to the AD9218 and are 180 degrees out of phase, enabling the data align allows Channel B output data to be available at the rising edge of Clock A. If the same encode clock is provided to both channels and the data align pin is enabled, output data from Channel B is 180 degrees out of phase with respect to Channel A. If the same encode clock is provided to both channels and the data align pin is disabled, both outputs are delivered on the same rising edge of the clock.

APPLICATIONS

The wide analog bandwidth of the AD9218 makes it very attractive for a variety of high performance receiver and encoder applications. Figure 44 shows the dual ADC in a typical low cost I and Q demodulator implementation for cable, satellite, or wireless LAN modem receivers. The excellent dynamic performance of the ADC at higher analog input frequencies and encode rates lets users employ direct IF sampling techniques. IF sampling eliminates or simplifies analog mixer and filter stages to reduce total system cost and power.

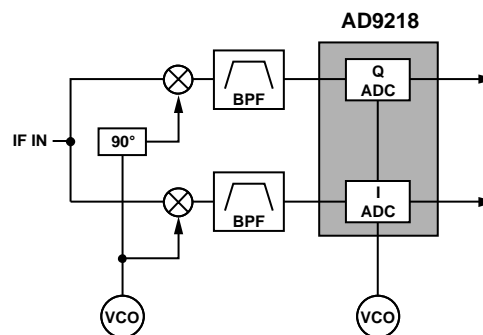


Figure 44. Typical I/Q Demodulation Scheme

02001B-044

AD9218

AD9218/AD9288 CUSTOMER PCB BOM

Table 9. Bill of Material

| # | QTY | REFDES | DEVICE | PACKAGE | VALUE | Comments |
|----|-----|---|-------------------------------|----------------------|-------------------|---|
| 1 | 29 | C1, C3-C15, C20, C21, C24, C25, C27, C30-C35, C39-C42 | Capacitor | 0603 | .1 μ F | |
| 2 | 2 | C2, C36 | Capacitor | 0603 | 15 pF | 8138 out |
| 3 | 7 | C16-C19, C26, C37, C38 | Capacitor | TAJD | 10 μ F | |
| 4 | 28 | E1, E2, E3, E4, E12-E30, E34-E38 | W-HOLE | W-HOLE | | |
| 5 | 4 | H1, H2, H3, H4 | MTHOLE | MTHOLE | | |
| 6 | 5 | J1, J2, J3, J4, J5 | SMA | SMA | | J2, J3, not placed |
| 7 | 3 | P1, P4, P11 | 4-pin power connector | Post | Z5.531.3425.0 | Wieland |
| 8 | 3 | P1, P4, P11 | 4-pin power connector | Detachable Connector | 25.602.5453.0 | Wieland |
| 9 | 1 | P2, P3 ¹ | 80-pin rt. angle male | | TSW-140-08-L-D-RA | Samtec |
| 10 | 4 | R1, R2, R32, R34 | Resistor | 0603 | 36 Ω | R1, R2, R32, R34, not placed |
| 11 | 9 | R3, R7, R11, R14, R22, R23, R24, R30, R51 | Resistor | 0603 | 50 Ω | R11, R22, R23, R24, R30, R51 not placed |
| 12 | 17 | R4, R5, R8, R9, R10, R12, R13, R20, R33, R35, R36, R37, R40, R42, R43, R50, R53 | Resistor | 0603 | Zero Ω | R43, R50 not placed |
| 13 | 2 | R6, R38 | Resistor | 0603 | 25 Ω | R6, R38 not placed |
| 14 | 6 | R15, R16, R18, R26, R29, R31 | Resistor | 0603 | 500 Ω | R16, R29 not placed |
| 15 | 2 | R17, R25 | Resistor | 0603 | 525 Ω | |
| 16 | 2 | R19, R27 | Resistor | 0603 | 4K Ω | |
| 17 | 12 | R21, R28, R39, R41, R44, R46-R49, R52, R54, R55 | Resistor | 0603 | 1K Ω | |
| 18 | 2 | T1, T2 | Transformer | ADT1-1WT | | Minicircuits |
| 19 | 1 | U1 | AD9288 or AD9218 ² | LQFP48 | | |
| 20 | 2 | U2, U3 | 74LCX821 | | | |
| 21 | 2 | U5, U6 | SN74VCX86 | | | |
| 22 | 4 | U7, U8, U9, U10 | Resistor array | CTS | 47 Ω | 768203470G |
| 23 | 2 | U11, U12 | AD8138 opamp ³ | | | |

¹ P2, P3 are implemented as one physical 80-pin connector SAMTEC TSW-140-08-L-D-RA.

² AD9288/PCB populated with AD9288-100, AD9218-65/PCB populated with AD9218-65, AD9218-105/PCB populated with AD9218-105.

³ To use optional amp: place R22, R23, R30, R24, R16, R29, remove R4, R36.

EVALUATION BOARD

The AD9218/AD9288 customer evaluation board offers an easy way to test the AD9218 or the AD9288. The compatible pinout of the two parts facilitates the use of one PCB for testing either part. The PCB requires power supplies, a clock source, and a filtered analog source for most ADC testing required.

POWER CONNECTOR

Power is supplied to the board via a detachable 12-lead power strip. The minimum 3 V supplies required to run the board are V_{DD} , V_{DL} , and V_{DD} . To allow the use of the optional amplifier path, ± 5 V supplies are required.

ANALOG INPUTS

Each channel has an independent analog path that uses a wideband transformer to drive the ADC differentially from a single-ended sine source at the input SMAs. The transformer paths can be bypassed to allow the use of a dc-coupled path using two AD8138 op amps with a simple board modification. The analog input should be band-pass filtered to remove any harmonics in the input signal and to minimize aliasing.

VOLTAGE REFERENCE

The AD9218 has an internal 1.25 V voltage reference; an external reference for each channel may be employed instead by connecting two external voltage references at the power connector and setting jumpers at E18 and E19. The evaluation board is shipped configured for internal reference mode.

CLOCKING

Each channel can be clocked by a common clock input at SMA input ENCODE A/B. The channels can also be clocked independently by a simple board modification. The clock input should be a low jitter sine source for maximum performance.

DATA OUTPUTS

The data outputs are latched on board by two 10-bit latches and drive an 8-pin connector which is compatible with the dual-channel FIFO board that is available from Analog Devices. This board, together with ADC analyzer software, can greatly simplify ADC testing.

DATA FORMAT/GAIN

The DFS/Gain pin can be biased for desired operation at the DFS jumper located at the S1, S2 jumpers.

TIMING

Timing on each channel can be controlled if needed on the PCB. Clock signals at the latches or the Data Ready signals that go to the output 80-pin connector can be inverted if required. Jumpers also allow for biasing of Pins S1 and S2 for power-down and timing alignment control.

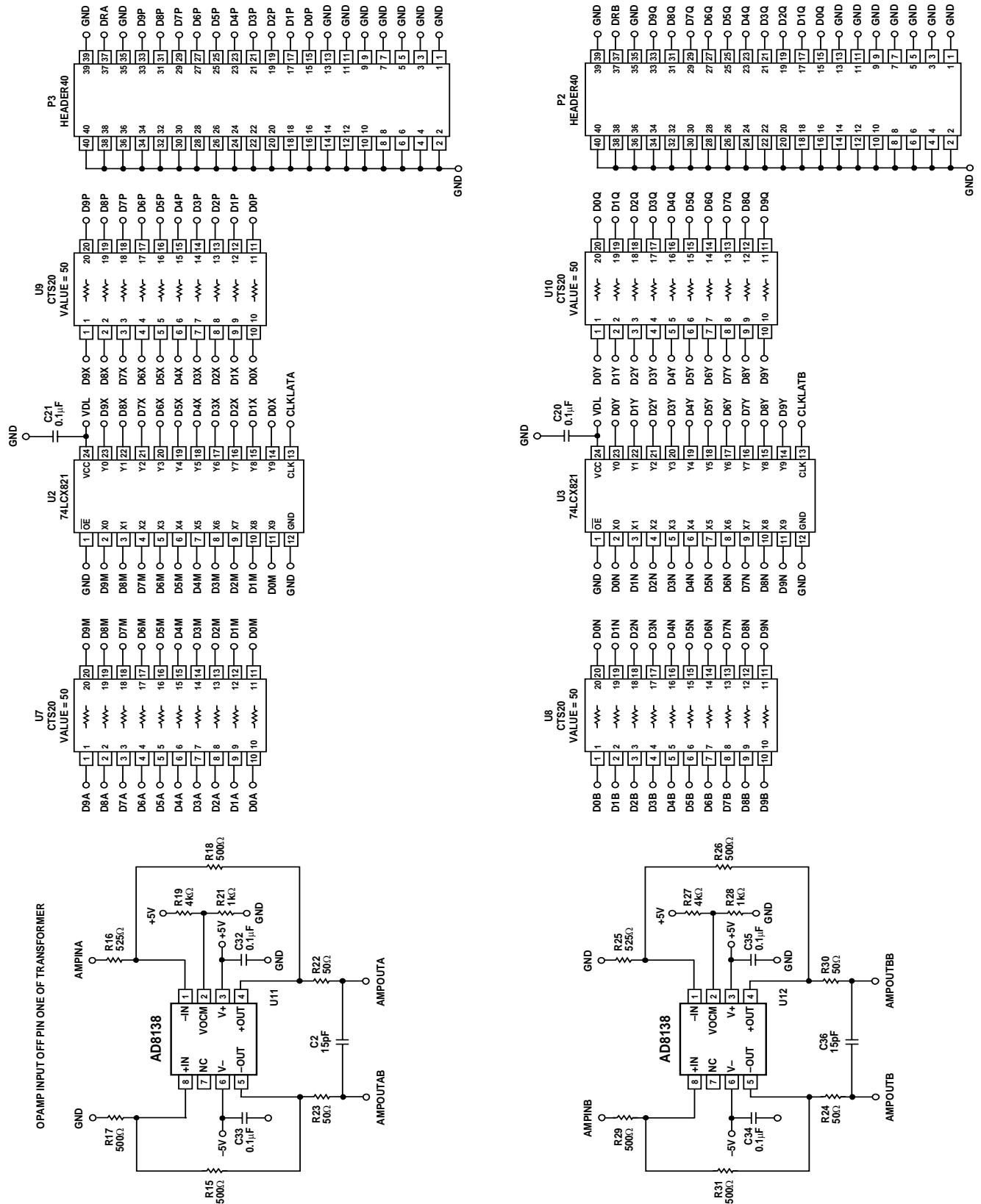


Figure 46. PCB Schematic (Continued)

AD9218

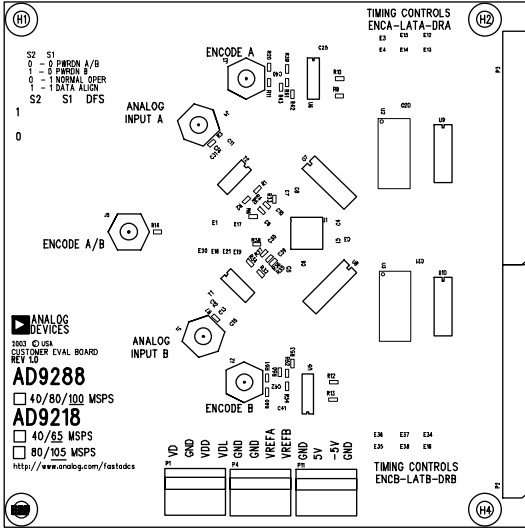


Figure 47. Top Silkscreen

02001-B-047

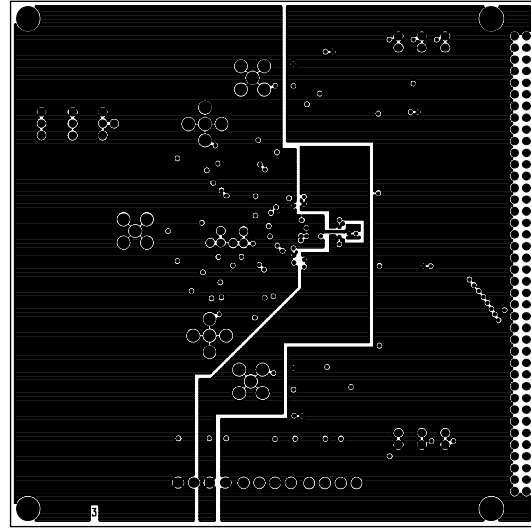


Figure 50. Split Power Plane

02001-B-050

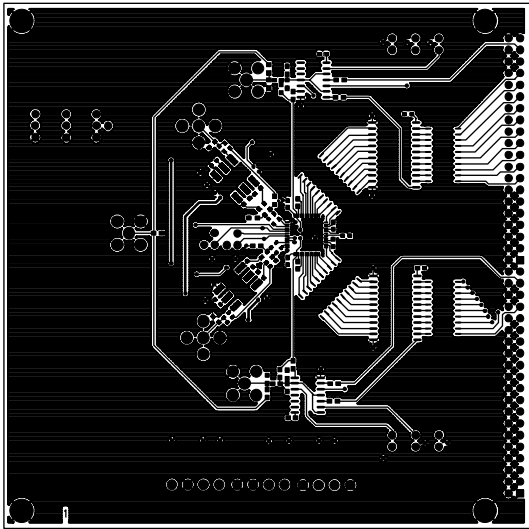


Figure 48. Top Routing

02001-B-048

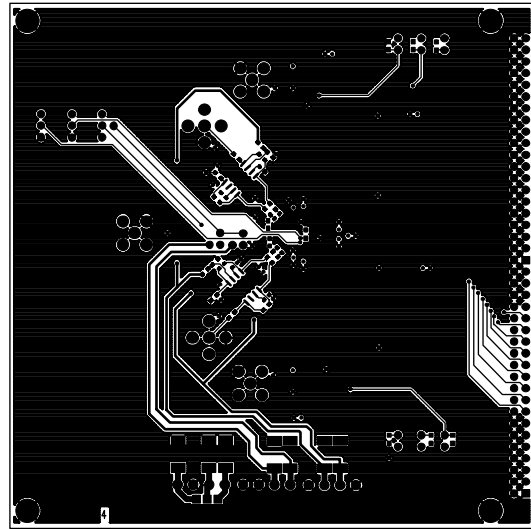


Figure 51. Bottom Routing

02001-B-051

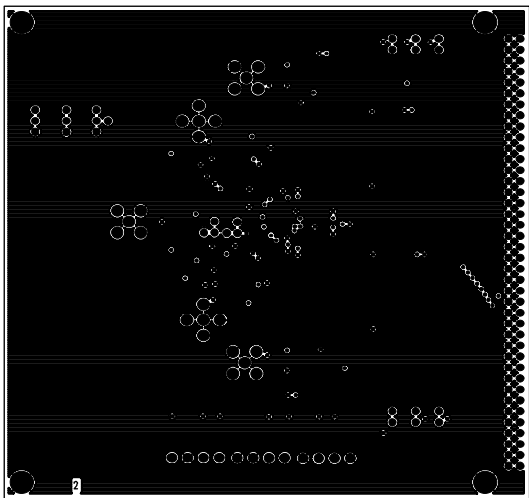


Figure 49. Ground Plane

02001-B-049

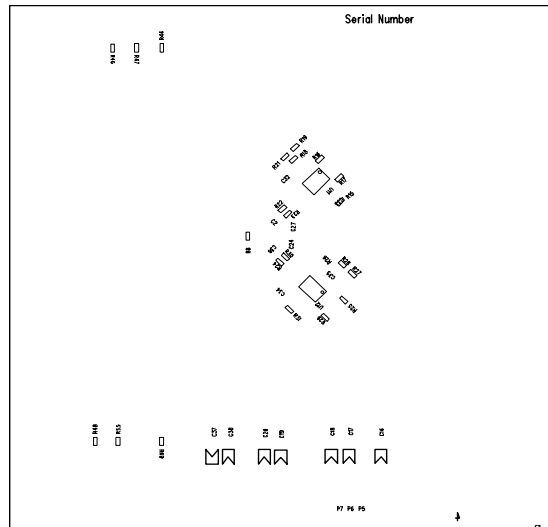


Figure 52. Bottom Silkscreen

02001-B-052

TROUBLESHOOTING

If the board does not seem to be working correctly, try the following:

- Verify power at the IC pins.
- Check that all jumpers are in the correct position for the desired mode of operation.
- Verify that V_{REF} is at 1.23 V.
- Try running encode clock and analog inputs at low speeds (20 MSPS/1 MHz) and monitor LCX821 outputs, DAC outputs, and ADC outputs for toggling.

The AD9218 evaluation board is provided as a design example for customers of Analog Devices, Inc. ADI makes no warranties, express, statutory, or implied, regarding merchantability or fitness for a particular purpose.

OUTLINE DIMENSIONS

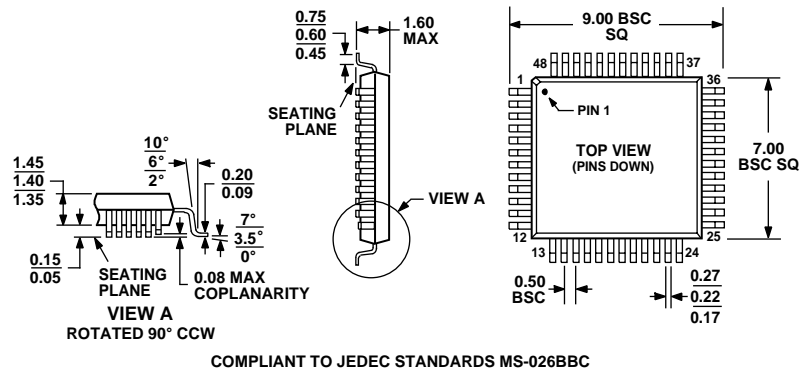


Figure 53. 48-Lead Low Profile Quad Flat Package [LQFP]

(ST-48)

Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-------------------------------|-------------------|---|----------------|
| AD9218BST-40 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BST-RL40 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-40 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-RL40 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BST-65 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BST-RL65 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-65 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-RL65 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BST-80 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BST-RL80 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-80 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-RL80 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BST-105 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BST-RL105 | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-105 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218BSTZ-RL105 ¹ | -40°C to +85°C | Low Profile Quad Flat Pack (1.4 mm thick: LQFP) | ST-48 |
| AD9218-65PCB | | Evaluation Board (Supports -40/-65 Grade) | |
| AD9218-105PCB | | Evaluation Board (Supports -80/-105 Grade) | |

¹ Z = Pb-free part.

AD9218

NOTES