Low Cost, DC to 150 MHz Variable Gain Amplifier

AD8330

FEATURES

Fully differential signal path, also used with single-sided signals
Inputs from 0.3 mV to 1 V rms, rail-to-rail outputs
Differential R_{IN} = 1 kΩ; R_{OUT} (each output) 75 Ω
Automatic offset compensation (optional)
Linear-in-dB and linear-in-magnitude gain modes
0 dB to 50 dB, for 0 V < V_{DBS} < 1.5 V (30 mV/dB)
Inverted gain mode: 50 dB to 0 dB at −30 mV/dB
×0.03 to ×10 nominal gain for 15 mV < V_{MAG} < 5 V
Constant bandwidth: 150 MHz at all gains
Low noise: 5 nV/√Hz typical at maximum gain
Low distortion: ≤−62 dBc typical
Low power: 20 mA typical at V_S of 2.7 V to 6 V
Available in a space-saving, 3 mm × 3 mm LFCSP package

APPLICATIONS

Pre-ADC signal conditioning
75 Ω cable driving adjust
AGC amplifiers

FUNCTIONAL BLOCK DIAGRAM

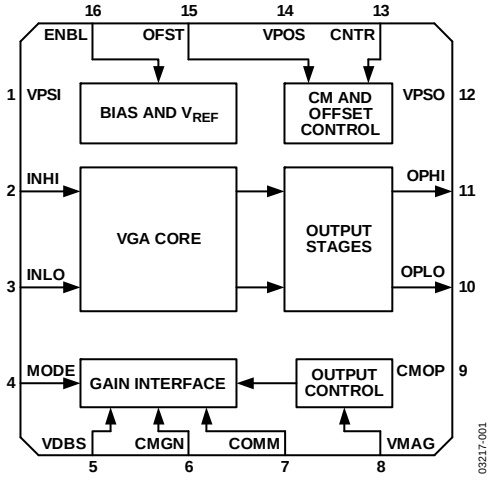

Figure 1.

GENERAL DESCRIPTION

The AD8330 is a wideband variable gain amplifier for applications requiring a fully differential signal path, low noise, well-defined gain, and moderately low distortion, from dc to 150 MHz. The input pins can also be driven from a single-ended source. The peak differential input is ±2 V, allowing sine wave operation at 1 V rms with generous headroom. The output pins can drive single-sided loads essentially rail-to-rail. The differential output resistance is 150 Ω. The output swing is a linear function of the voltage applied to the VMAG pin that internally defaults to 0.5 V, providing a peak output of ±2 V. This can be raised to 10 V p-p, limited by the supply voltage.

The basic gain function is linear-in-dB, controlled by the voltage applied to Pin VDBS. The gain ranges from 0 dB to 50 dB for control voltages between 0 V and 1.5 V—a slope of 30 mV/dB. The gain linearity is typically within ±0.1 dB. By changing the logic level on Pin MODE, the gain decreases over the same range, with an opposite slope. A second gain control port is provided at the VMAG pin and allows the user to vary the numeric gain from a factor of 0.03 to 10. All the parameters of the AD8330 have low sensitivities to temperature and supply voltages.

Using VMAG, the basic 0 dB to 50 dB range can be repositioned to any value from 20 dB higher (that is, 20 dB to 70 dB) to at least 30 dB lower (that is, –30 dB to +20 dB) to suit the application, thereby providing an unprecedented gain range of over 100 dB. A unique aspect of the AD8330 is that its bandwidth and pulse response are essentially constant for all gains, over both the basic 50 dB linear-in-dB range, but also when using the linear-in-magnitude function. The exceptional stability of the HF response over the gain range is of particular value in those VGA applications where it is essential to maintain accurate gain law-conformance at high frequencies.

An external capacitor at Pin OFST sets the high-pass corner of an offset reduction loop, whose frequency can be as low as 5 Hz. When this pin is grounded, the signal path becomes dc-coupled. When used to drive an ADC, an external common-mode control voltage at Pin CNTR can be driven to within 0.5 V of either ground or V_S to accommodate a wide variety of requirements. By default, the two outputs are positioned at the midpoint of the supply, $V_S/2$. Other features, such as two levels of power-down (fully off and a hibernate mode), further extend the practical value of this exceptionally versatile VGA.

The AD8330 is available in 16-lead LFCSP and 16-lead QSOP packages and is specified for operation from −40°C to +85°C.

Rev. E

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REVISION HISTORY

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1/08—Rev. C to Rev. D

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6/06—Rev. B to Rev. C

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SPECIFICATIONS

V_S = 5 V, T_A = 25°C, C_L = 12 pF on OPHI and OPLO, R_L = ∞, V_{DBS} = 0.75 V, V_{MODE} = high, V_{MAG} = Pin VMAG open circuit (0.5 V), V_{OFST} = 0 V, differential operation, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT INTERFACE	Pin INHI, Pin INLO				
Full-Scale Input	V_{DBS} = 0 V, differential drive	±1.4	±2		V
	V_{DBS} = 1.5 V	±4.5	±6.3		mV
Input Resistance	Pin-to-pin	800	1 k	1.2 k	Ω
Input Capacitance	Either pin to COMM		4		pF
Voltage Noise Spectral Density	f = 1 MHz, V_{DBS} = 1.5 V; inputs ac-shorted		5		nV/√Hz
Common-Mode Voltage Level			3.0		V
Input Offset	Pin OFST connected to Pin COMM		1		mV rms
Drift			2		µV/°C
Permissible CM Range[1]		0		V_S	V
Common-Mode AC Rejection	f = 1 MHz, 0.1 V rms		−60		dB
	f = 50 MHz		−55		dB
OUTPUT INTERFACE	Pin OPHI, Pin OPLO				
Small Signal −3 dB Bandwidth	0 V < V_{DBS} < 1.5 V		150		MHz
Peak Slew Rate	V_{DBS} = 0 V		1500		V/µs
Peak-to-Peak Output Swing		±1.8	±2	±2.2	V
	V_{MAG} ≥ 2 V (peaks are supply limited)	±4	±4.5		V
Common-Mode Voltage	Pin CNTR O/C	2.4	2.5	2.6	V
Voltage Noise Spectral Density	f = 1 MHz, V_{DBS} = 0 V		62		nV/√Hz
Differential Output Impedance	Pin-to-pin	120	150	180	Ω
HD2[2]	V_{OUT} = 1 V p-p, f = 10 MHz, R_L = 1 kΩ		−62		dBc
HD3[2]	V_{OUT} = 1 V p-p, f = 10 MHz, R_L = 1 kΩ		−53		dBc
OUTPUT OFFSET CONTROL	Pin OFST				
AC-Coupled Offset	C_{HPF} on Pin OFST (0 V < V_{DBS} < 1.5 V)		10		mV rms
High-Pass Corner Frequency	C_{HPF} = 3.3 nF, from OFST to CNTR (scales as 1/C_{HPF})		100		kHz
COMMON-MODE CONTROL	Pin CNTR				
Usable Voltage Range		0.5		4.5	V
Input Resistance	From Pin CNTR to V_S/2		4		kΩ
DECIBEL GAIN CONTROL	VDBS, CMGN, and MODE pins				
Normal Voltage Range	CMGN connected to COMM		0 to 1.5		V
Elevated Range	CMGN O/C (V_{CMGN} rises to 0.2 V)		0.2 to 1.7		V
Gain Scaling	Mode high or low	27	30	33	mV/dB
Gain Linearity Error	0.3 V ≤ V_{DBS} ≤ 1.2 V	−0.35	±0.1	+0.35	dB
Absolute Gain Error	V_{DBS} = 0 V	−2	±0.5	+2	dB
Bias Current	Flows out of Pin VDBS		100		nA
Incremental Resistance			100		MΩ
Gain Settling Time to 0.5 dB Error	V_{DBS} stepped from 0.05 V to 1.45 V or 1.45 V to 0.05 V		250		ns
Mode Up/Down	Pin MODE				
Mode Up Logic Level	Gain increases with V_{DBS}, MODE = O/C	1.5			V
Mode Down Logic Level	Gain decreases with V_{DBS}			0.5	V
LINEAR GAIN INTERFACE	Pin VMAG, Pin CMGN				
Peak Output Scaling, Gain vs. V_{MAG}	See the Circuit Description section	3.8	4.0	4.2	V/V
Gain Multiplication Factor vs. V_{MAG}	Gain is nominal when V_{MAG} = 0.5 V		×2		
Usable Input Range		0		5	V
Default Voltage	V_{MAG} O/C	0.48	0.5	0.52	V
Incremental Resistance			4		kΩ
Bandwidth	For V_{MAG} ≥ 0.1 V		150		MHz

Parameter	Conditions	Min	Typ	Max	Unit
CHIP ENABLE	Pin ENBL				
Logic Voltage for Full Shutdown				0.5	V
Logic Voltage for Hibernate Mode	Output pins remain at CNTR	1.3	1.5	1.7	V
Logic Voltage for Full Operation		2.3			V
Current in Full Shutdown			20	100	μA
Current in Hibernate Mode			1.5		mA
Minimum Time Delay[3]			1.7		μs
POWER SUPPLY	VPSI, VPOS, VPSO, COMM, and CMOP pins				
Supply Voltage		2.7		6	V
Quiescent Current	V_{DBS} = 0.75 V		20	27	mA

[1] The use of an input common-mode voltage significantly different from the internally set value is not recommended due to its effect on noise performance. See Figure 56.
[2] See the Typical Performance Characteristics section for more detailed information on distortion in a variety of operating conditions.
[3] For minimum sized coupling capacitors.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage	6 V
Power Dissipation	
RQ-16 Package[1]	0.62 W
CP-16-3 Package	1.67 W
Input Voltage at Any Pin	V_S + 200 mV
Storage Temperature Range	−65°C to +150°C
θ_{JA}	
RQ-16 Package	105.4°C/W
CP-16-3 Package	60°C/W
θ_{JC}	
RQ-16 Package	39°C/W
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 60 sec)	300°C

[1] Four-Layer JEDEC Board (252P).

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

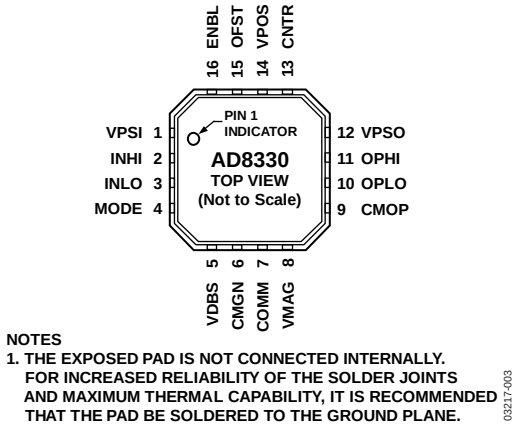

Figure 2. 16-Lead LFCSP Pin Configuration

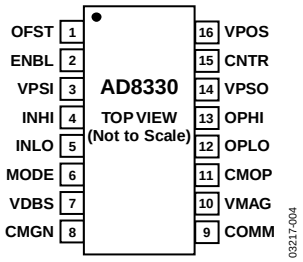

Figure 3. 16-Lead QSOP Pin Configuration

Table 3. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VPSI	Positive Supply for Input Stages.
2	INHI	Differential Signal Input, Positive Polarity.
3	INLO	Differential Signal Input, Negative Polarity.
4	MODE	Logic Input: Selects Gain Slope. High = gain up vs. V_{DBS}.
5	VDBS	Input for Linear-in-dB Gain Control Voltage, V_{DBS}.
6	CMGN	Common Baseline for Gain Control Interfaces.
7	COMM	Ground for Input and Gain Control Bias Circuitry.
8	VMAG	Input for Gain/Amplitude Control, V_{MAG}.
9	CMOP	Ground for Output Stages.
10	OPLO	Differential Signal Output, Negative Polarity.
11	OPHI	Differential Signal Output, Positive Polarity.
12	VPSO	Positive Supply for Output Stages.
13	CNTR	Common-Mode Output Voltage Control.
14	VPOS	Positive Supply for Inner Stages.
15	OFST	Used in Offset Control Modes.
16	ENBL	Power Enable, Active High.
	EPAD	Exposed Pad. It is recommended that the pad be soldered to the ground plane.

Table 4. 16-Lead QSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	OFST	Used in Offset Control Modes.
2	ENBL	Power Enable, Active High.
3	VPSI	Positive Supply for Input Stages.
4	INHI	Differential Signal Input, Positive Polarity.
5	INLO	Differential Signal Input, Negative Polarity.
6	MODE	Logic Input: Selects Gain Slope. High = gain up vs. V_{DBS}.
7	VDBS	Input for linear-in-dB Gain Control Voltage, V_{DBS}.
8	CMGN	Common Baseline for Gain Control Interfaces.
9	COMM	Ground for Input and Gain Control Bias Circuitry.
10	VMAG	Input for Gain/Amplitude Control, V_{MAG}.
11	CMOP	Ground for Output Stages.
12	OPLO	Differential Signal Output, Negative Polarity.
13	OPHI	Differential Signal Output, Positive Polarity.
14	VPSO	Positive Supply for Output Stages.
15	CNTR	Common-Mode Output Voltage Control.
16	VPOS	Positive Supply for Inner Stages.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, C_L = 12 pF, V_{DBS} = 0.75 V, V_{MODE} = high (or O/C) V_{MAG} = O/C (0.5 V), R_L = ∞, V_{OFST} = 0, differential operation, unless otherwise noted.

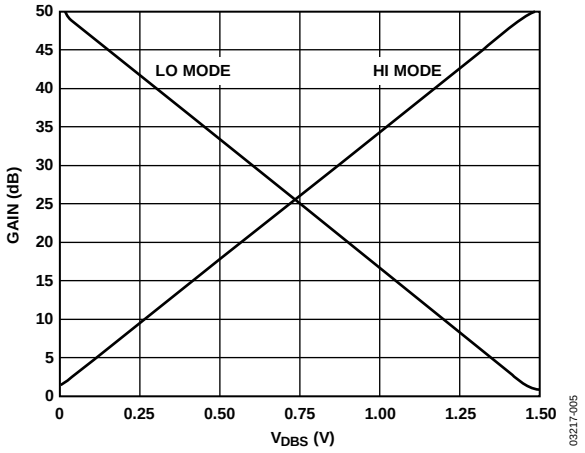

Figure 4. Gain vs. V_{DBS}

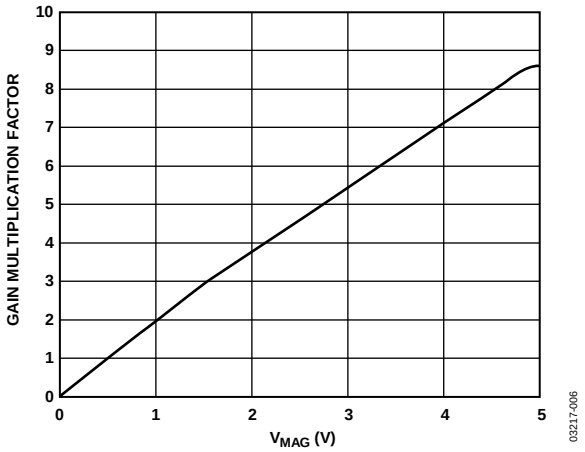

Figure 5. Linear Gain Multiplication Factor vs. V_{MAG}

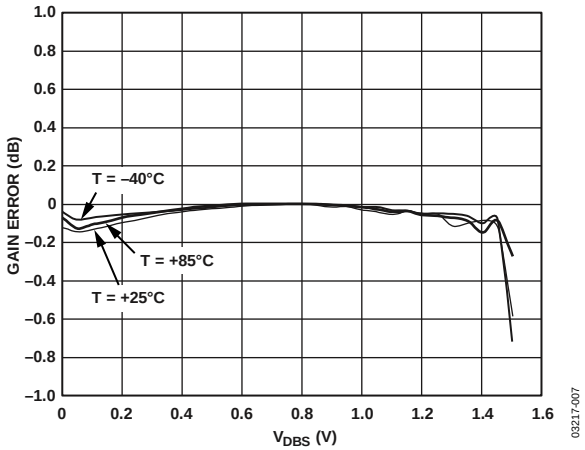

Figure 6. Gain Linearity Error Normalized at 25°C vs. V_{DBS}, at Three Temperatures, f = 1 MHz

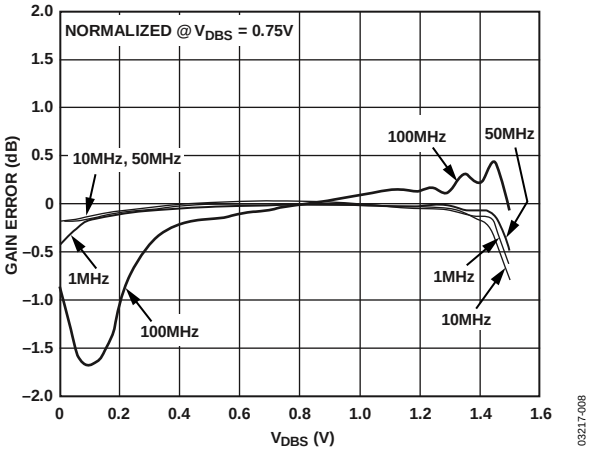

Figure 7. Gain Error vs. V_{DBS} at Various Frequencies

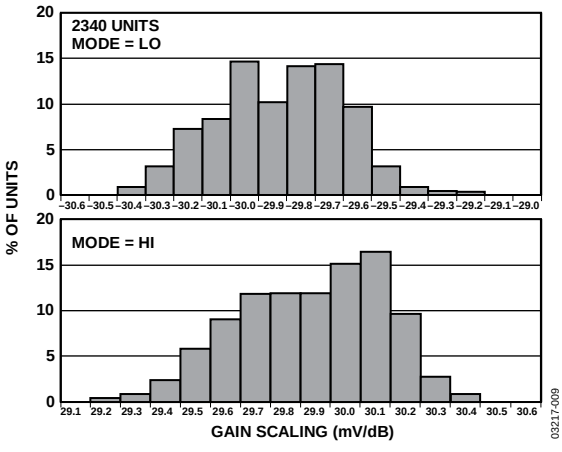

Figure 8. Gain Slope Histogram

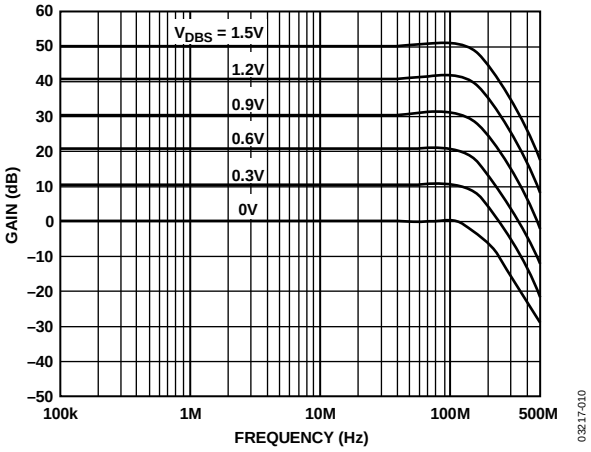

Figure 9. Frequency Response in 10 dB Steps for Various Values of V_{DBS}

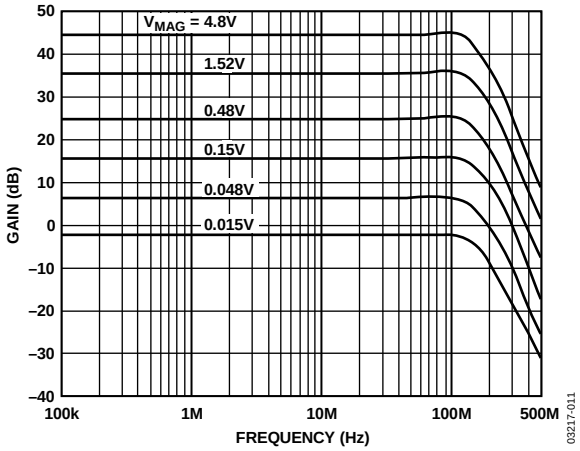

Figure 10. Frequency Response for Various Values of V_{MAG}, V_{DBS} = 0.75 V

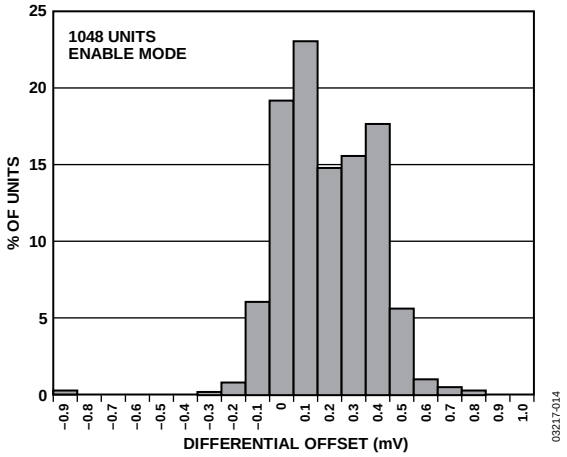

Figure 13. Differential Input Offset Histogram

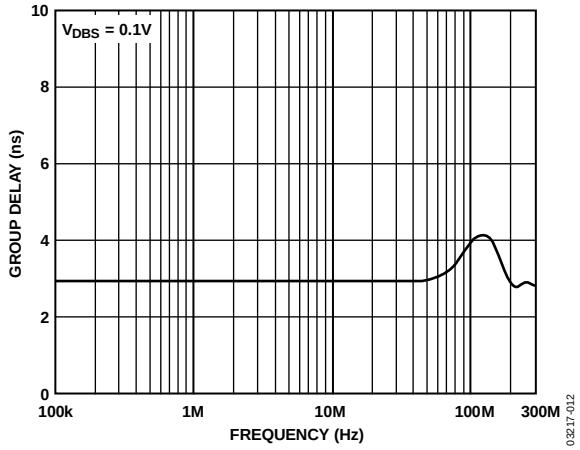

Figure 11. Group Delay vs. Frequency

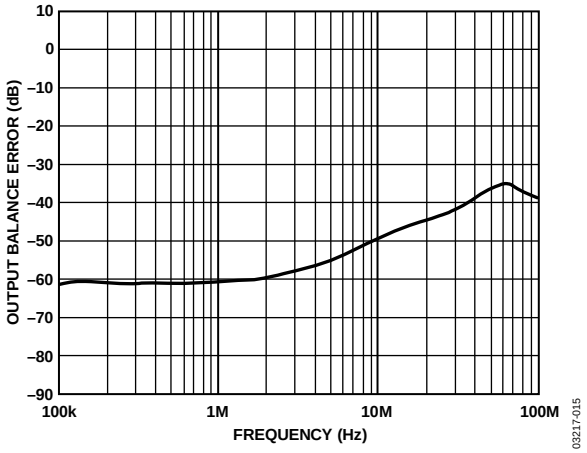

Figure 14. Output Balance Error vs. Frequency for a Representative Part

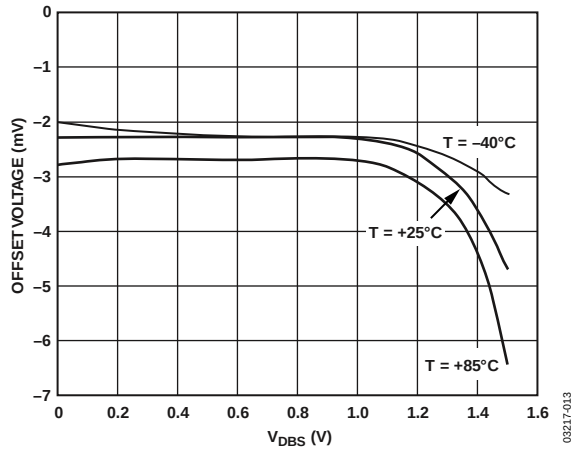

Figure 12. Differential Output Offset vs. V_{DBS} for Three Temperatures, for a Representative Part

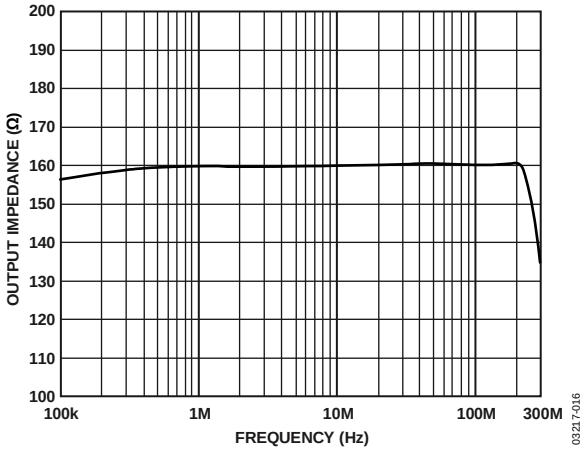

Figure 15. Output Impedance vs. Frequency

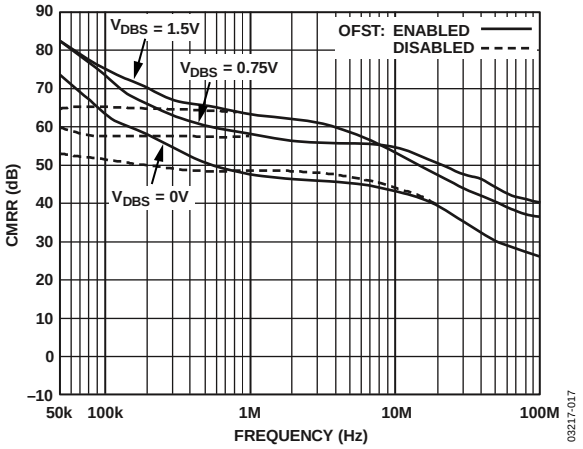

Figure 16. CMRR vs. Frequency

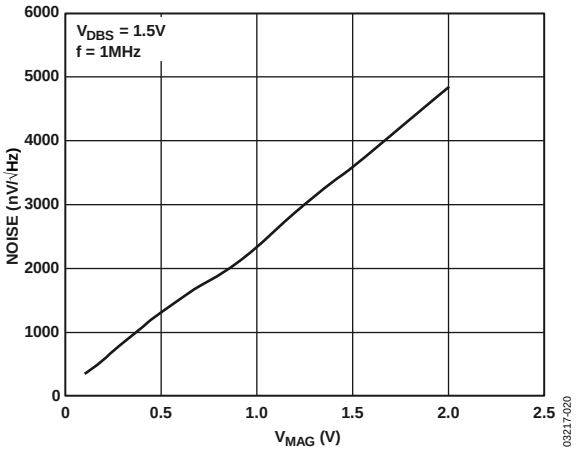

Figure 19. Output Referred Noise vs. V_{MAG}

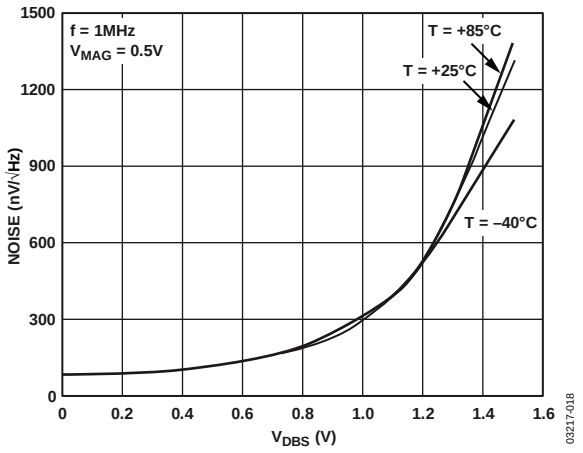

Figure 17. Output Referred Noise vs. V_{DBS} for Three Temperatures

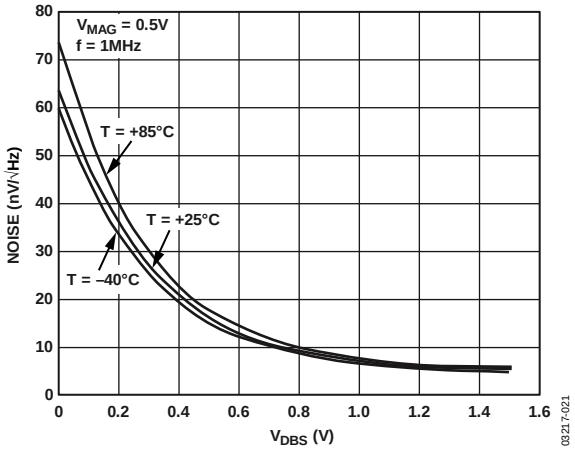

Figure 20. Input Referred Noise vs. V_{DBS} for Three Temperatures

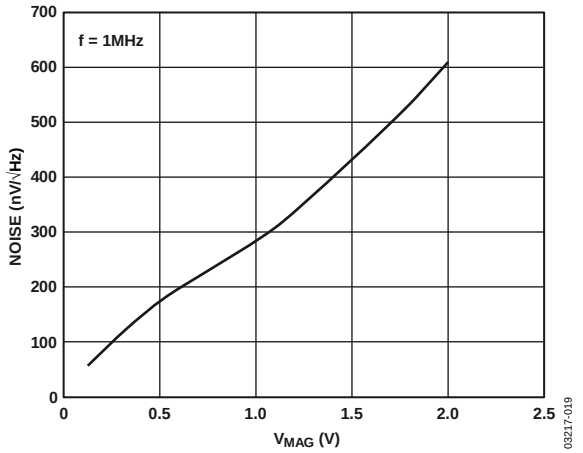

Figure 18. Output Referred Noise vs. V_{MAG}, V_{DBS} = 0.75 V

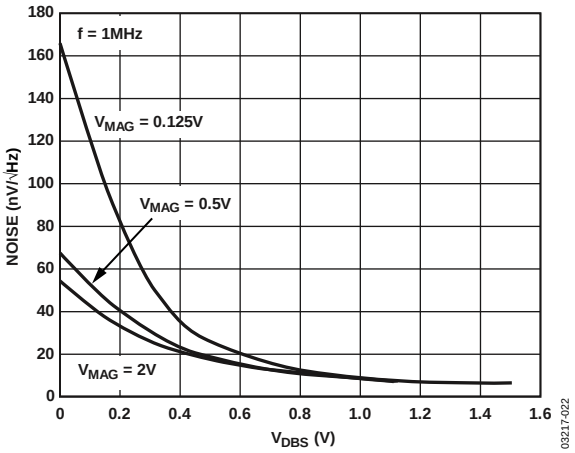

Figure 21. Input Referred Noise vs. V_{DBS} for Three Values of V_{MAG}

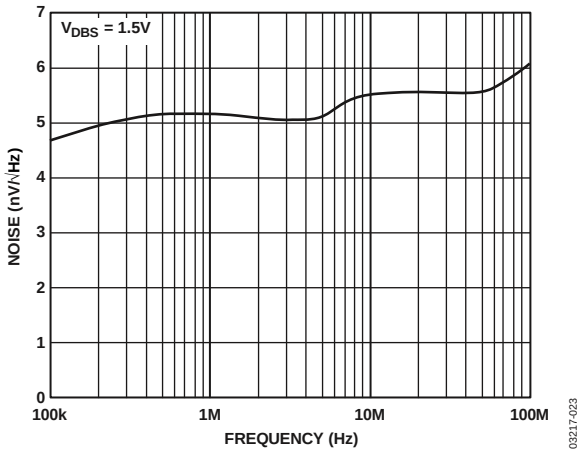

Figure 22. Input Referred Noise vs. Frequency

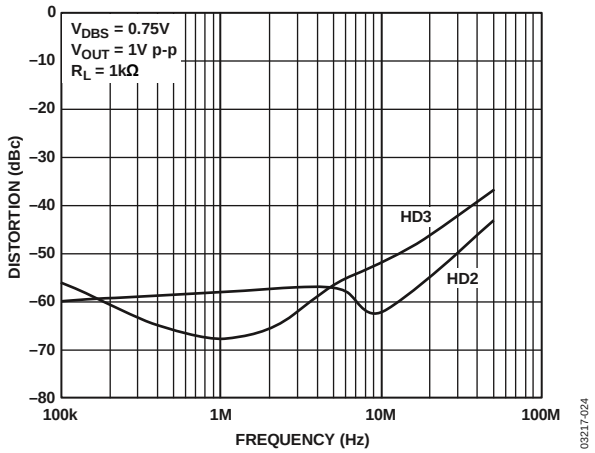

Figure 23. Harmonic Distortion vs. Frequency

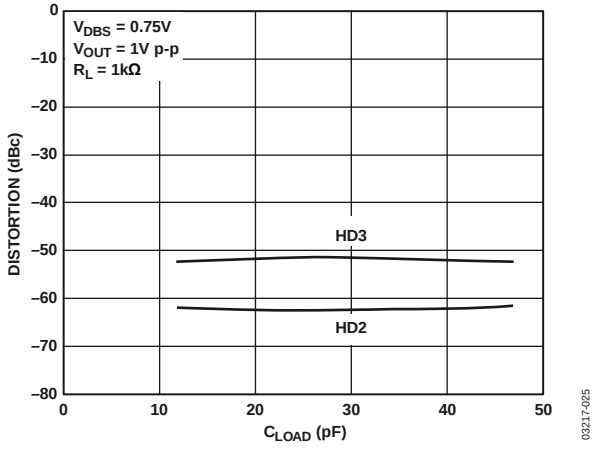

Figure 24. Harmonic Distortion vs. C_{LOAD}

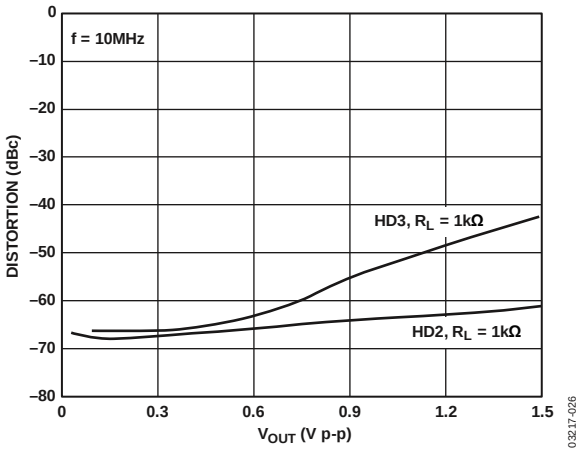

Figure 25. Harmonic Distortion vs. V_{OUT}, V_{MAG} = 0.5 V

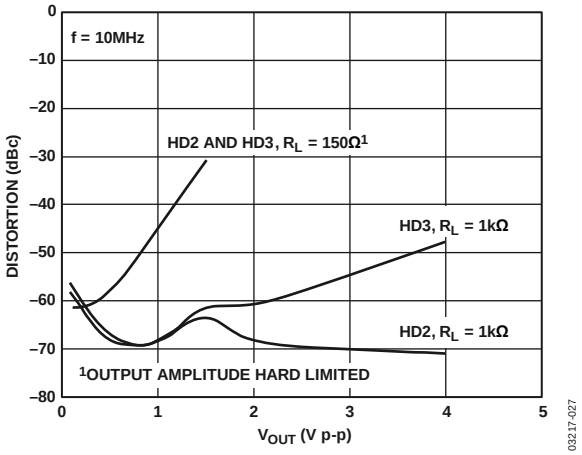

Figure 26. Harmonic Distortion vs. V_{OUT}, V_{MAG} = 2.0 V

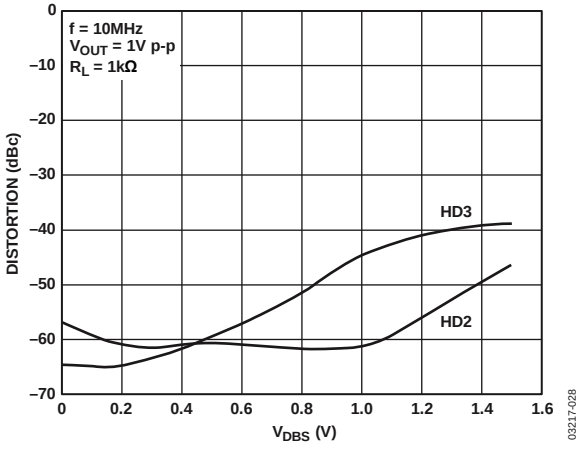

Figure 27. Harmonic Distortion vs. V_{DBS}

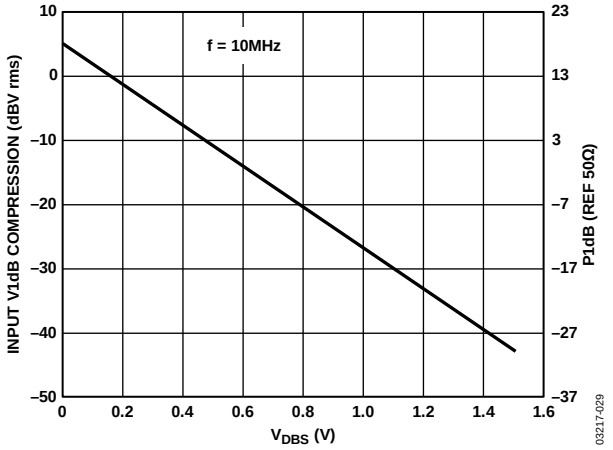

Figure 28. Input V1dB Compression vs. V_{DBS}

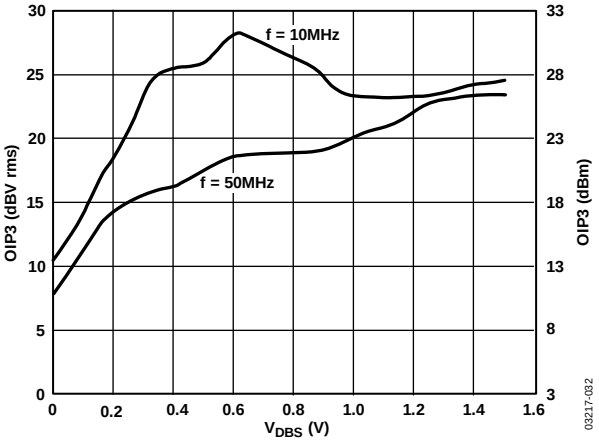

Figure 31. OIP3 vs. V_{DBS}

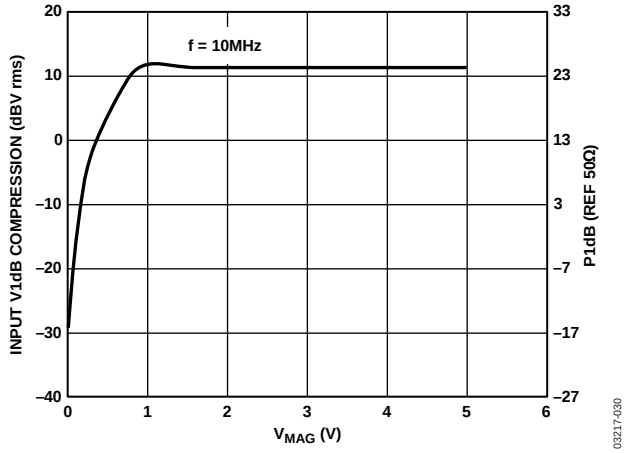

Figure 29. Output V1dB Compression vs. V_{MAG}

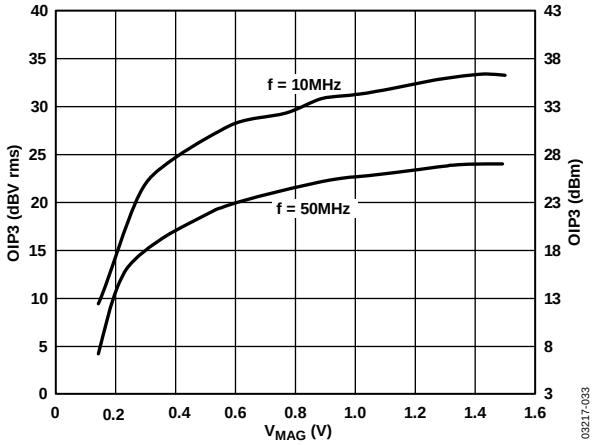

Figure 32. OIP3 vs. V_{MAG}

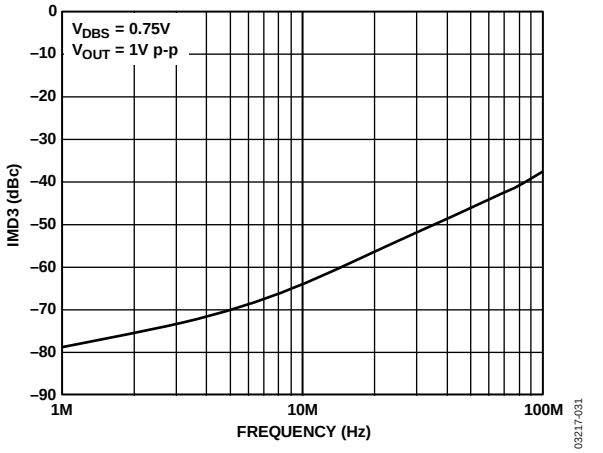

Figure 30. IMD3 Distortion vs. Frequency

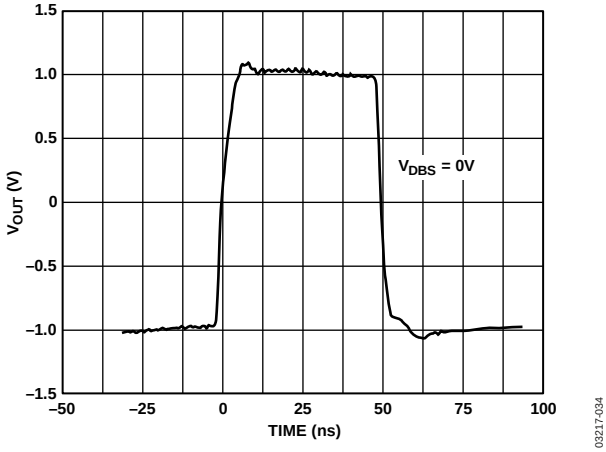

Figure 33. Full-Scale Transient Response, V_{DBS} = 0 V

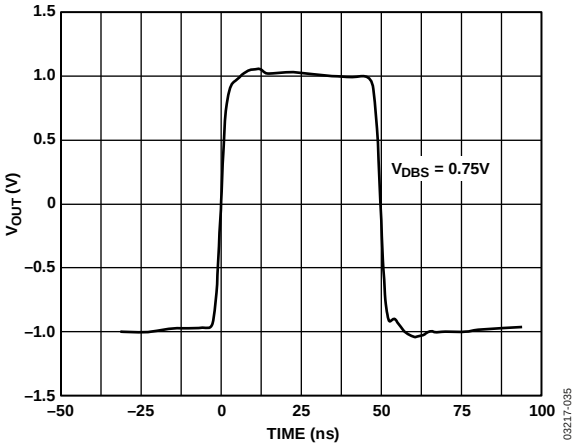

Figure 34. Full-Scale Transient Response, V_{DBS} = 0.75 V, f = 1 MHz, V_{OUT} = 2 V p-p

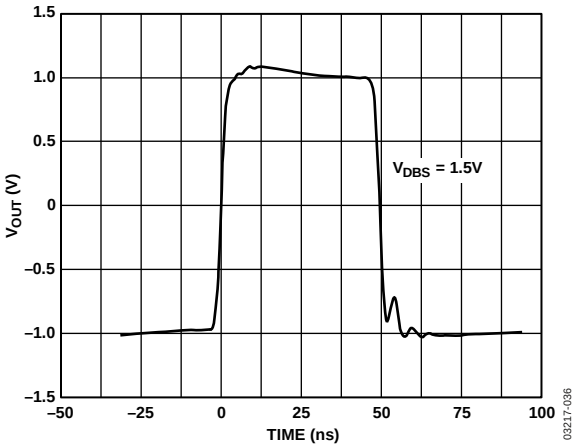

Figure 35. Full-Scale Transient Response, V_{DBS} = 1.5 V, f = 1 MHz, V_{OUT} = 2 V p-p

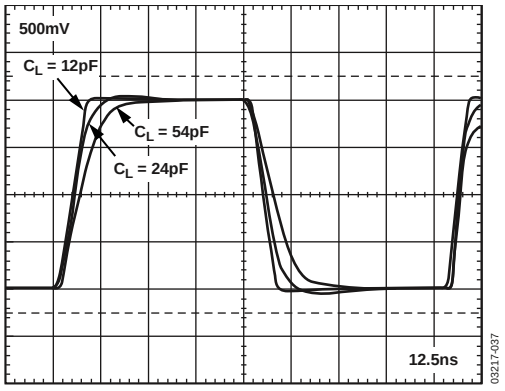

Figure 36. Transient Response vs. Various Load Capacitances, G = 25 dB

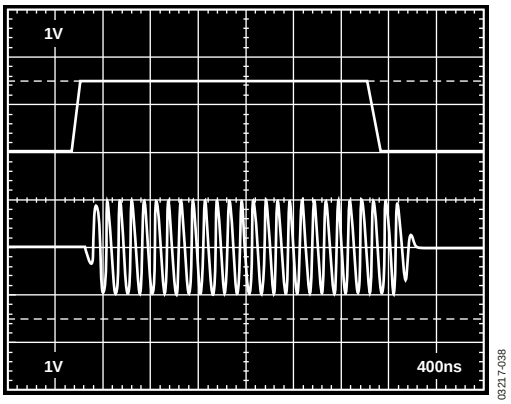

Figure 37. V_{DBS} Interface Response, Top: V_{DBS}, Bottom: V_{OUT}

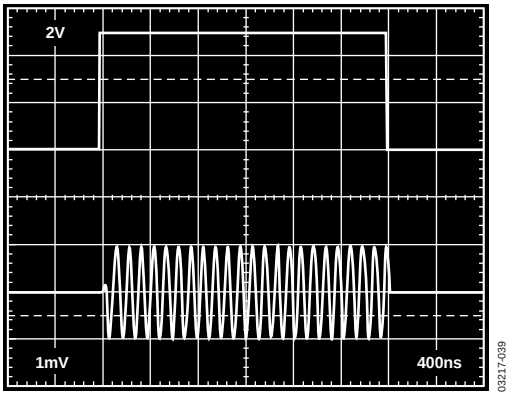

Figure 38. V_{MAG} Interface Response, Top: V_{MAG}, Bottom: V_{OUT}

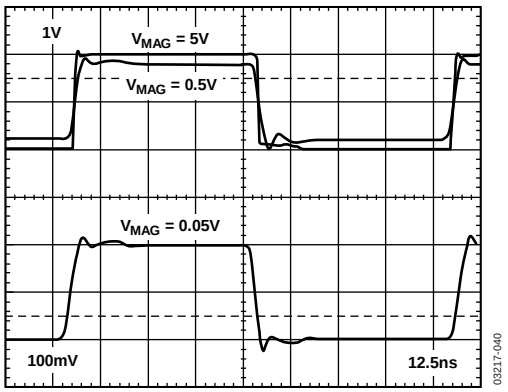

Figure 39. Transient Response vs. V_{MAG}

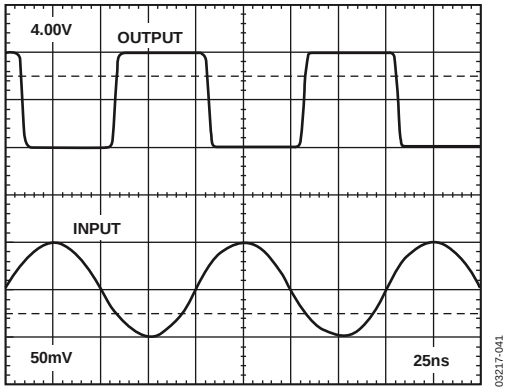

Figure 40. Overdrive Response, V_{DBS} = 1.5 V, V_{MAG} = 0.5 V, 18.5 dB Overdrive

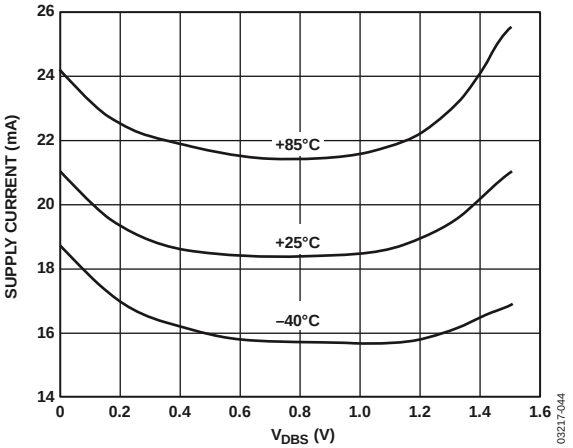

Figure 43. Supply Current vs. V_{DBS} at Three Temperatures

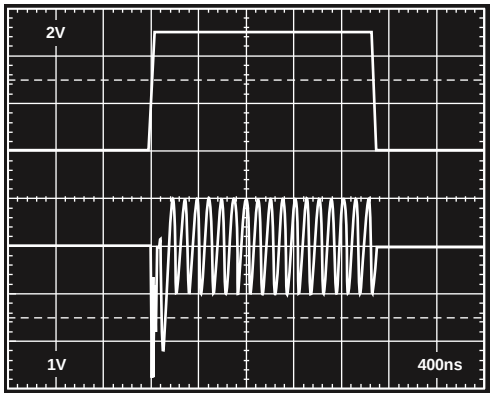

Figure 41. ENBL Interface Response. Top: V_{ENBL}; Bottom: V_{OUT}, f = 10 MHz

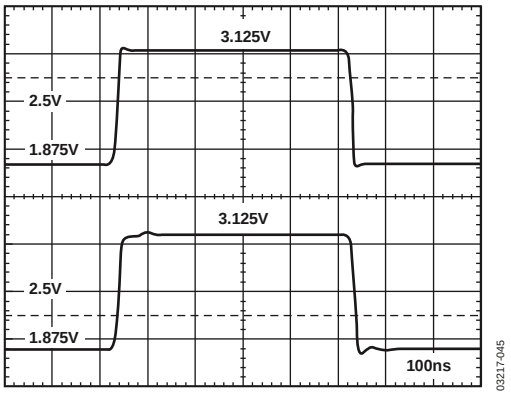

Figure 44. CNTR Transient Response, Top: Input to CNTR, Bottom: V_{OUT} Single-Ended

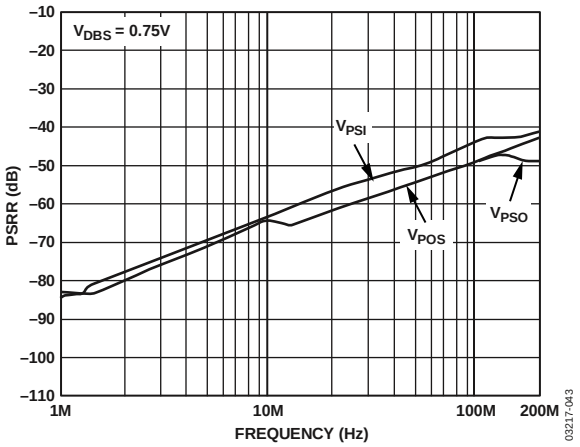

Figure 42. PSRR vs. Frequency

THEORY OF OPERATION

CIRCUIT DESCRIPTION

Many monolithic variable gain amplifiers use techniques that share common principles that are broadly classified as translinear. This term refers to circuit cells whose functions depend directly on the very predictable properties of bipolar junction transistors, notably the linear dependence of their transconductance on collector current. Since the discovery of these cells in 1967, and their commercial exploitation in products developed during the early 1970s, accurate wide bandwidth analog multipliers, dividers, and variable gain amplifiers have invariably employed translinear principles.

Although these techniques are well understood, the realization of a high performance variable gain amplifier (VGA) requires special technologies and attention to many subtle details in its design. The AD8330 is fabricated on a proprietary silicon-on-insulator, complementary bipolar IC process and draws on decades of experience in developing many leading edge products using translinear principles to provide an unprecedented level of versatility.

Figure 45 shows a basic representative cell comprising just four transistors. This, or a very closely related form, is at the heart of most translinear multipliers, dividers, and VGAs. The key concepts are as follows:

First, the ratio of the currents in the left-hand and right-hand pairs of transistors is identical, represented by the modulation factor, x, with values between −1 and +1. Second, the input signal is arranged to modulate the fixed tail current, I_D, to cause the variable value of x, introduced in the left-hand pair, to be replicated in the right-hand pair, and, thus, generate the output by modulating its nominally fixed tail current, I_N. Third, the current gain of this cell is exactly $G = I_N/I_D$ over many decades of variable bias current.

In practice, the realization of the full potential of this circuit involves many other factors, but these three elementary ideas remain essential.

By varying I_N, the overall function is that of a two-quadrant analog multiplier, exhibiting a linear relationship to both the signal modulation factor (x) and this numerator current. On the other hand, by varying I_D, a two-quadrant analog divider is realized, having a hyperbolic gain function with respect to the input factor, x, controlled by this denominator current. The AD8330 exploits both modes of operation. However, because a hyperbolic gain function is generally of less value than one in which the decibel gain is a linear function of a control input, a special interface is included to provide either increasing or decreasing exponential control of I_D.

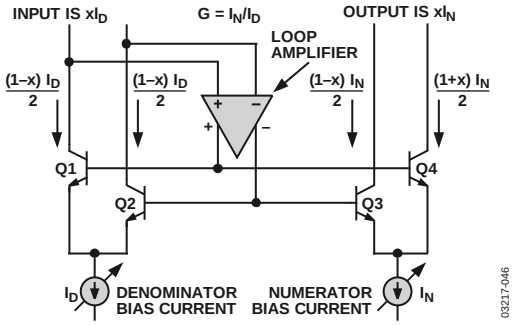

Figure 45. Basic Core

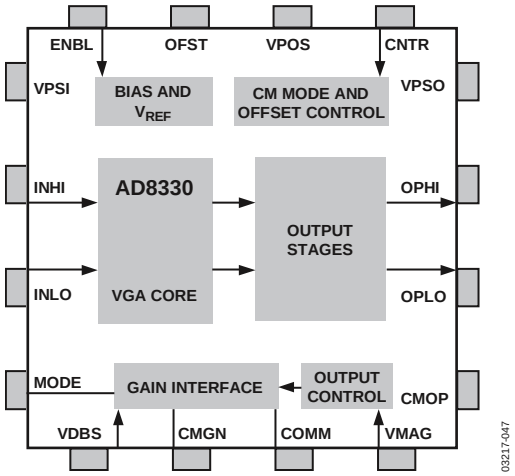

Figure 46. Block Schematic

Overall Structure

Figure 46 shows a block schematic of the AD8330 locating the key sections. More detailed descriptions of its structure and features are provided throughout the Theory of Operation section; however, Figure 46 provides a general overview of its capabilities.

The VGA core contains a more elaborate version of the cell shown in Figure 45. The current, I_D, is controlled exponentially (linear-in-decibels) through the decibel gain interface at Pin VDBS and its local common, Pin CMGN. The gain span (that is, the decibel difference between maximum and minimum values) provided by this control function is slightly more than 50 dB. The absolute gain from input to output is a function of source and load impedance, and depends on the voltage on a second gain control pin (VMAG), explained in the Normal Operating Conditions section.

Normal Operating Conditions

To minimize confusion, normal operating conditions are defined as follows:

The input pins are voltage driven (the source impedance is assumed to be zero).

The output pins are open circuited (the load impedance is assumed to be infinite).

Pin VMAG is unconnected setting up the output bias current (I_N in the four-transistor gain cell) to its nominal value.

Pin CMGN is grounded.

MODE is either tied to a logic high or left unconnected, to set the up gain mode.

The effects of other operating conditions are considered separately.

Throughout this data sheet, the end-to-end voltage gain for the normal operating conditions is referred to as the basic gain. Under these conditions, it runs from 0 dB when V_{DBS} = 0 V (where this voltage is more exactly measured with reference to Pin CMGN, which is not necessarily tied to ground) up to 50 dB for V_{DBS} = 1.5 V. The gain does not fold over when the VDBS pin is driven below ground or above its nominal full-scale value.

The input is accepted at the INHI/INLO differential port. These pins are internally biased to roughly the midpoint of the supply, V_S (it is actually ~2.75 V for V_S = 5 V, V_{DBS} = 0 V, and 1.5 V for V_S = 3 V), but the AD8330 is able to accept a forced common-mode value, from zero to V_S, with certain limitations. This interface provides good common-mode rejection up to high frequencies (see Figure 16) and, thus, can be driven in either a single-sided or differential manner. However, operation using a differential drive is preferable, and this is assumed in the specifications, unless otherwise stated.

The pin-to-pin input resistance is specified as 950 Ω ± 20%. The driving-point impedance of the signal source can range from zero up to values considerably in excess of this resistance, with a corresponding variation in noise figure (see Figure 53). In most cases, the input is coupled via two capacitors, chosen to provide adequate low frequency transmission. This results in the minimum input noise that increases when some other common-mode voltage is forced onto these pins. The short-circuit, input-referred noise at maximum gain is approximately 5 nV/√Hz.

Output Pin OPHI and Output Pin OPLO operate at a common-mode voltage at the midpoint of the supply, $V_S/2$, within a few millivolts. This ensures that an analog-to-digital converter (ADC) attached to these outputs operates within the often narrow range permitted by their design. When a common-mode voltage other than $V_S/2$ is required at this interface, it can easily be forced by applying an externally provided voltage to the output centering pin, CNTR. This voltage can run from zero to the full supply, though the use of such extreme values leaves only a small range for the differential output signal swing.

The differential impedance measured between OPHI and OPLO is 150 Ω ± 20%. It follows that both the gain and the full-scale voltage swing depend on the load impedance; both are nominally halved when this is also 150 Ω. A fixed impedance output interface, rather than an op amp style voltage-mode output, is preferable in high speed applications because the effects of complex reactive loads on the gain and phase can be better controlled. The top end of the AD8330 ac response is optimally flat for a 12 pF load on each pin, but this is not critical, and the system remains stable for any value of load capacitance including zero.

Another useful feature of this VGA in connection with the driving of an ADC is that the peak output magnitude can be precisely controlled by the voltage on Pin VMAG. Usually, this voltage is internally preset to 500 mV, and the peak differential unloaded output swing is ±2 V ± 3%. However, any voltage from zero to at least 5 V can be applied to this pin to alter the peak output in an exactly proportional way. Because either output pin can swing rail-to-rail, which in practice means down to at least 0.35 V and to within the same voltage below the supply, the peak-to-peak output between these pins can be as high as 10 V using V_S = 6 V.

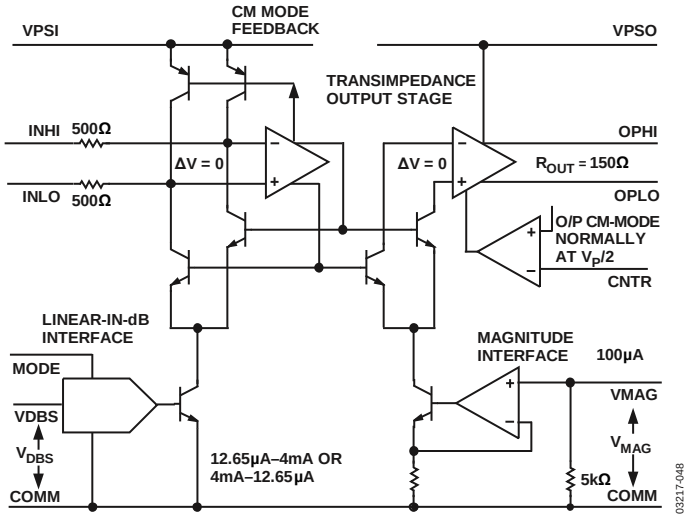

Figure 47. Schematic of Key Components

Linear-in-dB Gain Control (V_{DBS})

All Analog Devices, Inc., VGAs featuring a linear-in-dB gain law, such as the X-AMP® family, provide exact, constant gain scaling over the fully specified gain range, and the deviation from the ideal response is within a small fraction of a dB. For the AD8330, the scaling of both of its gain interfaces is substantially independent of process, supply voltage, or temperature. The basic gain, G_B, is simply

$$G_B(dB) = \frac{V_{DBS}}{30\text{ mV}} \quad (1)$$

where V_{DBS} is in volts.

Alternatively, this can be expressed as a numerical gain magnitude

$$G_{BN} = 10^{\frac{V_{DBS}}{0.6\ V}} \quad (2)$$

The gain can be increased or decreased by changing the voltage, V_{MAG}, applied to the VMAG pin. The internally set default value of 500 mV is derived from the same band gap reference that determines the decibel scaling. The tolerance on this voltage, and mismatches in certain on-chip resistors, cause small gain errors (see the Specifications section). Though not all applications of VGAs demand accurate gain calibration, it is a valuable asset in many situations, for example, in reducing design tolerances.

Figure 47 shows the core circuit in more detail. The range and scaling of V_{DBS} is independent of the supply voltage, and the gain control pin, VDBS, presents a high incremental input resistance (~100 MΩ) with a low bias current (~100 nA), making the AD8330 easy to drive from a variety of gain control sources.

Inversion of the Gain Slope

The AD8330 supports many features that further extend the versatility of this VGA in wide bandwidth gain control systems. For example, the logic pin, MODE, allows the slope of the gain function to be inverted, so that the basic gain starts at +50 dB for a gain voltage, V_{DBS}, of zero and runs down to 0 dB when this voltage is at its maximum specified value of 1.5 V. The basic forms of these two gain control modes are shown in Figure 48.

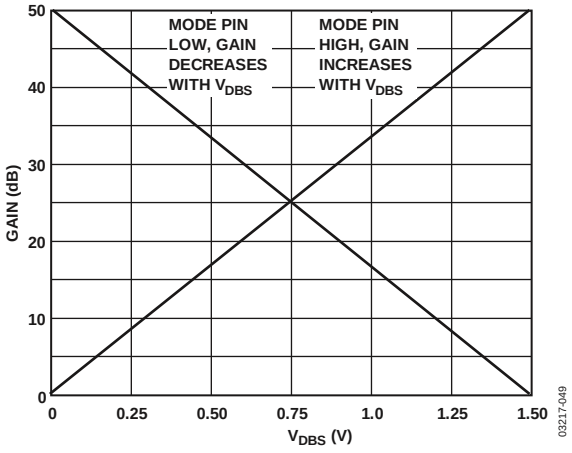

Figure 48. Two Gain Directions of the AD8330

Gain Magnitude Control (V_{MAG})

In addition to the basic linear-in-dB control, two more gain control features are provided. The voltage applied to Pin VMAG provides accurate linear-in-magnitude gain control with a very rapid response. The bandwidth of this interface is >100 MHz. When this pin is unconnected, V_{MAG} assumes its default value of 500 mV (see Figure 47) to set up the basic 0 dB to 50 dB range. However, any voltage from ~15 mV to 5 V can be applied either to lower the gain by up to 30 dB or to raise it by 20 dB. The combined gain span is thus 100 dB, that is, the 50 dB basic gain span provided by V_{DBS} plus a 60 dB linear-in-magnitude span provided by V_{MAG}. The latter modifies the basic numerical gain G_{BN} to generate a total gain, expressed here in magnitude terms.

$$G_T = G_{BN}\frac{V_{MAG}}{0.5\ \text{V}} \quad (3)$$

Using this to calculate the output voltage,

$$V_{OUT} = 2 \times G_{IN} \times V_{IN} \times V_{MAG} \quad (4)$$

from which it is apparent that the AD8330 implements a linear, two-quadrant multiplier with a bipolar V_{IN} and a unipolar V_{MAG}. Because the AD8330 is a dc-coupled system, it can be used in many applications where a wideband two-quadrant multiplier function is required, from dc up to about 100 MHz from either input (V_{IN} or V_{MAG}).

As V_{MAG} is varied, so also is the peak output magnitude, up to a point where this is limited by the absolute output limit imposed by the supply voltage. In the absence of the latter effect, the peak output into an open-circuited load is just

$$V_{OUT\_PK} = \pm 4\ V_{MAG} \quad (5)$$

whereas for a load resistance of R_L directly across OPHI and OPLO, it is

$$V_{OUT\_PK} = \frac{\pm 2\ V_{MAG} R_L}{(R_L + 150)} \quad (6)$$

These capabilities are illustrated in Figure 49, where V_S = 6 V, R_L = O/C, V_{DBS} = 0 V, V_{IN} is swept from −2.5 V dc to +2.5 V dc, and V_{MAG} is set to 0.25 V, 0.5 V, 1 V, and 2 V. Except for the last value of V_{MAG}, the peak output follows Equation 5. This exceeds the supply-limited value when V_{MAG} = 2 V and the peak output is ±5.65 V, that is, ±6 V − 0.35 V. Figure 50 demonstrates the high speed multiplication capability. The signal input is a 100 MHz, 0.1 V sine wave, V_{DBS} is set to 0.6 V, and V_{MAG} is a square wave at 5 MHz alternating from 0.25 V to 1 V. The output is ideally a sine wave switching in amplitude between 0.5 V and 2 V.

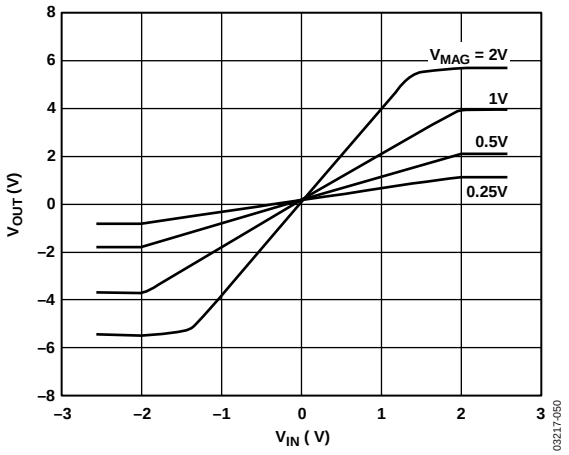

Figure 49. Effect of V_{MAG} on Gain and Peak Output

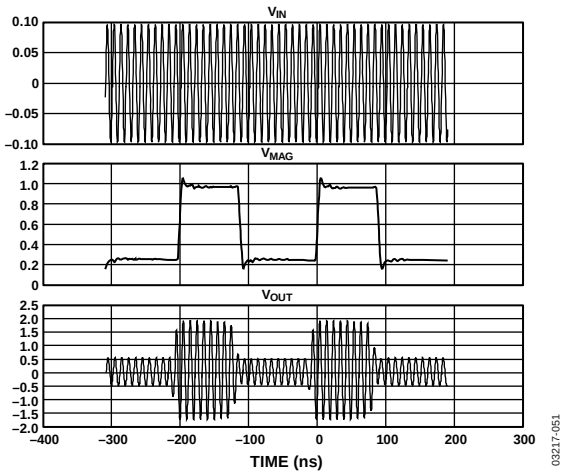

Figure 50. Using VMAG in Modulation Mode

Another gain related feature allows both gain control ranges to be accurately raised by 200 mV. To enable this offset, open circuit CMGN (Pin 6, LFCSP; Pin 8, LQFP) and add a 0.1 µF capacitor to ground. In use, the nominal range for V_{DBS} extends from 0.2 V to 1.7 V and V_{MAG} from 0.2 V to 5.2 V. These specifications apply for any supply voltage. This allows the use of DACs whose output range does not include ground as sources for the gain control function(s).

Note that the 200 mV that appears on this pin affects the response to an externally applied V_{MAG}, but when Pin VMAG is unconnected, the internally set default value of 0.5 V still applies. Furthermore, Pin CMGN can, if desired, be driven by a user-supplied voltage to reposition the baseline for V_{DBS} (or for an externally applied V_{MAG}) to any other voltage up to 500 mV. In all cases, the gain scaling, its law conformance, and temperature stability are unaffected.

Two Classes of Variable Gain Amplifiers

Note that there are two broad classes of VGAs. The first type is designed to cope with a very wide range of input amplitudes and, by virtue of its gain control function, compress this range down to an essentially constant output. This is the function needed in an AGC system. Such a VGA is called an IVGA, referring to a structure optimized to address a wide range of input amplitudes. By contrast, an OVGA is optimized to deliver a wide range of output values while operating with an essentially constant input amplitude. This function might be needed, for example, in providing a variable drive to a power amplifier.

It is apparent from the foregoing sections that the AD8330 is both an IVGA and an OVGA in one package. This is an unusual and possibly confusing degree of versatility for a VGA; therefore, these two distinct control functions are described at separate points throughout this data sheet to explain the operation and applications of this product. It is, nevertheless, useful to briefly describe the capabilities of these features when used together.

Amplitude/Phase Response

The ac response of the AD8330 is remarkably consistent not only over the full 50 dB of its basic gain range, but also with changes of gain due to alteration of V_{MAG}, as demonstrated in Figure 51. This is an overlay of two sets of results: first, with a very low V_{MAG} of 16 mV that reduces the overall gain by 30 dB [20 × log10(500 mV/16 mV)]; second, with V_{MAG} = 5 V that increases the gain by 20 dB = 20 × log10(5 V/0.5 V).

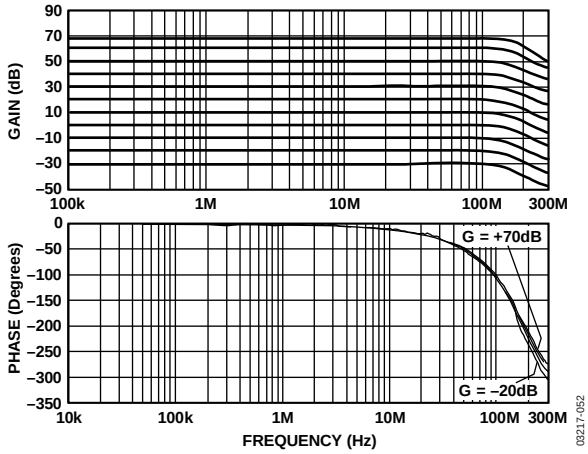

Figure 51. AC Performance over a 100 dB Gain Range Obtained by Using Two Values of V_{MAG}

This 50 dB step change in gain produces two sets of gain curves, having a total gain span of 100 dB. It is apparent that the amplitude and phase response are essentially independent of the gain over this wide range, an aspect of the AD8330 performance potential unprecedented in any prior VGA.

It is unusual for an application to require such a wide range of gains; and, as a practical matter, the peak output voltage for V_{MAG} = 16 mV is reduced by the factor 16/500, compared to its nominal value of ±2 V, to only ±64 mV. As previously noted, most applications of VGAs require that they operate in a mode that is predominantly of either an IVGA or OVGA style, rather than mixed modes.

With this limitation in mind, and simply to illustrate the unusual possibilities afforded by the AD8330, note that, with appropriate drive to V_{DBS} and V_{MAG} in tandem, the gain span is a remarkable 120 dB, extending from −50 dB to +70 dB, as shown in Figure 52 for operation at 1 MHz and 100 MHz. In this case, V_{DBS} and V_{MAG} are driven from a common control voltage, V_{GAIN}, that varies from 1.2 mV to 5 V, with 30% (1.5/5) of V_{GAIN} applied to V_{DBS}, and 100% applied to V_{MAG}.

The gain varies in a linear-in-dB manner with V_{DBS}, although the response from V_{MAG} is linear-in-magnitude. Consequently, the overall numerical gain as the product of these two functions is

$$GAIN = V_{GAIN} / 0.5\ \text{V} \times 0.3 \times 10^{\frac{V_{GAIN}}{0.6\ \text{V}}} \quad (7)$$

In rare cases where such a wide gain range is of value, the calibration is still accurate and the temperature is stable.

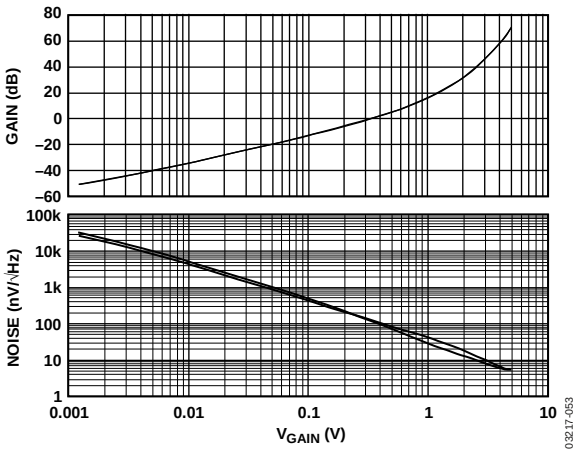

Figure 52. Gain Control Function and Input Referred Noise Spectral Density over a 120 dB Range

Noise, Input Capacity, and Dynamic Range

The design of variable gain amplifiers invariably incurs some compromises in noise performance. However, the structure of the AD8330 is such that this penalty is minimal. Examination of the simplified schematic (Figure 47) shows that the input voltage is converted to current-mode form by the two 500 Ω resistors at Pin INHI and Pin INLO, whose combined Johnson noise contributes 4.08 nV/√Hz. The total input noise at full gain, when driven from a low impedance source, is typically 5 nV/√Hz after accounting for the voltage and current noise contributions of the loop amplifier. For a 200 kHz channel bandwidth, this amounts to 2.24 μV rms. The peak input at full gain is ±6.4 mV, or +4.5 mV rms for a sine wave signal. The signal-to-noise ratio at full input, that is, the dynamic range, for these conditions is, thus, 20 log10(4.5 mV/2.24 μV), or 66 dB. The value of V_{MAG} has essentially no effect on the input referred noise, but it is assumed to be 0.5 V.

Below midgain (25 dB, V_{DBS} = 0.75 V), noise in the output section dominates, and the total input noise is 11 nV/√Hz, or 4.9 μV rms in a 200 kHz bandwidth, and the peak input is 78 mV rms. Thus, the dynamic range increases to 84 dB. At minimum gain, the input noise is up to 120 nV/√Hz, or 53.7 mV rms in the assumed 200 kHz bandwidth, while the input capacity is ±2 V, or +1.414 V rms (sine), a dynamic range of 88.4 dB. In calculating the dynamic range for other channel bandwidths, Δf, subtract 10 log10(Δf/200 kHz) from these illustrative values. A system operating with a 2 MHz bandwidth, for example, exhibits dynamic range values that are uniformly 10 dB lower; used in an audio application with a 20 kHz bandwidth, they are 10 dB higher.

Noise figure is a misleading metric for amplifiers that are not impedance matched at their input, which is the special condition resulting only when both the voltage and current components of a signal, that is, the signal power, are used at the input port. When a source of impedance (R_S) is terminated using a resistor of R_S (a condition that is not to be confused with matching), only one of these components is used, either the current (as in the AD8330) or the voltage. Then, even if the amplifier is perfect, the noise figure cannot be better than 3 dB. The 1 kΩ internal termination resistance would result in a minimum noise figure of 3 dB for an R_S of 1 kΩ if the amplifier were noise-free. However, this is not the case, and the minimum noise figure occurs at a slightly different value of R_S (for an example, see Figure 53 and the Using the AD8330 section).

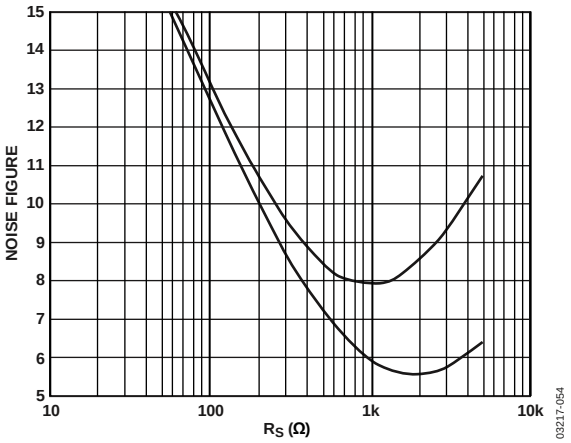

Figure 53. Noise Figure for Source Resistance of 50 Ω to 5 kΩ, at f = 10 MHz (Lower) and 100 MHz (Simulation)

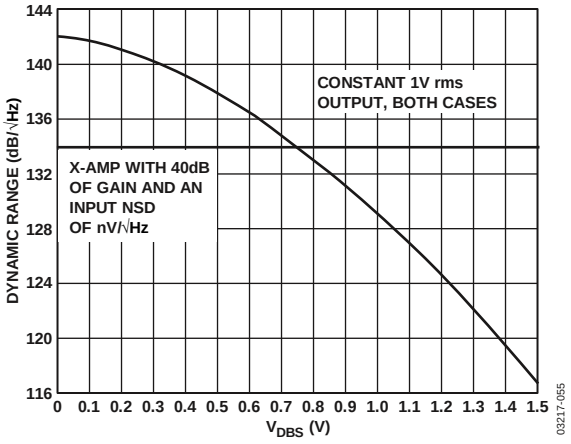

Figure 54. Dynamic Range in dB/√Hz vs. V_{DBS} (V_{MAG} = 0.5 V, 1 V rms Output) Compared with a Representative X-AMP (Simulation)

Dynamic Range

The ratio of peak output swing, expressed in rms terms, to the output-referred noise spectral density provides a measure of dynamic range, in dB/√Hz. For a certain class of variable gain amplifiers, exemplified by the Analog Devices X-AMP® family, the dynamic range is essentially independent of the gain setting because the peak output swing and noise are both constant. The AD8330 provides a different dynamic range profile because there is no longer a constant relationship between these two parameters. Figure 54 compares the dynamic range of the AD8330 to a representative X-AMP.

Input Common-Mode Range and Rejection Ratio

Input Pin INHI and Pin INLO should be ac-coupled in most applications to achieve the stated noise performance. In general, when direct coupling is used, care must be taken in setting the dc voltage level at these inputs, and particularly when minimizing noise is critical. This objective is complicated by the fact that the common-mode level varies with the basic gain voltage, V_{DBS}. Figure 55 shows this relationship for a supply voltage of 5 V, for temperatures of −40°C, +25°C, and +85°C. Figure 56 shows the input noise spectral density (R_S = 0) vs. the input common-mode voltage, for V_{DBS} = 0.5 V, 0.6 V, 0.75 V, and 1.5 V. It is apparent that there is a broad range over which the noise is unaffected by this dc level. The input CMRR is excellent (see Figure 16).

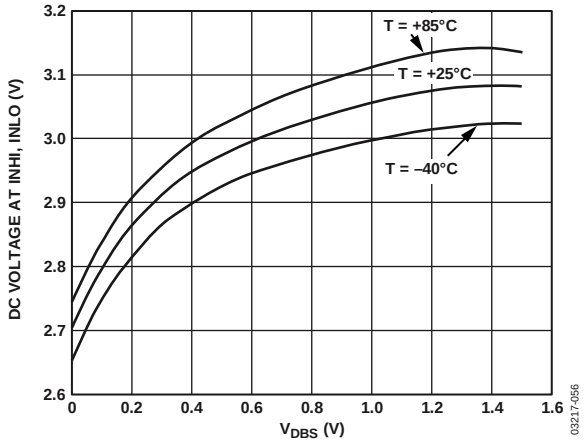

Figure 55. Common-Mode Voltage at Input Pins vs. V_{DBS}, for V_S = 5 V, T = −40°C, + 25°C, and + 85°C

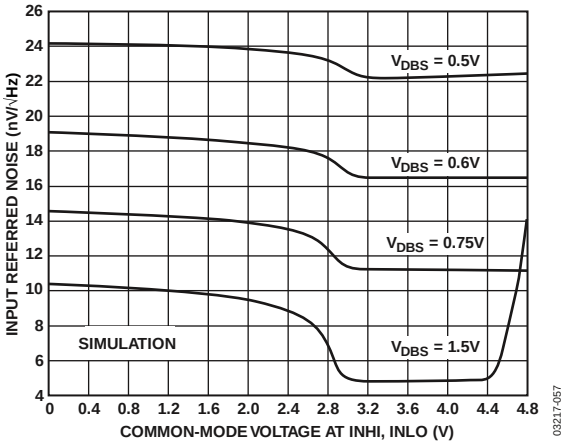

Figure 56. Input Noise vs. Common-Mode Input Voltage for V_{DBS} = 0.5 V, 0.6 V, 0.75 V, and 1.5 V

Output Noise and Peak Swing

The output noise of the AD8330 is the input noise multiplied by the overall gain, including any optional change to the voltage, V_{MAG}, applied to Pin VMAG. The peak output swing is also proportional to this voltage, which, at low gains and high values of V_{MAG}, affects the output noise.

The scaling for V_{DBS} = 0 V is as follows:

$$V_{OUT\_PK} = \pm 4\ V_{MAG} \quad (8)$$

$$V_{NOISE\_OUT} = (85 + 70\ V_{MAG})\ \text{nV}/\sqrt{\text{Hz}} \quad (9)$$

For example, using a reduced value of V_{MAG} = 0.25 V that lowers all gain values by 6 dB, the peak output swing is ±1 V (differentially) and the output noise spectral density evaluates to 102.5 nV/√Hz. The peak output swing is no different at full gain, but the noise becomes

$$V_{NOISE\_OUT} = (0.1 + 0.32\ V_{MAG})\ \mu\text{V}/\sqrt{\text{Hz}} \quad (10)$$

for R_S = 0 and V_{DBS} = 1.5 V, assuming an input noise of 5 nV/√Hz. The output noise for very small values of V_{MAG} (at or below 15 mV) is not precise, partly because the small input offset associated with this interface has a large effect on the gain.

Offset Compensation

The AD8330 includes an offset compensation feature that is operational in the default condition (no connection to Pin OFST). This loop introduces a high-pass filter function into the signal path, whose −3 dB corner frequency is at

$$f_{HPF} = \frac{1}{(2\pi R_{INT} C_{HP})} \quad (11)$$

where:
C_{HP} is the external capacitance added from OFST to CNTR.
R_{INT} is an internal resistance of approximately 480 Ω, having a maximum uncertainty of about ±20%.

This evaluates to

$$f_{HPF} = \frac{330\,\mu}{C_{HP}}\ (C_{HP}\ \text{in}\ \mu\text{F}) \quad (12)$$

A small amount of peaking at this corner when using small capacitor values can be avoided by adding a series resistor. Useful combinations are C_{HP} = 3 nF, R_{HP} = 180 Ω, f = 100 kHz; C_{HP} = 33 nF, R_{HP} = 10 Ω, f = 10 kHz; C_{HP} = 0.33 µF, R_{HP} = 0 Ω, f = 1 kHz; C_{HP} = 3.3 µF, R_{HP} = 0 Ω, f = 100 Hz.

The offset compensation feature can be disabled simply by grounding the OFST pin. This provides a dc-coupled signal path, with no other effects on the overall ac response. Input offsets must be externally nulled in this mode of operation, as shown in Figure 58.

Effects of Loading on Gain and AC Response

The differential output impedance (R_O) is 150 Ω, and the frequency response of the output stage is optimized for operation with a certain load capacitance on each output pin (OPHI and OPLO) to ground, in combination with a load resistance (R_L) directly across these pins. In the absence of these capacitances, there is a small amount of peaking at the top extremity of the ac response. Suitable combinations are: $R_L = \infty$, C_L = 12 pF; R_L = 150 Ω, C_L = 25 pF; R_L = 75 Ω, C_L = 40 pF; or R_L = 50 Ω, C_L = 50 pF.

The gain calibration is specified for an open-circuited load, such as the high input resistance of an ADC. When resistively loaded, all gain values are nominally lowered as follows:

$$G_{LOADED} = \frac{G_{UNLOADED} R_L}{(150\ \Omega + R_L)} \quad (13)$$

Thus, when R_L = 150 Ω, the gain is reduced by 6 dB; for R_L = 75 Ω, the reduction is 9.5 dB; and for R_L = 50 Ω, it is 12 dB.

Gain Errors Due to On-Chip Resistor Tolerances

In all cases where external resistors are used, keep in mind that all on-chip resistances, including the R_O and the input resistance (R_I), are subject to variances of up to ±20%.

These variances need to be accounted for when calculating the gain with input and output loading. This sensitivity can be avoided by adjusting the source and load resistances to bear an inverse relationship as follows:

If $R_S = \alpha R_I$, then make $R_L = R_O/\alpha$; or,
if $R_L = \alpha R_O$, then make $R_S = R_I/\alpha$

The simplest case is when R_S = 1 kΩ and R_L = 150 Ω, therefore, the gain is 12 dB lower than the basic value. The reduction of peak swing at the load can be corrected by using V_{MAG} = 1 V, thereby restoring 6 dB of gain; using V_{MAG} = 2 V restores the full basic gain and doubles the peak available output swing.

Output (Input) Common-Mode Control

The output voltages are nominally positioned at the midpoint of the supply, $V_S/2$, over the range 2.7 V < V_S < 6 V, and this voltage appears at Pin CNTR, which is not normally expected to be loaded (the source resistance is ~4 kΩ). However, some circumstances require a small change in this voltage, and a resistor from CNTR to ground can lower this voltage, whereas a resistor to the supply raises it. On the other hand, this pin can be driven by an external voltage source to set the common-mode level to satisfy, for example, the needs of a following ADC. Any value from 0.5 V above ground to 0.5 V below the supply is permissible. Of course, when using an extreme common-mode level, the available output swing is limited, and it is recommended that a value equal or close to the default of $V_{CNTR} = V_S/2$ be used. There may be a few millivolts of offset between the applied voltage and the actual common-mode level at the output pins.

The input common-mode voltage, V_{CMI}, at Pin INHI and Pin INLO is slaved to the output, but with a shifted value of

$$V_{CMI} = 0.757\ V_{CNTR} + 1.12\ \text{V} \quad (14)$$

for V_{DBS} = 0.75 and T = 25°C. Thus, the default value for V_{CMI} when V_S = 5 V is 3.01 V (see Figure 55).

USING THE AD8330

This section describes a few general aspects of using the AD8330. Applying the AD8330 to a wide variety of circumstances requires very few precautions.

As in all high frequency circuits, careful observation of the ground nodes associated with each function is important. Three positive supply pins are provided: VPSI supports the input circuitry that often operates at a relatively high sensitivity; VPOS supports general bias sources and needs no decoupling; and VPSO biases the output stage where decoupling can be useful in maintaining a glitch-free output. Figure 57 shows the general case, where VPSI and VPSO are each provided with their own decoupling network, but this is not needed in all cases.

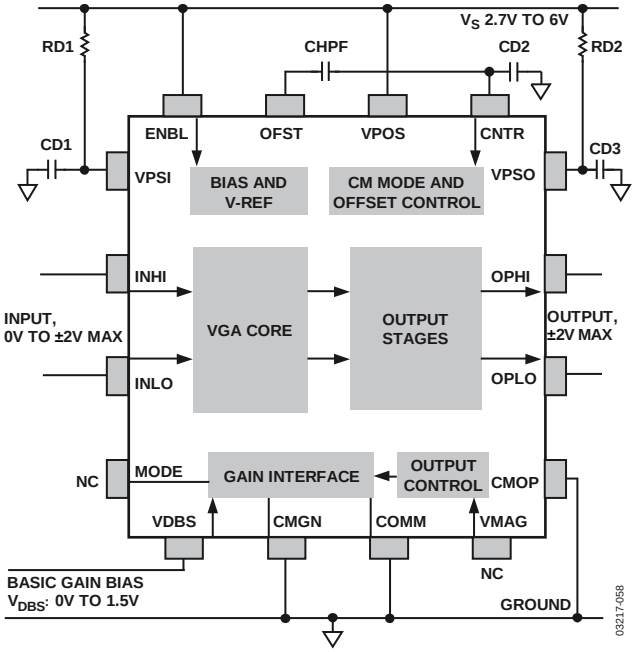

Figure 57. Power Supply Decoupling and Basic Connections

Because of the differential nature of the signal path, power supply decoupling is, in general, much less critical than in a single-sided amplifier; and where the minimization of board-level components is especially crucial, it is possible that these pins need no decoupling at all. On the other hand, when the signal source is single-sided, giving extra attention to the decoupling on Pin VPSI is sometimes required. Likewise, care is required in decoupling the VPSO pin if the output is loaded on only one of its two output pins. The general common (COMM) and the output stage common (CMOP) are usually grounded as shown in the Figure 57; however, the Applications section shows how a negative supply can optionally be used.

The AD8330 is enabled by taking the ENBL pin to a logical high (or, in all cases, the supply). The UP gain mode is enabled either by leaving the MODE pin unconnected or taking it to a logical high. When the opposite gain direction is needed, the MODE pin should be grounded or driven to a logical low. The low-pass corner of the offset loop is determined by Capacitor CHPF; this is preferably tied to the CNTR pin that in turn, should be decoupled to ground. The gain interface common pin (CMGN) is grounded, and the output magnitude control pin (VMAG) is left unconnected, or can optionally be connected to a 500 mV source for basic gain calibration.

Connections to the input and output pins are not shown in Figure 57 because of the many options that are available. When the AD8330 is used to drive an ADC, connect the OPHI and OPLO pins directly to the differential inputs of a suitable converter, such as an AD9214. If an adjustment is needed to this common-mode level, it can be introduced by applying that voltage to the CNTR pin, or, more simply, by using a resistor from this pin to either ground or the supply (see the Applications section). The CNTR pin can also supply the common-mode voltage to an ADC that supports such a feature.

When the loads to be driven introduce a dc resistive path to ground, coupling capacitors must be used. These should be of sufficient value to pass the lowest frequency components of the signal without excessive attenuation. Keep in mind that the voltage swing on such loads alternates both above and below ground, requiring that the subsequent component must be able to cope with negative signal excursions.

Gain and Swing Adjustments When Loaded

The output can also be coupled to a load via a transformer to achieve a higher load power by impedance transformation. For example, using a 2:1 turns ratio, a 50 Ω final load presents a 200 Ω load on the output. The gain loss (relative to the basic value with no termination) is 20 log10{(200+150)/200} or 4.86 dB, which can be restored by raising the voltage on the VMAG pin by a factor of $10^{4.86/20}$ or × 1.75, from its basic value of 0.5 V to 0.875 V. This also restores the peak swing at the 200 Ω level to ±2 V, or ±1 V into the 50 Ω final load.

Whenever a stable supply voltage is available, additional voltage swing can be provided by adding a resistor from the VMAG pin to the supply. The calculation is based on knowing that the internal bias is delivered via a 5 kΩ source; because an additional 0.375 V is needed, the current in this external resistor must be 0.375 V/5 kΩ = 75 µA. Thus, using a 5 V supply, a resistor of 5 V − 0.875 V/75 µA = 55 kΩ is used. Based on this example, the corrections for other load conditions are easy to calculate. If the effects on gain and peak output swing due to supply variations cannot be tolerated, VMAG must be driven by an accurate voltage.

Input Coupling

The dc common-mode voltage at the input pins varies with the supply, the basic gain bias, and temperature (see Figure 55); for this reason, many applications need to use coupling capacitors from the source that are large enough to support the lowest frequencies to be transmitted. Using one capacitor at each input pin, their minimum values can be readily found from the expression

$$C_{IN\_CPL} = \frac{320\ \mu F}{f_{HPF}} \quad (15)$$

where f_{HPF} is the −3dB frequency expressed in hertz. Thus, for an f_{HPF} of 10 kHz, 33 nF capacitors are used.

Occasionally, it is possible to avoid the use of coupling capacitors when the dc level of the driving source is within a certain range, as shown in Figure 56. This range extends from 3.5 V to 4.5 V when using a 5 V supply, and at high basic gains, where the effect of an incorrect dc level degrades the noise level due to internal aspects of the input stage. For example, suppose the driver, IC, is an LNA having an output topology in which its load resistors are taken to the supply, and the output is buffered by emitter followers. This presents a source for the AD8330 that can readily be directly coupled.

DC-Coupled Signal Path

In many cases, where the VGA is not required to provide its lowest noise, the full common-mode input range of zero to V_S can be used without problems, avoiding the need for any ac coupling means. However, such direct coupling at both the input and output does not automatically result in a fully dc-coupled signal path. The internal offset compensation loop must also be disengaged by connecting the OFST pin to ground. Keep in mind that at the maximum basic gain of 50 dB (×316), every millivolt of offset at the input, arising from whatever source, causes an output offset of 316 mV, which is an appreciable fraction of the peak output swing.

Because the offset correction loop is placed after the front-end variable gain sections of the AD8330, the most effective way of dealing with such offsets is at the input pins, as shown in Figure 58. For example, assume, for illustrative purposes, that the resistances associated with each side of the source in a certain application are 50 Ω. If this source has a very low (op amp) output impedance, the extra resistors should be inserted, with a negligible noise penalty and an attenuation of only 0.83 dB. The resistor values shown provide a trim range of about ±2 mV.

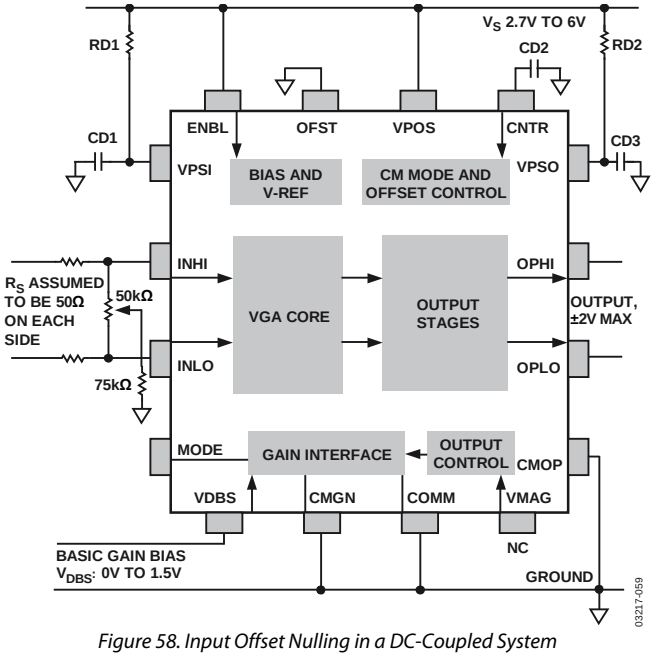

Figure 58. Input Offset Nulling in a DC-Coupled System

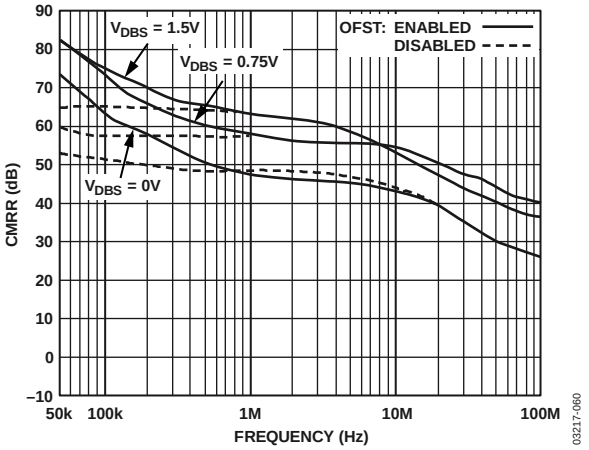

Figure 59. Input CMRR vs. Frequency for Various Values of V_{DBS}

Using Single-Sided Sources and Loads

Where the source provides a single-sided output, either INHI or INLO can be used for the input, with a polarity change when using INLO. The unused pin must be connected either through a capacitor to ground, or through a dc bias point that corresponds closely to the dc level on the active signal pin. The input CMRR over the full frequency range is illustrated in Figure 59. In some cases, an additional element such as a SAW filter (having a single-sided balanced configuration) or a flux-coupled transformer can be interposed. Where this element must be terminated in the correct impedance, other than 1 kΩ, it is necessary to add either shunt or series resistors at this interface.

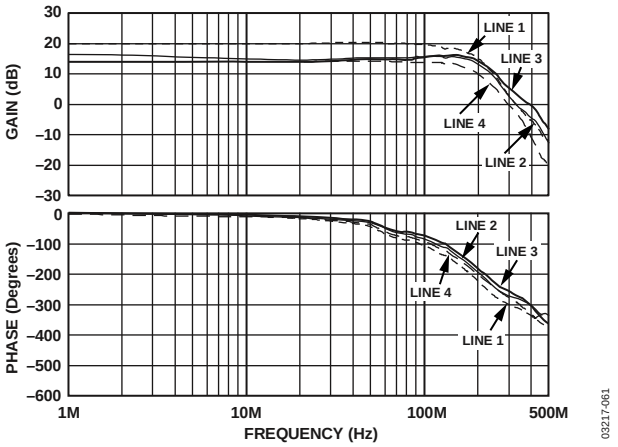

Figure 60. AC Gain and Phase for Various Loading Conditions

When driving a single-sided load, either OPHI or OPLO can be used. These outputs are very symmetric, so the only effect of this choice is to select the desired polarity. However, when the frequency range of interest extends to the upper limits of the AD8330, a dummy resistor of the same value should be attached to the unused output. Figure 60 illustrates the ac gain and phase response for various loads and V_{DBS} = 0.75 V. Line 1 shows the unloaded (C_L = 12 pF) case for reference; the gain is 6 dB lower (20 dB) using only the single-sided output. Adding a 75 Ω load from OPHI to an ac ground results in Line 2. The gain becomes a factor of ×1.5 V or 3.54 dB lower, but artifacts of the output common-mode control loop appear in both the magnitude and phase response.

Adding a dummy 75 Ω to OPLO results in Line 3: the gain is a further 2.5 dB lower, at about 14 dB. The CM artifacts are no longer present but a small amount of peaking occurs. If objectionable, this can be eliminated by raising both of the capacitors on the output pins to 25 pF, as shown in Line 4 of Figure 60.

The gain reduction incurred both by using only one output and by the additional effect of loading can be overcome by taking advantage of the VMAG feature, provided primarily for just such circumstances. Thus, to restore the basic gain in the first case (Line 1), a 1 V source should be applied to this pin; to restore the gain in the second case, this voltage should be raised by a factor of ×1.5 to 1.5 V. In Case 3 and Case 4, a further factor of ×1.33 is needed to make up the 2.5 dB loss, that is, V_{MAG} should be raised to 2 V. With the restoration of gain, the peak output swing at the load is, likewise restored to ±2 V.

Pulse Operation

When using the AD8330 in applications where its transient response is of greater interest and the outputs are conveyed to their loads via coaxial cables, the added capacitances can slightly differ in value, and can be placed either at the sending or load end of the cables, or divided between these nodes. Figure 61 shows an illustrative example where dual, 1 meter, 75 Ω cables are driven through dc-blocking capacitors and are independently terminated at ground level.

Because of the considerable variation between applications, only general recommendations can be made with regard to minimizing pulse overshoot and droop. The former can be optimized by adding small load capacitances, if necessary; the latter requires the use of sufficiently large capacitors (C1).

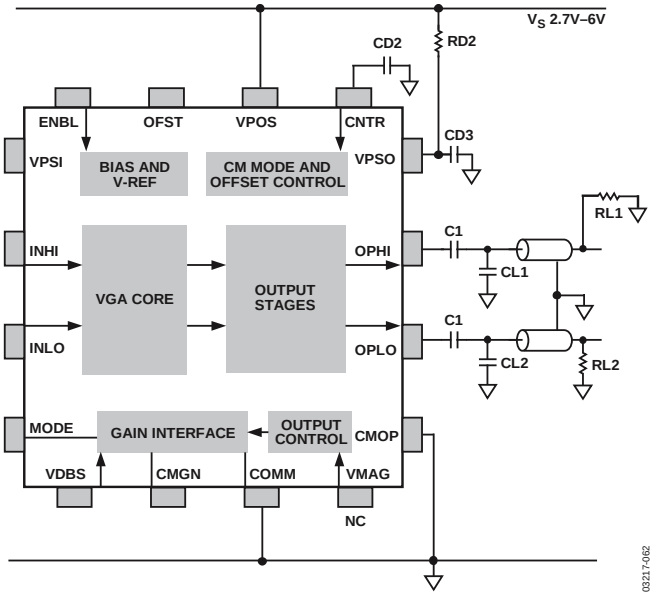

Figure 61. Driving Dual Cables with Grounded Loads

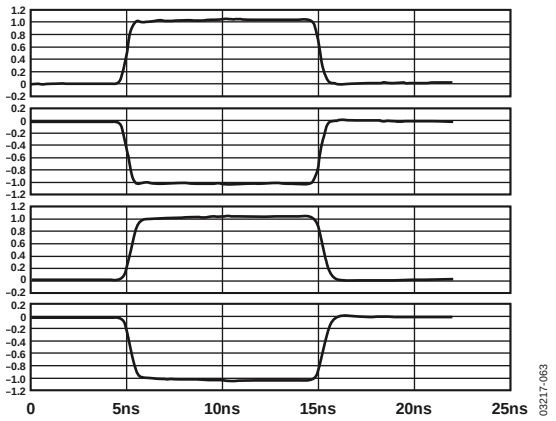

Figure 62. Typical Pulse Response for Figure 61

Figure 62 shows typical results for V_{DBS} = 0.24 V, a square wave input amplitude of 450 mV (the actual combination is not important), a rise time of 2 ns, and V_{MAG} raised to 2.0 V. In the upper waveforms, the load capacitors are both zero, and a small amount of overshoot is visible; with 40 pF, the response is cleaner. A shunt capacitance of 20 pF from OPHI to OPLO has a similar effect. Coupling capacitors for this demonstration are sufficiently large to prevent any visible droop over this time scale. The outputs at the load side eventually assume a mean value of zero, with negative and positive excursions depending on the duty cycle.

The bandwidth from Pin VMAG to these outputs is somewhat higher than from the normal input pins. Thus, when this pin is used to rapidly modulate the primary signal, some further experimentation with response optimization may be required. In general, the AD8330 is very tolerant of a wide range of loading conditions.

Preserving Absolute Gain

Although the AD8330 is not laser trimmed, its absolute gain calibration, based mainly on ratios, is very good. Full details are found in the Specifications section and in the typical performance curves (see the Typical Performance Characteristics section). Nevertheless, having finite input and output impedances, the gain is necessarily dependent on the source and load conditions. The loss that is incurred when either of these is finite causes an error in the absolute gain. The absolute gain can also be uncertain due to the approximately ±20% tolerance in the absolute value of the input and output impedances.

Often, such losses and uncertainties can be tolerated and accommodated by a correction to the gain control bias. On the other hand, the error in the loss can be essentially nulled by using appropriate modifications to either the source impedance (R_S) or the load impedance (R_L), or both (in some cases by padding them with series or shunt components).

The formulation for this correction technique was previously described. However, to simplify its use, Table 5 shows spot values for combinations of R_S and R_L resulting in an overall loss that is not dependent on sample-to-sample variations in on chip resistances. Furthermore, this fixed and predictable loss can be corrected by an adjustment to V_{MAG}, as indicated in Table 5.

Table 5. Preserving Absolute Gain

		Uncorrected Loss		V_{MAG} Required to
R_S (Ω)	R_L (Ω)	Factor	dB	Correct Loss
10	15 k	0.980	0.17	0.510
15	10 k	0.971	0.26	0.515
20	7.5 k	0.961	0.34	0.520
30	5.0 k	0.943	0.51	0.530
50	3.0 k	0.907	0.85	0.551
75	2.0 k	0.865	1.26	0.578
100	1.5 k	0.826	1.66	0.605
150	1.0 k	0.756	2.43	0.661
200	750	0.694	3.17	0.720
300	500	0.592	4.56	0.845
500	300	0.444	7.04	1.125
750	200	0.327	9.72	1.531
1 k	150	0.250	12.0	2.000
1.5 k	100	0.160	15.9	3.125
2 k	75	0.111	19.1	4.500

Calculation of Noise Figure

The AD8330 noise is a consequence of its intrinsic voltage noise spectral density (E_{NSD}) and the current noise spectral density (I_{NSD}). Their combined effect generates a net input noise, V_{NOISE_IN}, that is a function of the input resistance of the device (R_I), nominally 1 kΩ, and the differential source resistance (R_S) as follows:

$$V_{NOISE\_IN} = \sqrt{\left\{E_{NSD}{}^2 + I_{NSD}{}^2\left(R_I + R_S\right)^2\right\}} \tag{16}$$

Note that purely resistive source and input impedances as a concession to simplicity is assumed. A more thorough treatment of noise mechanisms, for the case where the source is reactive, is beyond the scope of these brief notes. Also note that V_{NOISE_IN} is the voltage noise spectral density appearing across INHI and INLO, the differential input pins. In preparing for the calculation of the noise figure, V_{SIG} is defined as the open-circuit signal voltage across the source, and V_{IN} is defined as the differential input to the AD8330. The relationship is simply

$$V_{IN} = \frac{V_{SIG}R_I}{\left(R_I + R_S\right)} \tag{17}$$

At maximum gain, E_{NSD} is 4.1 nV/√Hz, and I_{NSD} is 3 pA/√Hz. Thus, the short-circuit voltage noise is

$$V_{NOISE\_IN} = \sqrt{\left\{\left(4.1\ \text{nV}/\sqrt{\text{Hz}}\right)^2 + \left(3\,\text{pA}/\sqrt{\text{Hz}}\right)^2\left(1\ \text{k}\Omega + 0\right)^2\right\}} =$$

$$5.08\ \text{nV}/\sqrt{\text{Hz}} \tag{18}$$

Next, examine the net noise when $R_S = R_I$ = 1 kΩ, often incorrectly called the matching condition, rather than source impedance termination, which is the actual situation in this case.

Repeating the procedure,

$$V_{NOISE\_IN} = \sqrt{\left(4.1\text{ nV}/\sqrt{\text{Hz}}\right)^2 + \left(3\text{ pA}/\sqrt{\text{Hz}}\right)^2 \left(1\text{ k}\Omega + 1\text{ k}\Omega\right)^2}$$
$$= 7.3\text{ nV}/\sqrt{\text{Hz}} \quad (19)$$

The noise figure is the decibel representation of the noise factor, N_{FAC}, commonly defined as follows:

$$N_{FAC} = \frac{SNR\ at\ input}{SNR at\ output} \quad (20)$$

However, this is equivalent to

$$N_{FAC} = \frac{SNR\ at\ the\ source}{SNR\ at\ the\ input\ pins} \quad (21)$$

Let V_{NSD} be the voltage noise spectral density √kTRS due to the source resistance. Using Equation 17 gives

$$N_{FAC} = \frac{V_{SIG}\left\{R_I/\left(R_I + R_S\right)\right\}/V_{NSD}}{V_{IN}/\left\{V_{NOISE\_IN}R_S/\left(R_I + R_S\right)\right\}}$$
$$= \frac{R_I V_{NOISE\_IN}}{R_S\ V_{NSD}} \quad (22)$$

Then, using the result from Equation 19 for a source resistance of 1 kΩ, having a noise-spectral density of 4.08 nV/√Hz produces

$$N_{FAC} = \frac{\left(1\text{ k}\Omega\right)\left(7.3\text{ nV}/\sqrt{\text{Hz}}\right)}{\left(1\text{ k}\Omega\right)\left(4.08\text{ nV}/\sqrt{\text{Hz}}\right)} = 1.79 \quad (23)$$

Finally, converting this to decibels using

$$N_{FIG} = 10\log_{10}(N_{FAC}) \quad (24)$$

Thus, the resultant noise figure in this example is 5.06 dB, which is somewhat lower than the value shown in Figure 53 for this operating condition.

Noise as a Function of V_{DBS}

The chief consequence of lowering the basic gain using V_{DBS} is that the current noise spectral density I_{NSD} increases with the square root of the basic gain magnitude, G_{BN} such that

$$I_{NSD} = (3\text{ pA}/\sqrt{\text{Hz}})(\sqrt{G_{BN}}) \quad (25)$$

Therefore, at the minimum basic gain of ×0, I_{NSD} rises to 53.3 pA/√Hz. However, the noise figure rises to 17.2 db if it is recalculated using the procedures in Equation 16 through Equation 24.

Distortion Considerations

Continuously variable gain amplifiers invariably employ nonlinear circuit elements; consequently, it is common for their distortion to be higher than well-designed fixed gain amplifiers. The translinear multiplier principles used in the AD8330, in theory, yield extremely low distortion, a result of the fundamental linearization technique that is an inherent aspect of these circuits.

In practice, however, the effect of device mismatches and junction resistances in the core cell, and other mechanisms in its supporting circuitry inevitably cause distortion, further aggravated by other effects in the later output stages. Some of these effects are very consistent from one sample to the next, while those due to mismatches (causing predominantly even-order distortion components) are quite variable. Where the highest linearity (and lowest noise) is demanded, consider using one of the X-AMP products such as the AD603 (single-channel), AD604 (dual-channel), or AD8332 (wideband dual-channel with ultralow noise LNAs).

P1dB and V1dB

In addition to the nonlinearities that arise within the core of the AD8330, at moderate output levels, another metric that is more commonly stated for RF components that deliver appreciable power to a load is the 1 dB compression point. This is defined in a very specific manner: it is that point at which, with increasing output level, the power delivered to the load eventually falls to a value that is 1 dB lower than it would be for a perfectly linear system. (Although this metric is sometimes called the 1 dB gain compression point, it is important to note that this is not the output level at which the incremental gain has fallen by 1 dB).

As shown in Figure 49, the output of the AD8330 limits quite abruptly, and the gain drops sharply above the clipping level. The output power, on the other hand, using an external resistive load, R_L, continues to increase. In the most extreme case, the waveform changes from the sinusoidal form of the test signal, with an amplitude just below the clipping level, V_{CLIP}, to a square wave of precisely the same amplitude. The change in power over this range is from $(V_{CLIP}/\sqrt{2})^2/R_L$ to $(V_{CLIP})^2/R_L$, that is, a factor of 2, or 3 dB in power terms. It can be shown that for an ideal limiting amplifier, the 1 dB compression point occurs for an overdrive factor of 2 dB.

For example, if the AD8330 is driving a 150 Ω load and V_{MAG} is set to 2 V, the peak output is nominally ±4 V (as noted previously, the actual value, when loaded. can differ because of a mismatch between on-chip and external resistors), or 2.83 V rms for a sine wave output that corresponds to a power of 53.3 mW, that is, 17.3 dBm in 150 Ω. Thus, the P1dB level, at 2 dB above clipping, is 19.3 dBm.

Though not involving power transfer, it is sometimes useful to state the V1dB, which is the output voltage (unloaded or loaded) that is 2 dB above clipping for a sine waveform. In the above example, this voltage is still 2.83 V rms, which can be expressed as 9.04 dBV (0 dBV corresponds to a 1 V sine wave). Thus, the V1dB is at 11.04 dBV.

APPLICATIONS INFORMATION

The versatility of the AD8330, its very constant ac response over a wide range of gains, the large signal dynamic range, output swing, single supply operation, and low power consumption commend this VGA to a diverse variety of applications. Only a few can be described here, including the most basic uses and some unusual ones.

ADC DRIVING

The AD8330 is well-suited to drive a high speed converter. There are many high speed converters available, but to illustrate the general features, the example in this data sheet uses one of the least expensive, the AD9214. This is available in three grades for operation at 65 MHz, 80 MHz, and 105 MHz; the AD9214BRS-80 is a good complement to the general capabilities of this VGA.

Figure 63 shows the connections to drive an ADC. A 3.3 V supply is used for both parts. The ADC requires that its input pins be positioned at one third of the supply, or 1.1 V. Given that the default output level of the VGA is one-half the supply or 1.65 V, a small correction is introduced by the 8 kΩ resistor from CNTR to ground. The ADC specifications require that the common-mode input be within ±0.2 V of the nominal 1.1 V; variations of up to ±20% in the AD8330 on-chip resistors change this voltage by only ±70 mV. With the connections shown in Figure 63, the AD9214 is able to receive an input of 2 V p-p; the peak output of the AD8330 can be reduced if desired by adding a resistor from VMAG to ground. An overrange condition is signaled by a high state on Pin OR of the AD9214. DFS/GAIN is unconnected in this example producing an offset-binary output. To provide a twos complement output, it should be connected to the REF pin.

For ADCs running at sampling rates substantially below the bandwidth of the AD8330, an intervening noise filter is recommended to limit the noise bandwidth. A one-pole filter can easily be created with a single differential capacitor between the OPHI and OPLO outputs. For a corner frequency of f_C, the capacitor should have a value of

$$C_{FILT} = 1/942\, f_C \quad (26)$$

For example, a 10 MHz corner requires about 100 pF.

SIMPLE AGC AMPLIFIER

Figure 64 illustrates the use of the inverted gain mode and the offset gain range (0.2 V < V_{DBS} < 1.7 V) in supporting a low cost AGC loop. Q1 is used as a detector. When OPHI is sufficiently higher than CNTR, due to the signal swing, it conducts and charges C1. This raises V_{DBS} and rapidly lowers the gain. Note that MODE is grounded (see Figure 48). The minimum voltage needed across R1 to set up the full gain is 0.2 V because CMGN is dc open-circuited (this does not alter V_{MAG}) and the maximum voltage is 1.7 V.

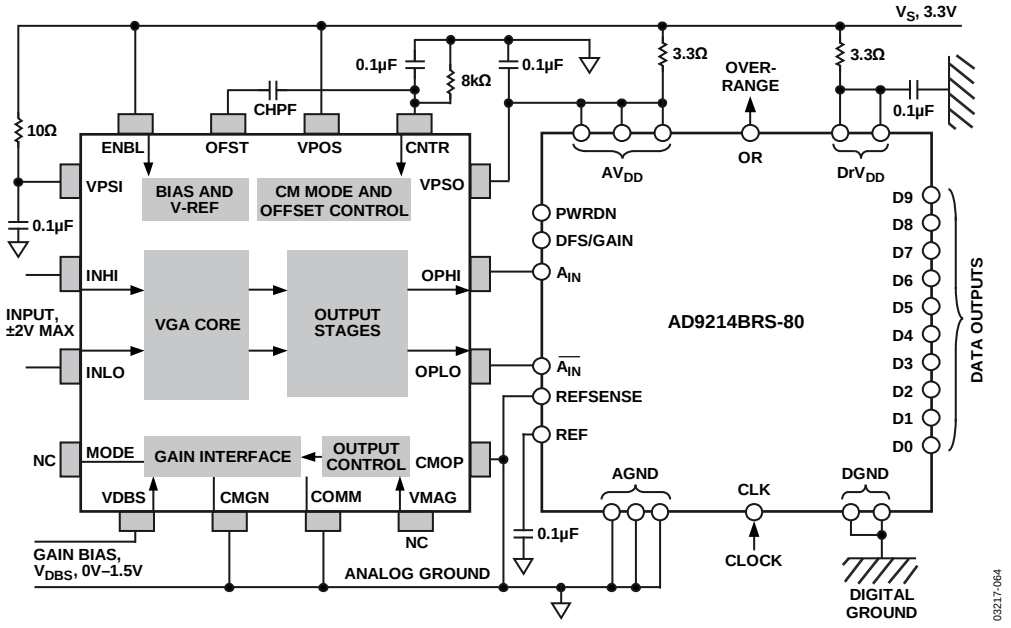

Figure 63. Driving an Analog-to-Digital Converter (Preliminary)

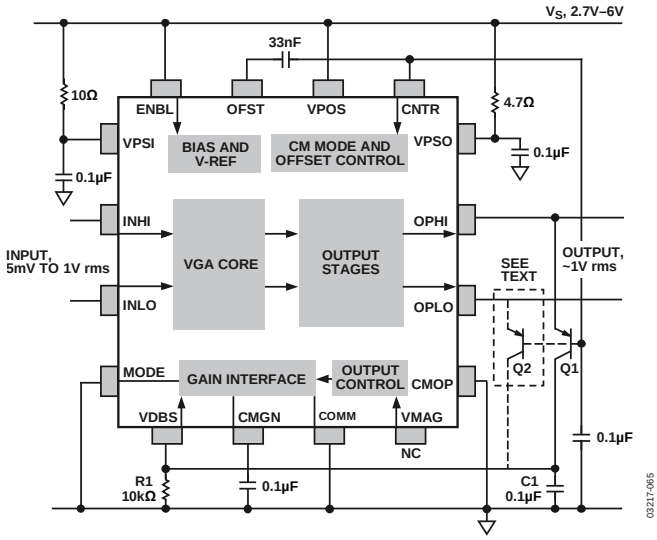

Figure 64. Simple AGC Amplifier (Preliminary)

When the loop is settled, the average current in Q1 is V_{DBS}/R1, which varies from 2 µA at maximum gain (V_{DBS} = 0.2 V) to 17 µA at minimum gain (V_{DBS} = 1.7 V). This change in the Q1 current causes an increase of ~0.25 dB over the full gain range in the differential output of nominally 0.75 dBV at midrange (3.08 V p-p), corresponding to a 200:1 compression ratio. This is plotted in Figure 65 for a representative 100 kHz input.

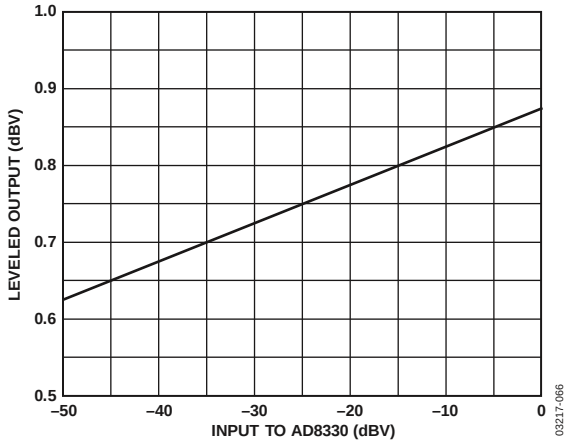

Figure 65. AGC Output vs. Input Amplitude (Simulation)

The upper panel in Figure 66 shows the time-domain output for fourteen 3 dB steps in input amplitude from 5.4 mV to 1.7 V. The waveforms in Figure 65 show the AGC voltage (V_{DBS}).

This simple detector exhibits a temperature variation in the differential output amplitude of about 4 mV/°C. It provides a fast attack time (an increase in the input is quickly leveled to the nominal output, due to the high peak currents in Q1) and a slow release time (a decrease in the input is not restored as quickly). The voltage at the VDBS pin can be used as an RSSI output, scaled 30 mV/dB. Note that the attack time can be halved by adding a second transistor, labeled Q2 in Figure 64. For operation at lower frequencies, the AGC hold capacitor must be increased.

WIDE RANGE TRUE RMS VOLTMETER

The AD8362 is an rms responding detector providing a dynamic range of 60 dB from low frequencies to 2.7 GHz. This can increase to 110 dB using an AD8330 as a preconditioner, provided the noise bandwidth is limited by an interstage low-pass or band-pass filter.

The VGA also provides an input port that is easier to drive than the 200 Ω input of the AD8362. Figure 67 shows the general scheme.

Both the AD8330 and AD8362 provide linear-in-decibel control interfaces. Thus, when the output of the AD8362 is used to control the gain of the AD8330, the functional form is unaffected. The overall scaling is 33 mV/dB. Figure 68 shows the time domain response using a loop filter capacitor of 10 nF, for inputs ranging from 10 µV to 1 V rms, that is, a 100 dB measurement range.

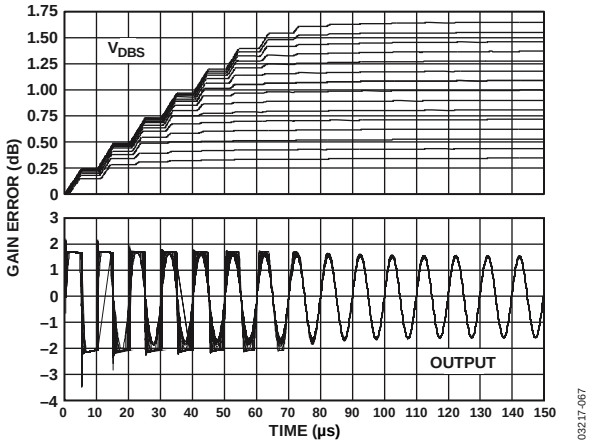

Figure 66. Time Domain Waveforms (Simulation)

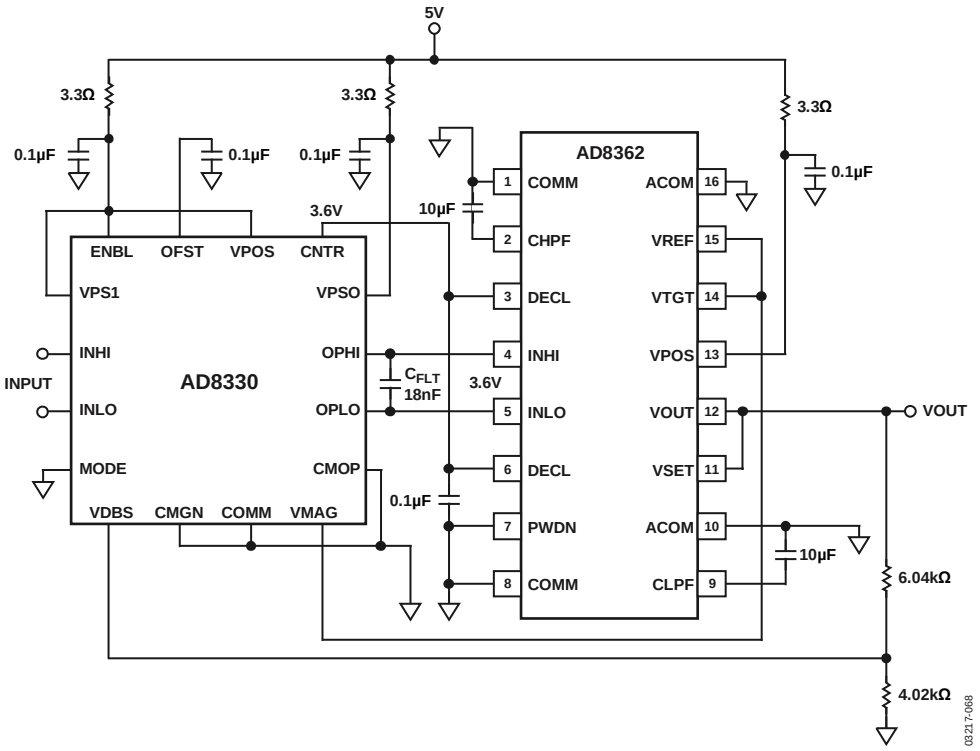

Figure 67. Wide Range True RMS Voltmeter (Preliminary)

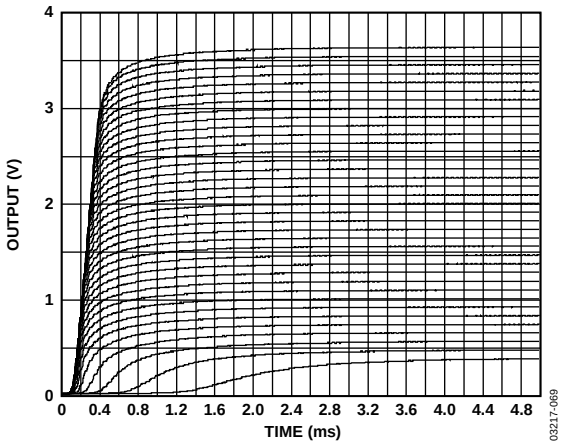

Figure 68. Time Domain Response of RMS Voltmeter (Simulation)

EVALUATION BOARD

GENERAL DESCRIPTION

The AD8330-EVALZ is an easy-to-use accessory that enables a hands-on evaluation of the AD8330 variable gain amplifier (VGA). It includes test pins for connections to all of the functional device inputs. Figure 69 is a full size photograph of the board.

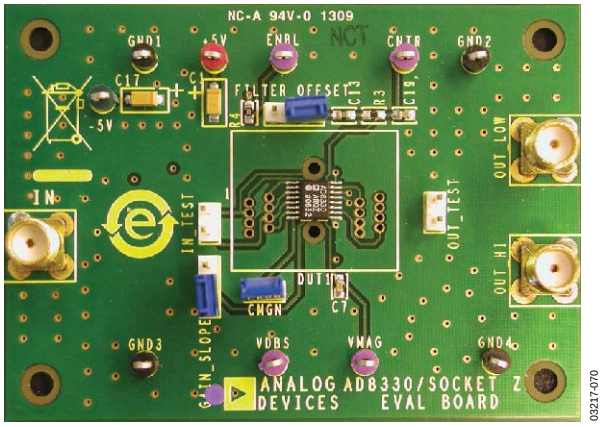

Figure 69. Photograph of the AD8330 Evaluation Board

BASIC OPERATION

The input SMA connector IN is terminated with a 49.9 Ω resistor (see Figure 70). For convenience, the board includes an AD8131 high speed differential amplifier to convert a single-ended signal source to the differential input of the AD8330. If desired, the AD8131 can be removed and the AD8330 can be driven at one of its inputs from a single-ended source.

The AD8330 output is observed at the SMA connectors OUT_HI and OUT_LO or by using the 2-pin header OUT_HI/ OUT_LO adjacent to the device.

The AD8330 requires only a +5 V power supply; however, because of the AD8131 buffer bipolar power supply requirements, ±5 V supplies are required to power the board. The current required for the board is approximately 40 mA from the +5 V supply and 10 mA from the −5 V supply.

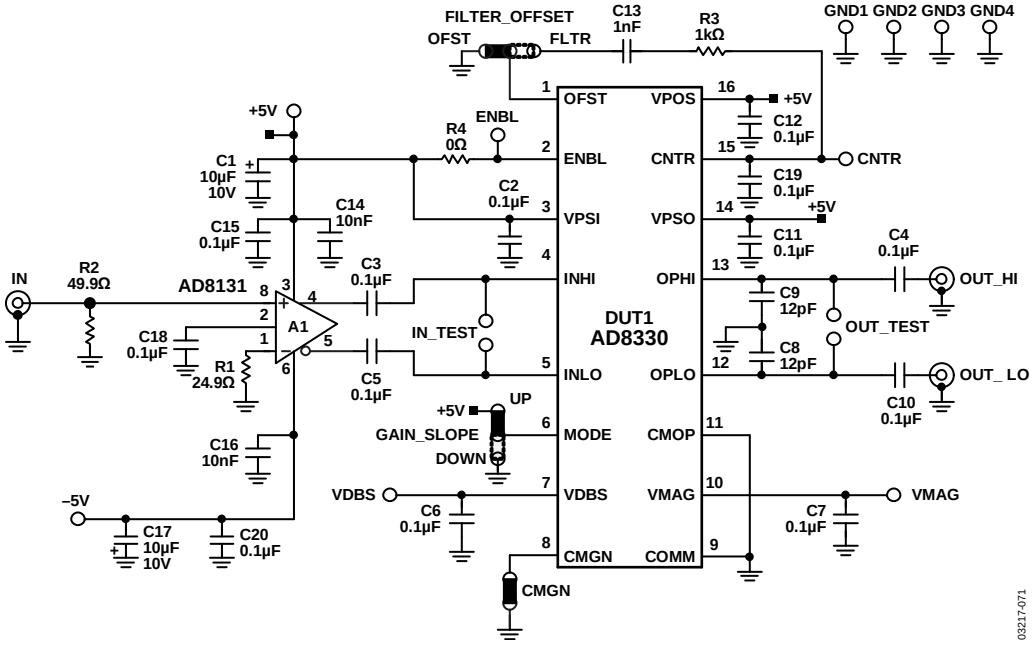

Figure 70. Schematic Diagram

OPTIONS

Table 6 lists the jumpers on the board and their functions.

Table 6. Functions of Jumpers

Name	Function
FLTR	Connects a high-pass filter to the offset control loop pin. This jumper is normally not installed.
OFST	Disables the offset correction loop. This jumper is installed for dc or low frequency operation.
UP	Mode up. Install for ascending gain with increasing VDBS gain control voltage.
DOWN	Mode down. Install for descending gain with increasing VDBS gain control voltage.

MEASUREMENT SETUP

The basic board connections for a typical measurement are shown in Figure 71. To minimize circuit-loading effects, a low capacitance FET probe is recommended for observing input or output waveforms. Two-pin headers, IN_TEST and OUT_TEST, are provided for this purpose. The SMA connectors OUT_HI and OUT_LO can also be used, but the user may need to account for load capacitance effects.

AD8330-EVALZ BOARD DESIGN

The AD8330-EVALZ is a 4-layer design for maximum ground-plane area. The evaluation board side silkscreen and wiring patterns are shown in Figure 72 through Figure 77.

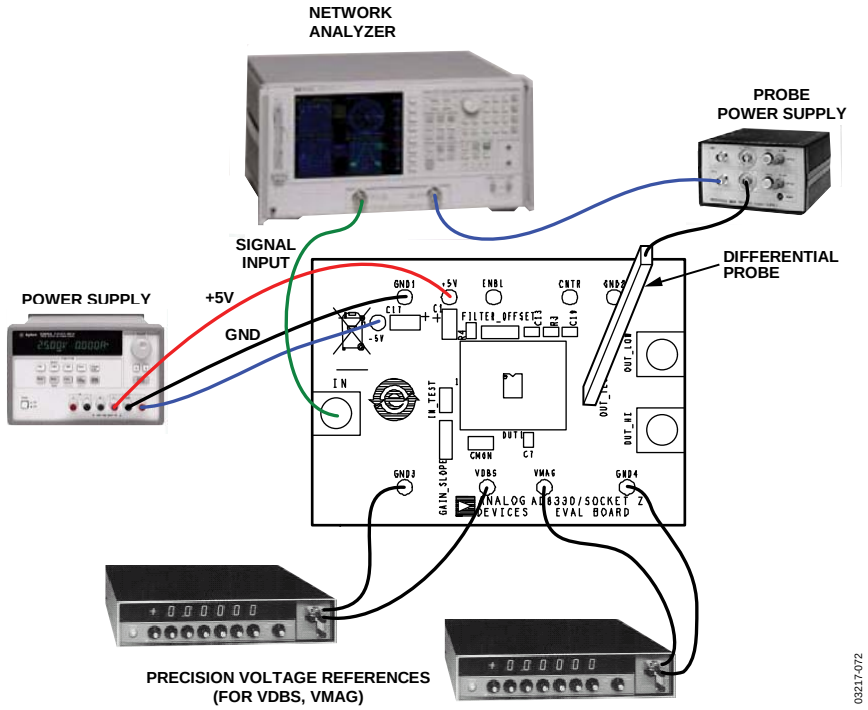

Figure 71. Typical Connections

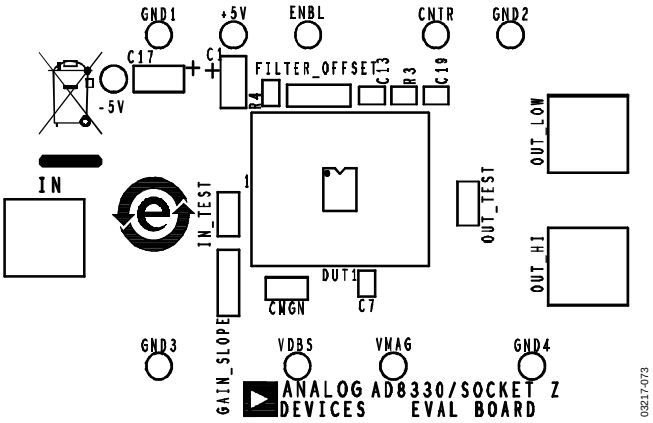

Figure 72. Component-Side Silkscreen

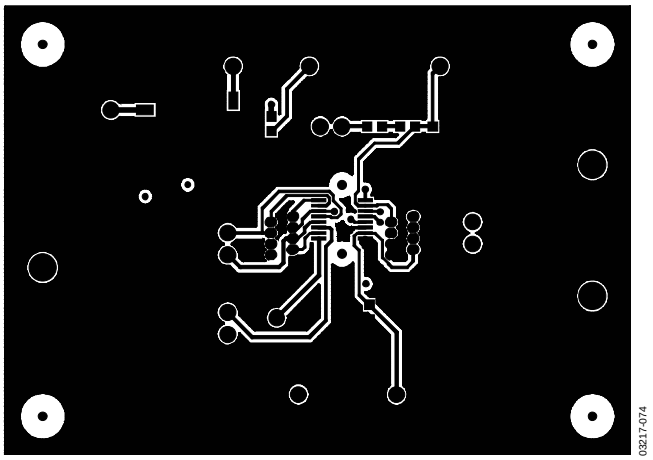

Figure 73. Component-Side Wiring

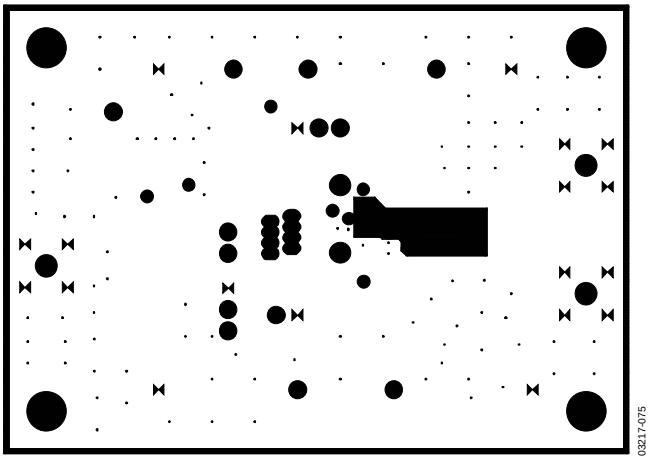

Figure 74. Ground Plane

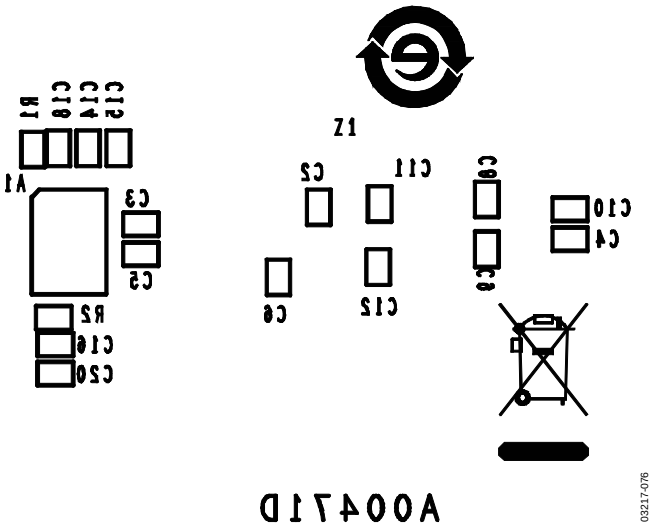

Figure 75. Wiring-Side Silkscreen

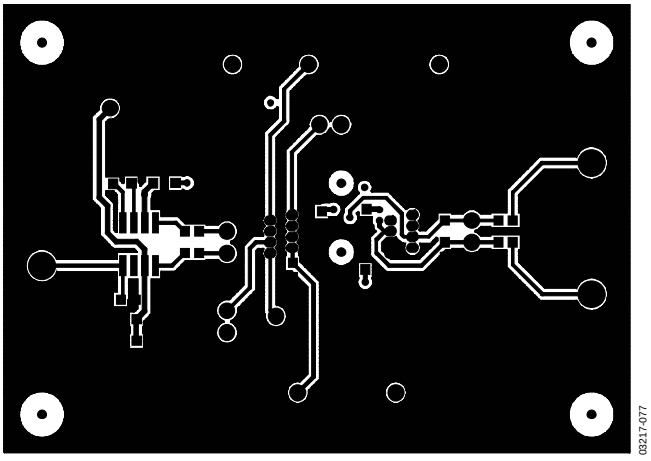

Figure 76. Wiring-Side Pattern

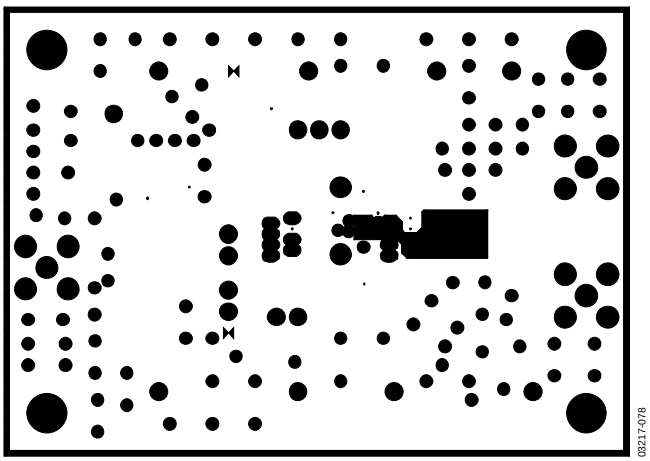

Figure 77. Inner Layer 2

OUTLINE DIMENSIONS

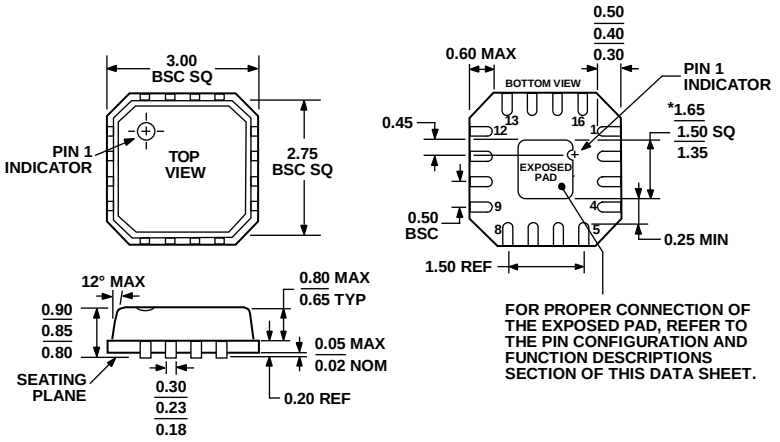

Figure 78. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad
(CP-16-3)
Dimensions shown in millimeters

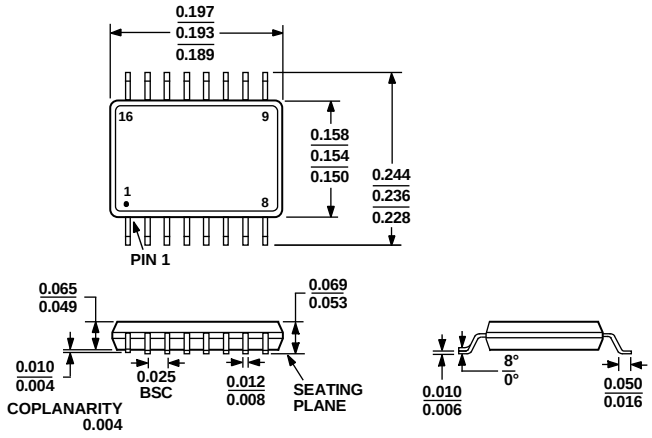

Figure 79. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8330ACPZ-R2	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFZ
AD8330ACPZ-RL	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFZ
AD8330ACPZ-R7	−40°C to +85°C	16-Lead LFCSP_VQ	CP-16-3	JFZ
AD8330ARQ	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQ-REEL	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQ-REEL7	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQZ	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQZ-RL	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330ARQZ-R7	−40°C to +85°C	16-Lead QSOP	RQ-16	
AD8330-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.

D03217-0-3/10(E)