AAT1171

600mA Voltage-Scaling Step-Down Converter for RF Power Amplifiers with Bypass Switch

SwitchReg™

General Description

The AAT1171 SwitchReg dynamically controls the operating voltage of a WCDMA or CDMA power amplifier inside single-cell, lithium-ion battery-powered systems. The AAT1171 outputs a voltage between 0.6V and 3.6V, thereby optimizing the amplifier efficiency at both low and high transmit levels.

The AAT1171 output voltage is controlled via an analog signal from the baseband processor. It can deliver 600mA of continuous load current while maintaining a low 45µA of no load quiescent current. The 2MHz switching frequency minimizes the size of external components while keeping switching losses low. To further improve system efficiency, an 85mΩ bypass MOSFET transistor is also included to allow the PA to be powered directly from the battery.

The AAT1171 maintains high efficiency thoughout the entire load range in Light Load (LL) mode, and can be forced into Pulse Wide Modulation (PWM) mode for low noise operation or can be synchronized to an external clock.

The AAT1171 is available in a Pb-free, space-saving TDFN33-12 package and is rated over the -40°C to +85°C temperature range.

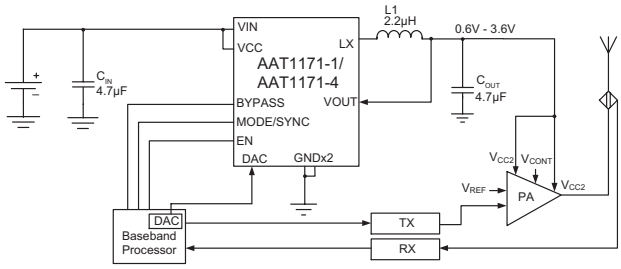
Features

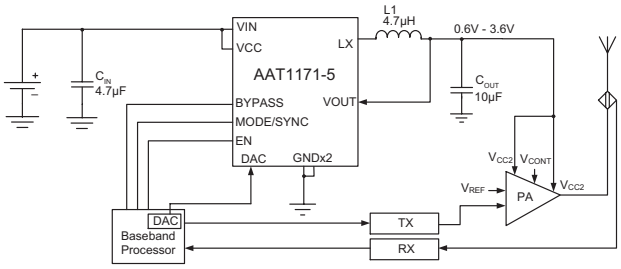
- V_{IN} Range: 2.7V to 5.5V
- Variable Output Voltage: 0.6V to 3.6V
- 600mA Output Current
- DAC Input: 0.2V to 1.2V
- High Output Accuracy: ±3%
- 45µA No Load Quiescent Current
- Internal Soft Start Limits Startup Current and Output Voltage Overshoot
- Synchronizable to External 19.8MHz System Clock
- Over-Temperature and Current Limit Protection
- Integrated 85mΩ Bypass MOSFET
- 2MHz Operation
- PWM/LL Control with Override
- Fast Start-Up:
  - 50µs (AAT1171-4, AAT1171-5)
  - 150µs (AAT1171-1)
- 100% Duty Cycle Operation
- <30µs Output Voltage Response Time
- 3x3mm 12-Pin TDFN Package
- Temperature Range: -40°C to +85°C

Applications

- WCDMA or CDMA PA in Cellular Phones, Smartphones, Feature Phones, etc.
- Express Card
- PCMCIA Data Cards

Typical Application



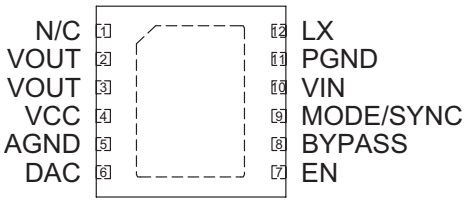


Pin Descriptions

Pin #	Symbol	Function
1	N/C	Not connected.
2, 3	VOUT	Feedback input pin. This pin is connected to the converter output. It is used to complete the control loop, regulating the output voltage to the desired value. When in bypass mode, a low resistance MOSFET is connected between this pin and VIN.
4	VCC	Bias supply. Supply power for the internal circuitry. Connect to input power via low pass filter with decoupling to AGND.
5	AGND	Analog ground. Connect the return of all small signal components to this pin.
6	DAC	Control voltage input from a DAC. Input voltage between 0.2V and 1.2V to control output voltage of the converter. Force pin to 1.3V for bypass switch enable.
7	EN	Enable DC/DC converter, active high.
8	BYPASS	Enable control to bypass the DC/DC converter when PA transmitting at full power from low battery voltage. Active high.
9	MODE/SYNC	This pin is used to program the device between PWM and LL mode: HIGH - PWM Mode Only LOW - LL Mode: PWM operation for loads above 100mA and variable switching frequency for loads below 100mA Connecting the SYNC pin to the system clock (19.8MHz) will override the internal clock and force the switching frequency to the external clock frequency divided by 10.
10	VIN	Input supply voltage for the converter. Must be closely decoupled.
11	PGND	Main power ground. Connect to the output and input capacitor return.
12	LX	Switching node. Connect the inductor to this pin. It is connected internally to the drain of both low- and high-side MOSFETs.
EP		Exposed paddle (bottom). Connect to ground directly beneath the package.

Pin Configuration

TDFN33-12
(Top View)



Absolute Maximum Ratings[1]

Symbol	Description	Value	Units
V_{CC}, V_{IN}	Input Voltage and Bias Power to GND	6.0	V
V_{LX}	LX to GND	-0.3 to V_{IN} + 0.3	V
V_{OUT}	VOUT to GND	-0.3 to V_{IN} + 0.3	V
V_N	EN, DAC, BYPASS, MODE/SYNC to GND	-0.3 to 6.0	V
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	°C

Thermal Information[2]

Symbol	Description	Value	Units
P_D	Maximum Power Dissipation, T_A = 25°C	2.0	W
θ_{JA}	Thermal Resistance, T_A = 25°C	50	°C/W

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Mounted on an FR4 board.

Electrical Characteristics[1]

T_A = -40°C to +85°C, unless otherwise noted. V_{IN} = V_{CC} = 3.6V; typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage		2.7		5.5	V
V_{UVLO}	UVLO Threshold	V_{IN} Rising		2.6		V
	UVLO Hysteresis			200		mV
V_{OUT}	V_{OUT} Programmable Range		0.6		3.6	V
V_{DACIN}	Input Voltage Range from DAC		0.2		1.2	V
I_Q	Quiescent Current	No Load, Light Load		45	70	µA
		No Load, PWM, V_{CC} Bias Current		420		
I_{SHDN}	Shutdown Current	EN = AGND = PGND			1.0	µA
I_{LIM}	P-Channel Current Limit	T_A = 25°C	1.2	1.6		A
$R_{DS(ON)H}$	High Side Switch On Resistance			230		mΩ
$R_{DS(ON)L}$	Low Side Switch On Resistance			230		mΩ
$R_{DS(ON)BP}$	Bypass Switch Resistance	V_{DAC} = 1.3V or BYPASS = VIN		85		mΩ
I_{LXLEAK}	LX Leakage Current	V_{CC} = 5.5V, V_{LX} = 0 to V_{CC}			1	µA
$\Delta V_{OUT}/V_{OUT}$	Load Regulation	I_{LOAD} = 0 to 500mA			0.5	%
$\Delta V_{OUT}/V_{OUT}/\Delta V_{IN}$	Line Regulation				0.2	%/V
R_{OUT}	Feedback Impedance			170		kΩ
V_{OUT}	Output Voltage Accuracy	V_{DAC} = 0.6V, I_{LOAD} = 0	1.746	1.8	1.854	V
F_{OSC}	Oscillator Frequency			2.0		MHz
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C
I_{LL}	Light Load Load Current Threshold			100		mA
t_{VOUTS}	Output Voltage Settling Time	V_{OUT} = 0.6V to $V_{OUT(MAX)}$, MODE/SYNC = V_{IN}			30	µs

1. The AAT1171 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.

Electrical Characteristics[1]

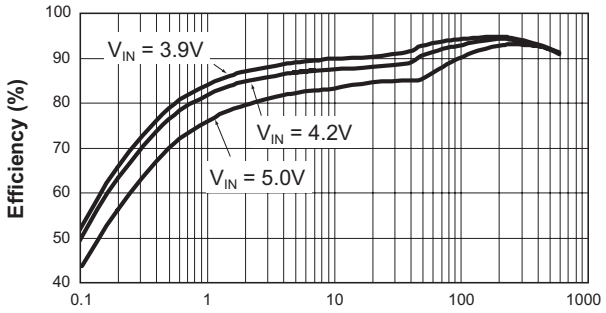
T_A = -40°C to +85°C, unless otherwise noted. V_{IN} = V_{CC} = 3.6V; typical values are T_A = 25°C.

Symbol	Description	Conditions	Min	Typ	Max	Units
PWM/Light Load/EN						
$V_{EN(L)}$	Enable Threshold Low				0.6	V
$V_{EN(H)}$	Enable Threshold High		1.4			V
I_{EN}	Input Low Current	V_{CC} = 5.5V	-1.0		1.0	µA
t_{EN}	Turn-On Enable Response Time	AAT1171-1: EN = Low to High, MODE/SYNC = High, V_{DAC} = 1.2V		150		µs
		AAT1171-4/AAT1171-5: EN = Low to High, MODE/SYNC = High, V_{DAC} = 1.2V		50		
SYNC						
F_{SYNC}	Synchronization Frequency	Sync to 19.8MHz[2]		19.8		MHz
$V_{SYNC(H)}$	SYNC High Level Threshold		1.6			V
$V_{SYNC(L)}$	SYNC Low Level Threshold				0.6	
I_{SYNC}	SYNC Low Current	V_{SYNC} = GND or V_{CC}	-1.0		1.0	µA
DAC Input						
Gain	Output Voltage/DAC Voltage[3]			3		V/V

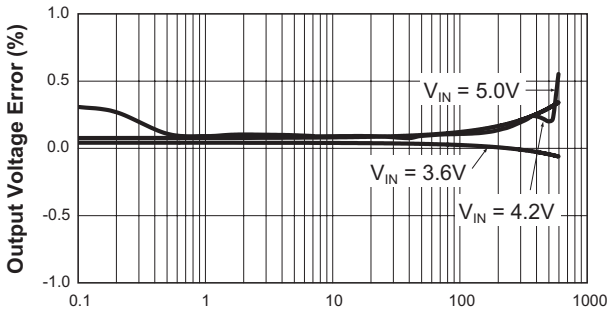
1. The AAT1171 is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range and is assured by design, characterization, and correlation with statistical process controls.
2. Please contact Sales for other synchronization frequencies.
3. Please contact Sales for other output voltage/DAC voltage gains.

Typical Characteristics

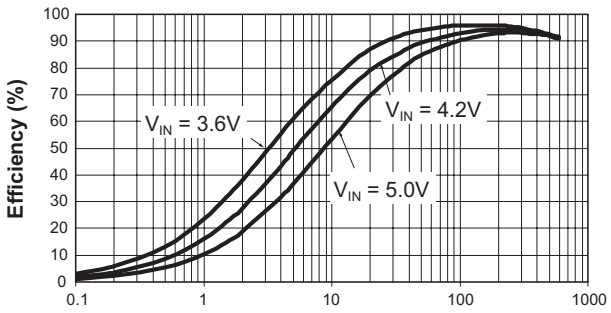
Efficiency vs. Output Current
(LL Mode; V_{OUT} = 3.3V)



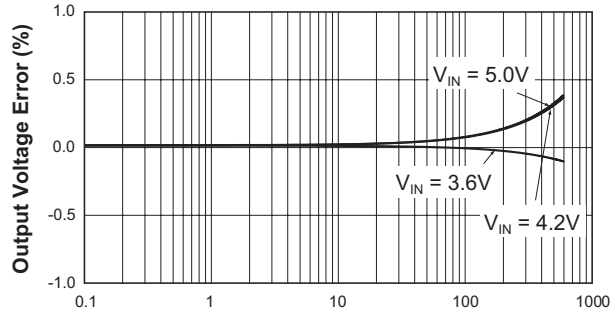
Load Regulation
(LL Mode; V_{OUT} = 3.3V)



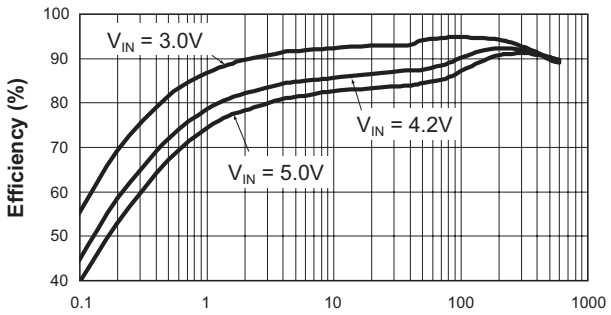
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 3.3V)



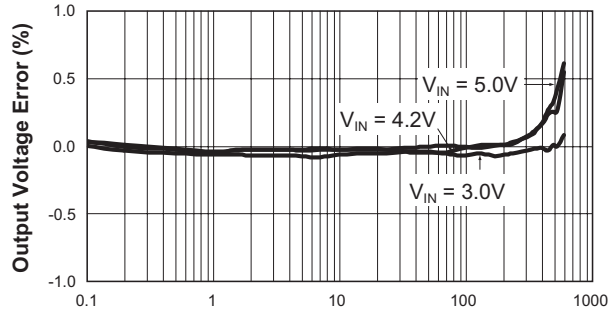
Load Regulation
(PWM Mode; V_{OUT} = 3.3V)



Efficiency vs. Output Current
(LL Mode; V_{OUT} = 2.5V)

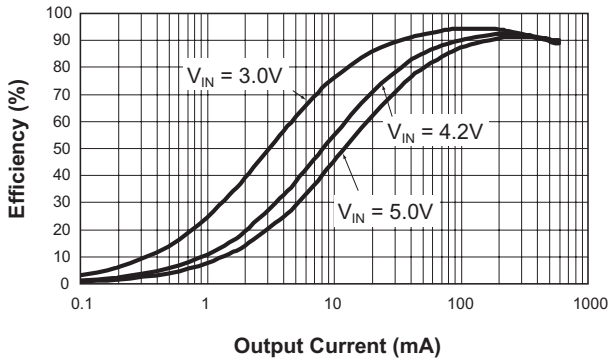


Load Regulation
(LL Mode; V_{OUT} = 2.5V)

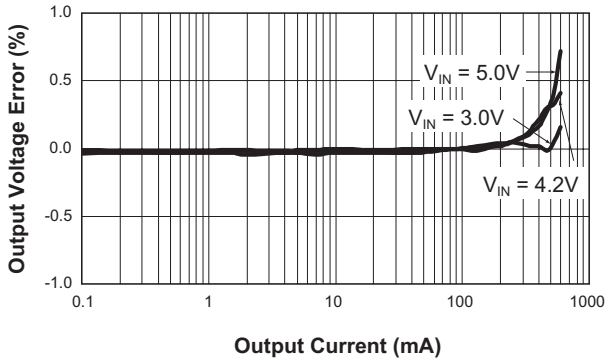


Typical Characteristics

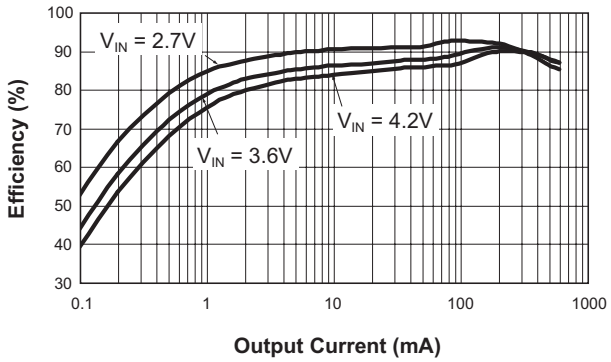
Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 2.5V)



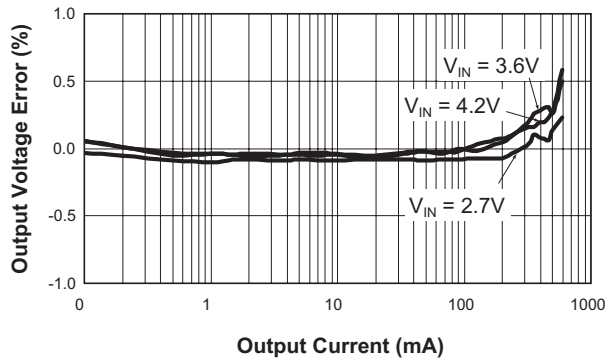
Load Regulation
(PWM Mode; V_{OUT} = 2.5V)



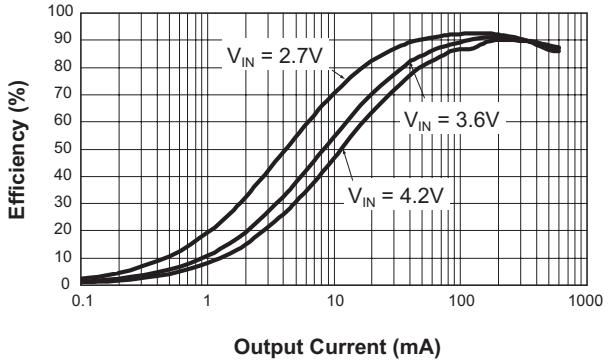
Efficiency vs. Output Current
(LL Mode; V_{OUT} = 1.8V)



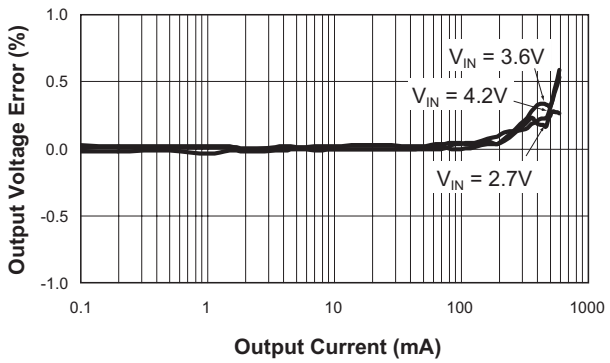
Load Regulation
(LL Mode; V_{OUT} = 1.8V)



Efficiency vs. Output Current
(PWM Mode; V_{OUT} = 1.8V)

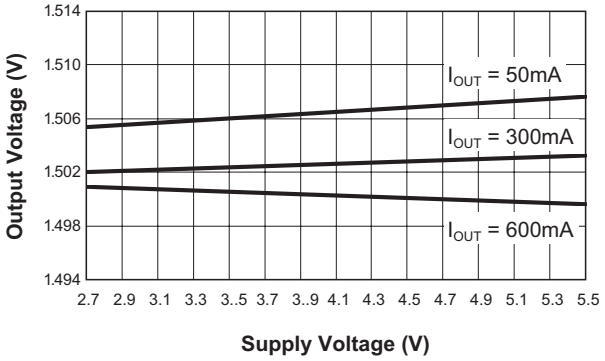


Load Regulation
(PWM Mode; V_{OUT} = 1.8V)

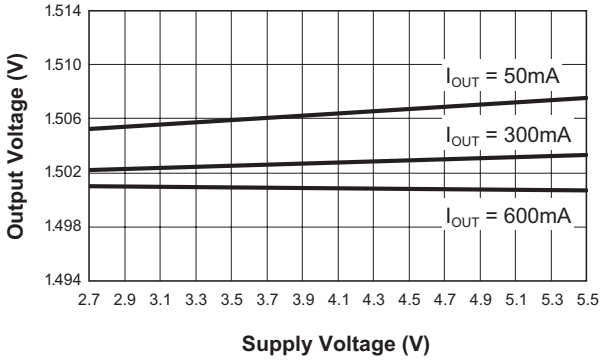


Typical Characteristics

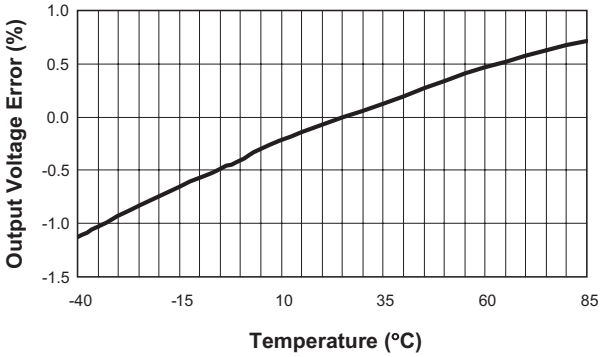
Output Voltage vs. Supply Voltage
(LL Mode; V_{OUT} = 1.5V)



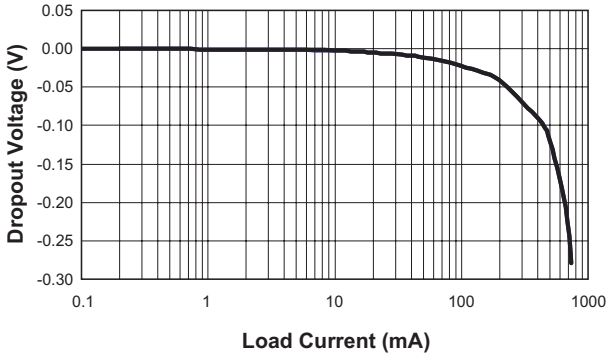
Output Voltage vs. Supply Voltage
(PWM Mode; V_{OUT} = 1.5V)



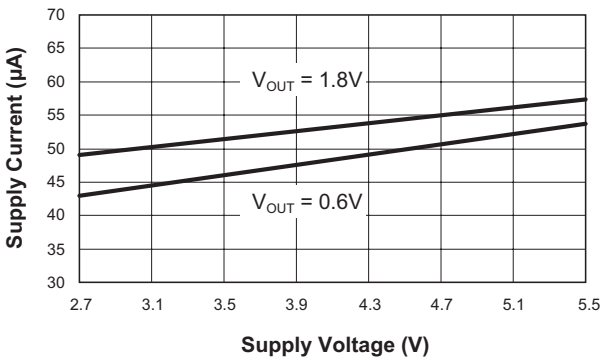
Output Voltage vs. Temperature
(V_{IN} = 3.6V; V_{OUT} = 1.8V; V_{DAC} = 0.6V; R_L = 10)



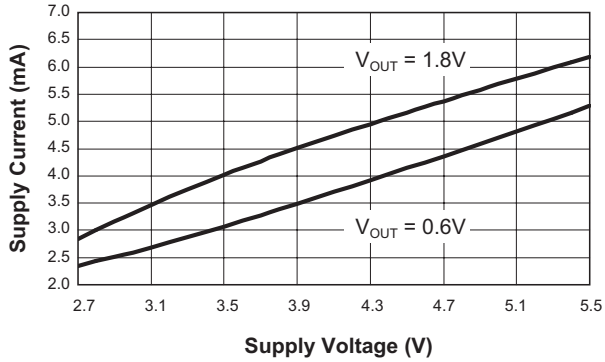
Bypass Mode Dropout Voltage vs. Load Current



Supply Current vs. Supply Voltage
(No Load; LL Mode)

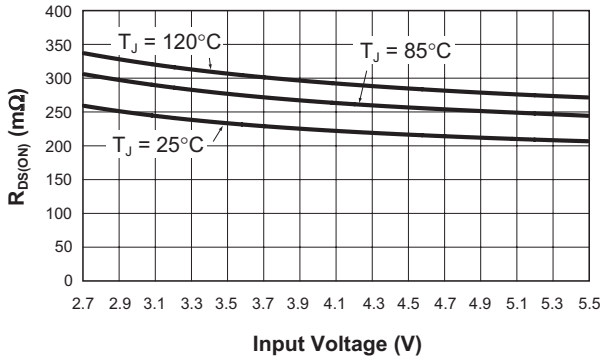


Supply Current vs. Supply Voltage
(No Load; PWM Mode)

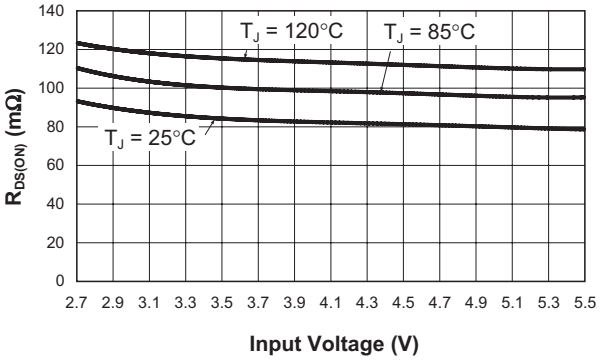


Typical Characteristics

P-Channel $R_{DS(ON)}$ vs. Input Voltage

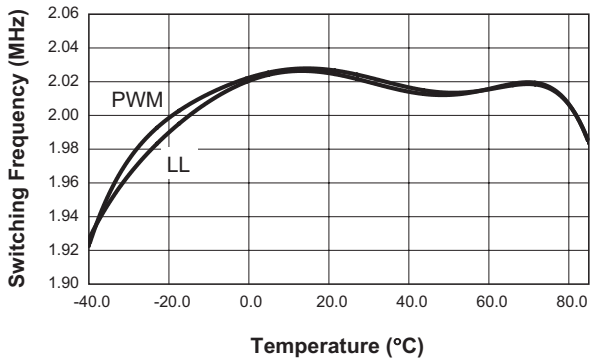


Bypass $R_{DS(ON)}$ vs. Input Voltage



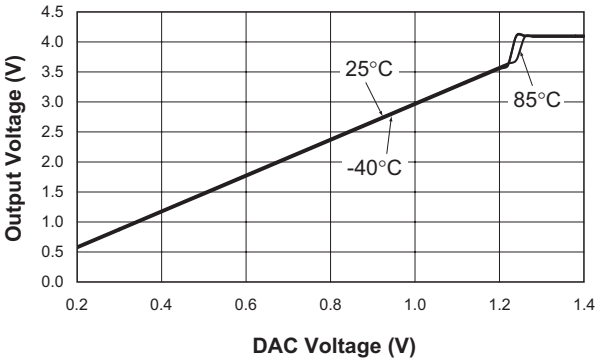
Switching Frequency vs. Temperature

(V_{IN} = 3.6V; V_{OUT} = 1.8V; R_L = 10)



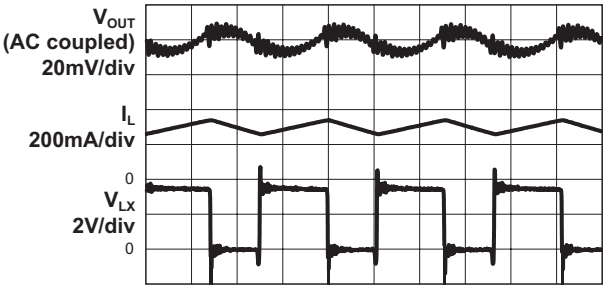
Output Voltage vs. DAC Voltage

(V_{IN} = 4.2V; LL Mode)



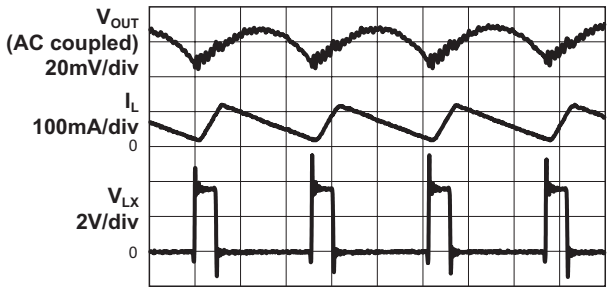
Heavy Load Switching Waveform

(V_{IN} = 3.6V; V_{OUT} = 1.8V; R_L = 3Ω; C_{OUT} = 4.7µF; L = 2.2µH)



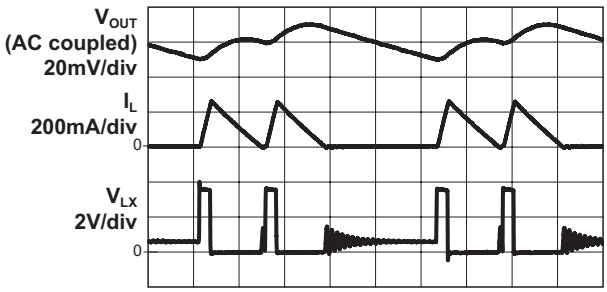
Typical Characteristics

Light Load Switching Waveform
(PWM Mode; V_{IN} = 4.2V; V_{OUT} = 0.6V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



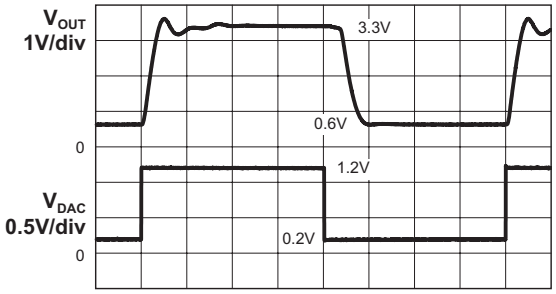
Time (200ns/div)

Light Load Switching Waveform
(LL Mode; V_{IN} = 4.2V; V_{OUT} = 0.6V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



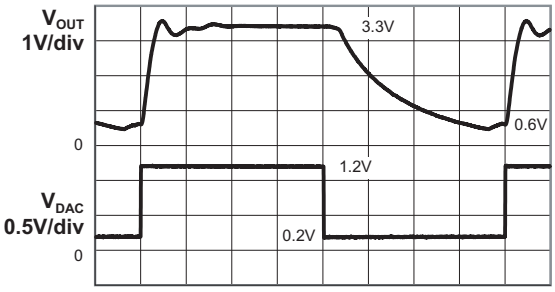
Time (1µs/div)

DAC Transient Response in PWM Mode
(V_{IN} = 3.6V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



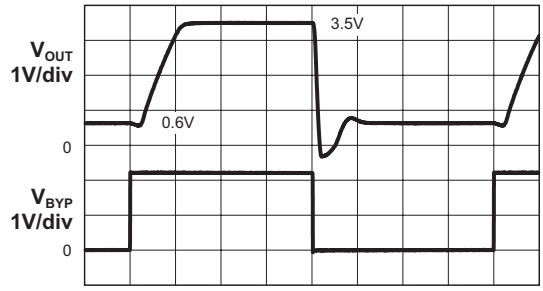
Time (25µs/div)

DAC Transient Response in LL Mode
(V_{IN} = 3.6V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



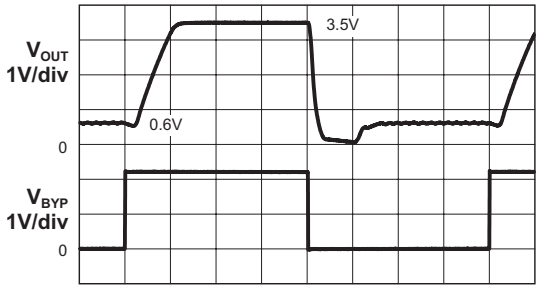
Time (25µs/div)

Bypass Transient Response
(PWM Mode; V_{IN} = 3.6V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



Time (25µs/div)

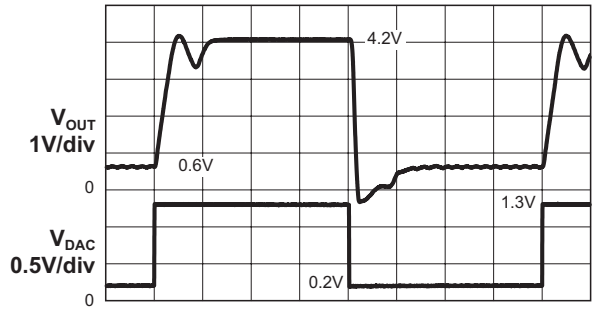
Bypass Transient Response
(LL Mode; V_{IN} = 3.6V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



Time (25µs/div)

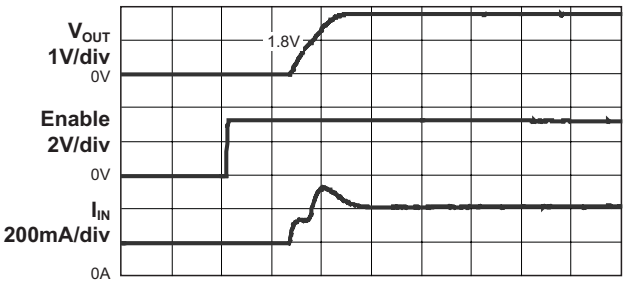
Typical Characteristics

DAC to Bypass Transient Response
(V_{IN} = 4.2V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



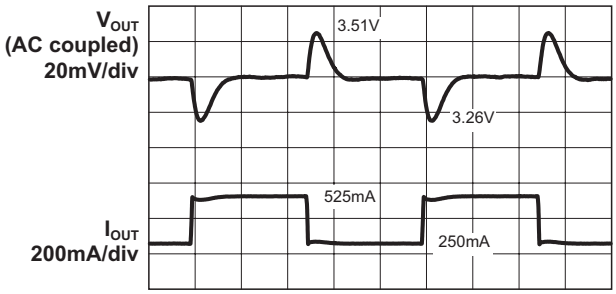
Time (25µs/div)

Enable Soft Start
(V_{IN} = 3.6V; V_{OUT} = 1.8V; R_L = 3.9Ω;
C_{OUT} = 4.7µF; L = 2.2µH)



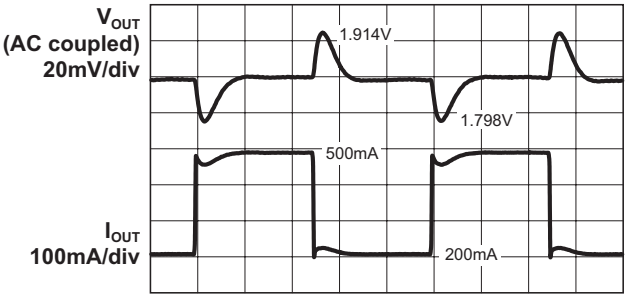
Time (20µs/div)

Load Transient Response
(V_{IN} = 4.2V; V_{OUT} = 3.3V; C_{OUT} = 4.7µF; L = 2.2µH)



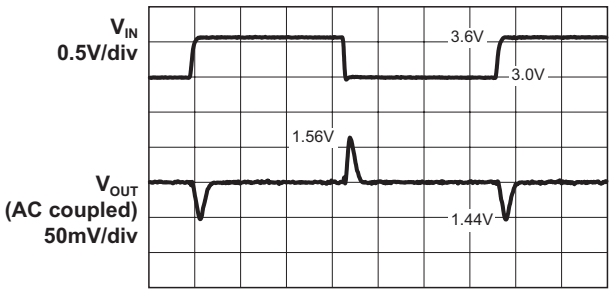
Time (20µs/div)

Load Transient Response
(V_{IN} = 3.6V; V_{OUT} = 1.8V; C_{OUT} = 4.7µF; L = 2.2µH)



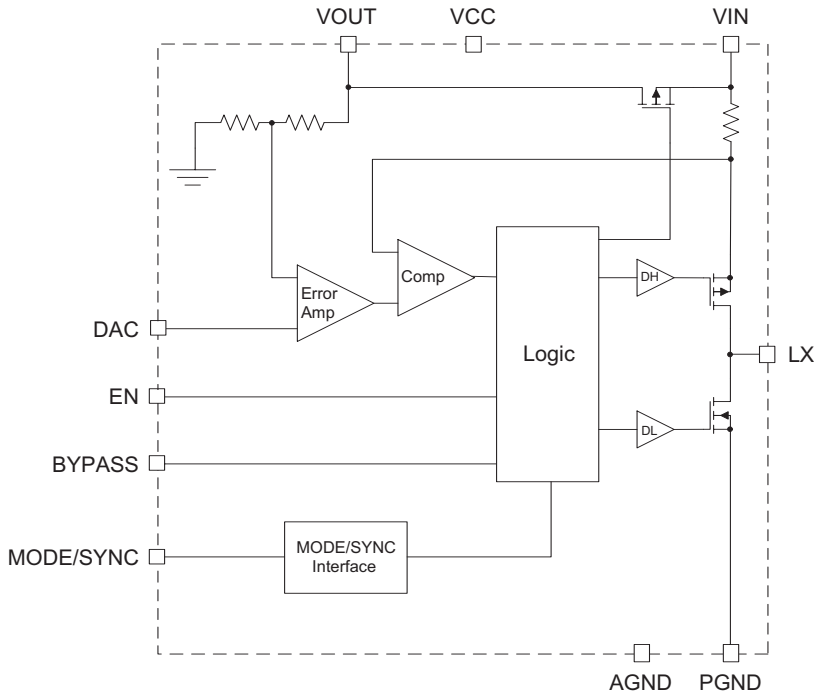
Time (20µs/div)

Line Transient Response
(V_{OUT} = 1.5V; R_L = 10Ω; C_{OUT} = 4.7µF; L = 2.2µH)



Time (50µs/div)

Functional Block Diagram



Functional Description

The AAT1171 is a 600mA 2MHz peak current mode synchronous step-down (buck) converter designed to operate from a single-cell lithium-ion battery with a 2.7V to 4.2V input range. The output voltage is dynamically programmed by the DAC input voltage.

To maximize converter efficiency over all load conditions, the converter automatically transitions to a variable frequency light load (LL) mode when the load is less than 100mA. When combined with the very low quiescent current, the LL mode maintains a high efficiency over the complete load range. For noise sensitive applications, the converter can be forced into a fixed frequency PWM mode. Provisions are also made for synchronization of the converter to an external system clock.

The synchronous buck converter power output devices are sized at 230mΩ for a 600mA full load output current. In addition to the converter output, an additional low resistance bypass MOSFET (85mΩ) can be connected between the battery input and the converter output (V_{IN} to V_{OUT}), bypassing the converter and output inductor to improve headroom and extend the WCDMA PA full power range. This reduces the battery voltage necessary for a WCDMA RF power amplifier to meet linearity requirements, thus extending operating time. In dual mode systems, the bypass mode may also be used when the WCDMA RF power amplifier is in GSM mode. Bypass mode is activated by setting the bypass input high or by forcing the baseband DAC output voltage to 1.3V.

The AAT1171 requires only three external components for operation (C_{IN}, C_{OUT}, L_X). The high 2MHz switching frequency reduces the inductor size required to 2.2µH for the AAT1171-1/AAT1171-4 and 4.7µH for the AAT1171-5. This reduces the DC resistance and improves the converter efficiency while minimizing the inductor footprint and height. The output voltage of the converter is regulated to within 0.5% and will settle in less than 30µs (according to WCDMA specifications) in response to any step change in the DAC input.

Under-voltage lockout, internal compensation, soft-start, over-current, and over-temperature protection are also included.

DAC Output Voltage Control

The output voltage is programmed by way of the DAC input voltage. The DAC to output gain for the AAT1171 is 3.

$$V_{OUT} = 3 \cdot V_{DAC}$$

The DAC input voltage range is 0.2V to 1.2V, which corresponds to an output voltage range of 0.6V to 3.6V (see Figure 1). For a 1.3V DAC level, the bypass switch is activated and the output voltage level is equivalent to the input voltage minus the bypass MOSFET ($R_{DS(ON)(bp)}$) drop.

Bypass Mode

In bypass mode, the AAT1171 bypasses the output inductor, connecting the input directly to the output through a low $R_{DS(ON)}$ 85mΩ MOSFET. Bypass mode is initiated by applying 1.3V to the DAC input or by applying a logic high to the bypass input. When not activated, a logic level low must be applied to the bypass input pin. The bypass MOSFET current is limited to 600mA.

LL/PWM Control

Two control modes are available with the AAT1171: LL mode and PWM mode. PWM mode maintains a fixed switching frequency regardless of load. The fixed switching frequency gives the advantage of lower output ripple and simplified output and input noise filtering. PWM mode also provides a faster output voltage response to changes in the DAC voltage.

In LL mode, the converter transitions to a variable switching frequency as the load decreases below 100mA. Above 100mA, where switching losses no longer dominate, the switching frequency is fixed. The LL mode's effect on the DAC to output voltage response time is most notable when transitioning from a high output voltage to a low voltage. When the converter is in PWM mode, the inductor current can be reversed and the output voltage actively discharged by the synchronous MOSFET. While in LL mode, the output voltage is discharged by the load only, resulting in a slower response to a DAC transition from a high to a low voltage.

For PWM mode, apply a logic level high to the MODE/SYNC pin; for LL mode, apply a logic level low to the MODE/SYNC pin.

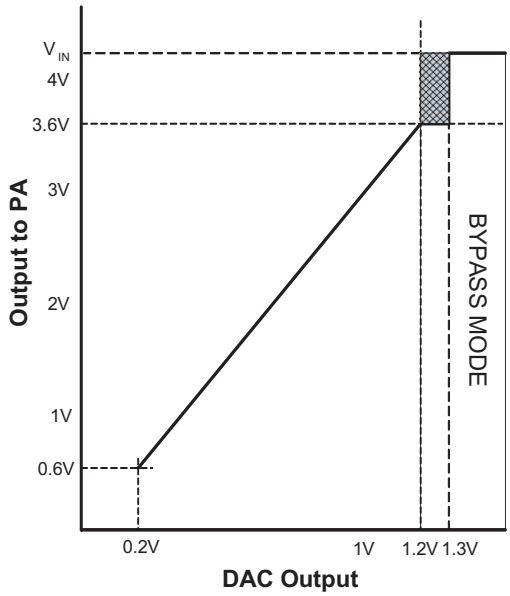


Figure 1: V_{OUT} vs. V_{DAC}.

Soft Start/Enable

The AAT1171 soft-start control prevents output voltage overshoot and limits inrush current when either the input power or the enable input is applied. When pulled low, the enable input forces the converter into a low-power, non-switching state with less than 1µA bias current.

Low Dropout Operation

For conditions where the input voltage drops to the output voltage level, the converter duty cycle increases to 100%. As 100% duty cycle is approached, the minimum off-time initially forces the high-side on-time to exceed the 2MHz clock period, reducing the converter switching frequency. Once the input drops to the level where the output can no longer be regulated, the high-side P-channel MOSFET is enabled continuously for 100% duty cycle. The output voltage then tracks the input voltage minus the IR drop of the high side P-channel MOSFET $R_{DS(ON)}$.

UVLO Shutdown

Under-voltage lockout (UVLO) circuitry monitors the input voltage and disables the converter when the input voltage drops to 2.4V, guaranteeing sufficient operating input voltage to maintain output voltage regulation and control. For a rising input voltage, the UVLO circuitry enables the converter 200mV above the shutdown level at 2.6V.

Current Limit and Short-Circuit Protection

The high-side P-channel MOSFET current limit comparator limits the peak inductor current to 1.6A. In PWM mode, the synchronous MOSFET current limit comparator limits the peak negative inductor current, and output capacitor discharge current is limited to 1A. In bypass mode, the bypass MOSFET current is limited to 600mA. In the event of an overload or short-circuit condition, the current limit protects the load and the AAT1171 power devices. Upon removal of the short-circuit or fault condition, the AAT1171 output automatically recovers to the regulated level.

Thermal Overload Protection

The maximum junction temperature is limited by the AAT1171 over-temperature shutdown protection circuitry. Both the step-down converter and the bypass MOSFET are disabled when the junction temperature reaches 140°C. Normal operation resumes once the junction temperature drops to 125°C.

External Synchronization

The AAT1171 switching frequency can be synchronized to an external square wave clock via the MODE/SYNC input. The external clock frequency range and logic levels for which the AAT1171 will remain synchronized are listed in the Electrical Characteristics table of this datasheet.

Applications Information

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. Because the required slope compensation varies with output voltage, the AAT1171 varies the slope compensation to match the output voltage. This allows the use of a single inductor value for all output voltage levels. The inductor value is 2.2µH for the AAT1171-1/AAT1171-4 and 4.7µH for the AAT1171-5.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics.

The inductor should not show any appreciable saturation under normal load conditions. The inductor ripple current varies with both the input voltage and the output voltage and peaks at the maximum input voltage with the output at one half of the input voltage. For the typical AAT1171, this corresponds to a 4.2V input voltage and a 2.1V output voltage. With the suggested 2.2µH inductor, this corresponds to 239mA peak-to-peak ripple current. For a 600mA DC load current, the peak inductor current would be 718mA. In order to prevent saturation under normal load conditions, the peak inductor current should be less than the inductor saturation current.

$$I_{PK(MAX)} = I_O + \frac{V_{IN(MAX)}}{8 \cdot L \cdot F_S}$$

$$= 0.6A + \frac{4.2V}{8 \cdot 2.2\mu H \cdot 2MHz}$$

$$= 0.6A + 0.12A$$

$$= 0.72A$$

Some inductors may meet peak and average current requirements yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor. The inductor losses can be estimated by using the full load output current. The output inductor losses can then be calculated to estimate their effect on overall device efficiency.

$$PL = I_O^2 \cdot DCR = 0.6A^2 \cdot 0.14\Omega = 50mW$$

$$\eta = \frac{P_O}{P_O + PL} = \frac{3.4 \cdot 0.6A}{3.4V \cdot 0.6A + 50mW} = 97\%$$

The 2.2µH inductor selected for the AAT1171 evaluation board has a 140mΩ DCR and a 0.91A DC current rating. At 600mA load current, the inductor loss is 50mW which gives 2.4% loss in efficiency for a 600mA 3.4V output voltage with an inductor that measures 3.2x3.2x1.2mm.

Output Capacitor Selection

The AAT1171-1/AAT1171-4 are designed for use with 4.7µF 10V X5R ceramic output capacitors, while the AAT1171-5 is designed for use with 10µF 10V X5R ceramic output capacitors. Although a larger output capacitor provides improved response to large load transients, it also limits the output voltage rise and fall time in response to the DAC input. For stable operation, with sufficient phase and gain margin, the internal voltage loop compensation limits the minimum output capacitor value to 4.7µF. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The output voltage droop due to load transients is dominated by the output capacitor. During a step increase in load current, the output capacitor supplies the load current while the control loop responds. Within two or three switching cycles, the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum output capacitor value necessary to meet a given output voltage droop requirement (V_{DROOP}) for a given load transient.

The maximum output capacitor RMS ripple current is:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Input Capacitor Selection

A 10V X5R or X7R ceramic capacitor is suggested for the input capacitor with typical values ranging from 4.7µF to 10µF. To estimate the required input capacitance size, determine the acceptable input ripple level (V_{PP}) and solve for C, as shown below. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage. Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, due to the voltage coefficient of a 10µF 6.3V X5R ceramic capacitor, with an applied voltage of 5V DC the capacitance decreases to 6µF.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4}$$

$$V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_{IN} is twice V_o; therefore, the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT1171. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in Figure 4.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients with errors in loop phase and gain measurements.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic capacitor (C3 of Figure 5) should be placed in parallel with the low ESR, ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

DAC Programming Gain

The output voltage is dynamically controlled by the DAC input voltage. The DAC to output gain is fixed at 3. The typical response time for a 0.2V to 1.2V pulsed signal on the DAC input is less than 30µs. The DAC gain can be reduced by an external resistive divider at the DAC input, as shown in the evaluation board schematic in Figures 2 and 3. For a DAC to output gain of 2 and R2 at 10kΩ, R1 is 4.99kΩ.

$$R1 = \frac{(3 - G_{DAC})R2}{G_{DAC}} = \frac{(3 - 2)10k\Omega}{2} = 4.99k\Omega$$

Thermal Calculations

There are three types of losses associated with the AAT1171 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power MOSFET devices. Switching losses are dominated by the gate charge of the power MOSFET devices. The AAT1171 main and synchronous power MOSFETs are sized to have similar $R_{DS(ON)}$ values that track with the input voltage. At full load, assuming continuous conduction mode (CCM), a simplified form of the step-down converter losses is given by:

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)} + (t_{SW} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{sw} is used to estimate the full load switching losses, which are dominated by the gate charge losses.

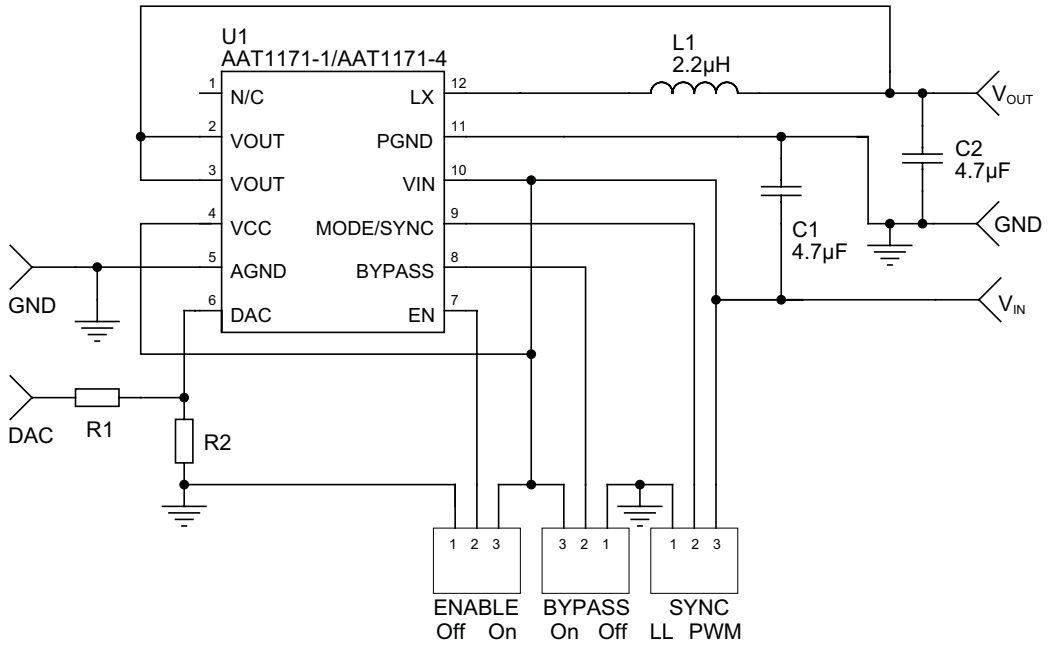


Figure 2: AAT1171-1/AAT1171-4 Evaluation Board Schematic.

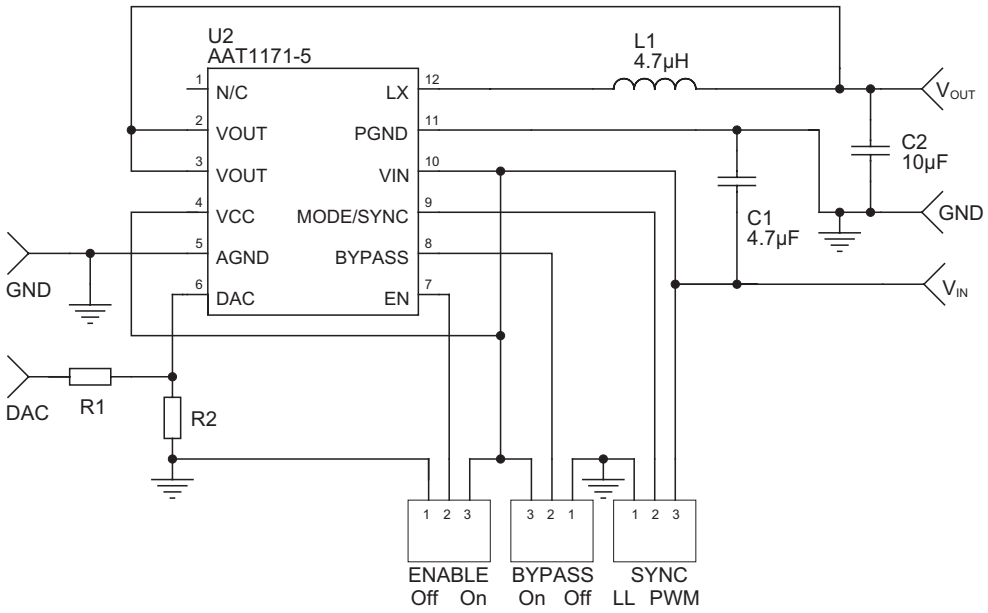


Figure 3: AAT1171-5 Evaluation Board Schematic.

For the condition where the buck converter is at 100% duty cycle dropout, the total device dissipation reduces to:

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)} + I_Q \cdot V_{IN}$$

In bypass mode, the bypass MOSFET $R_{DS(ON)(bp)}$ is used to determine the losses. The power MOSFET $R_{DS(ON)}$ increases with decreasing input voltage and the associated losses are a maximum at the minimum input voltage (2.7V).

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)(bp)} + I_Q \cdot V_{IN}$$

Since the $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

After calculating the total losses, the maximum junction temperature can be derived from the θ_{JA} for the TDFN33-12 package which is typically 50°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB}$$

Layout

The suggested PCB layout for the AAT1171 is shown in Figures 4 and 5. The following guidelines should be used to ensure a proper layout.

1. The input capacitor (C1) should connect as closely as possible to VIN (Pin 10) and PGND (Pin 11).
2. C2 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible.
3. The PCB trace connected to VOUT (Pins 2 and 3) is tied to the bypass path, as well as the feedback path for the control loop. In bypass mode, the full load current is delivered directly from the battery input; therefore, this trace should be sufficient to handle current up to the bypass current limit level.
4. The resistance of the trace from the load return to PGND (Pin 11) should be kept to a minimum. This minimizes any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. For good thermal coupling, PCB vias are required from the pad for the TDFN exposed paddle to the ground plane. The via diameter should be 0.3mm to 0.33mm and positioned on a 1.2mm grid.

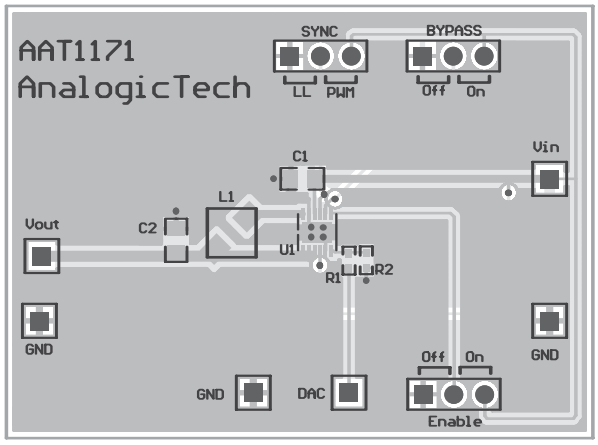


Figure 4: AAT1171 Evaluation Board Top Side Layout.

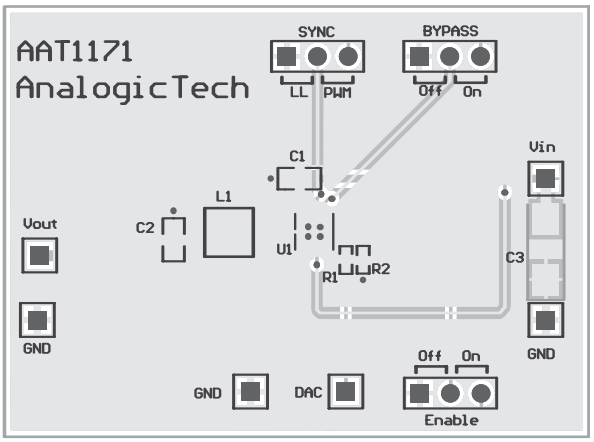


Figure 5: AAT1171 Evaluation Board Bottom Side Layout.

PA Step-Down Converter Design Example

Specifications

$V_{O(BUCK)}$ 0.6V to 3.4V with R_L =10Ω

V_{IN} 2.7V to 4.2V (3.6V nominal)

F_S 2.0MHz

T_{AMB} 85°C

Output Inductor

L1 = 2.2µH

For Copper Electronics SD3112, 2.2µH, DCR = 140mΩ.

$$\Delta I_{L1(MAX)} = \frac{V_O}{L \cdot F_S} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{2.1V}{2.2\mu H \cdot 2.0MHz} \cdot \left(1 - \frac{2.1V}{4.2V}\right) = 239mA$$

The maximum inductor ripple current occurs at 50% duty cycle at the maximum input voltage.

$$I_{PKL1} = I_O + \frac{\Delta I_{L1(MAX)}}{2} = 0.6A + 0.118A = 0.718A$$

$$P_{L1} = I_O^2 \cdot DCR = 0.6A^2 \cdot 140m\Omega = 50mW$$

Output Capacitor

Specify that V_{DROOP} = 0.2V for a 600mA load pulse.

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 0.6A}{0.2V \cdot 2.0MHz} = 4.5\mu F$$

$$I_{RMS} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{(V_O) \cdot (V_{IN(MAX)} - V_O)}{L1 \cdot F_S \cdot V_{IN(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{3.4V \cdot (4.2V - 3.4V)}{4.7\mu H \cdot 2.0MHz \cdot 4.2V} = 69mArms$$

$$P_{ESR} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (69mA)^2 = 24\mu W$$

Input Capacitor

Specify a maximum input voltage ripple of V_{PP} = 25mV.

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{25mV}{0.6A} - 5m\Omega\right) \cdot 4 \cdot 2.0MHz} = 3.4\mu F$$

$$I_{RMS} = \frac{I_O}{2} = 0.3Arms$$

$$P = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (0.3A)^2 = 0.45mW$$

AAT1171 Losses

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)} + (t_{sw} \cdot F_S \cdot I_O + I_Q) \cdot V_{IN}$$

$$= 0.6^2 \cdot 0.29\Omega + (5ns \cdot 2.0MHz \cdot 0.6A + 60\mu A) \cdot 4.2V = 104mW$$

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB} = 104mW \cdot 50°C/W = 5.2°C + 70°C = 75.2°C$$

AAT1171 Dropout Losses

$$P_{TOTAL} = I_O^2 \cdot R_{DS(ON)(HS)} + I_Q \cdot V_{IN}$$

$$= 0.6^2 \cdot 310m\Omega + 100\mu A \cdot 3.5V = 112mW$$

$$T_{J(MAX)} = P_{TOTAL} \cdot \Theta_{JA} + T_{AMB} = 112mW \cdot 50°C/W = 5.6°C + 70°C = 75.6°C$$

Manufacturer	Value	Device	Voltage	Case Size	Part Number
AVX www.avxcorp.com	10µF	Output Capacitor	10V	0805	0805ZD106KAT
Murata www.murata.com	4.7µF	Output or Input Capacitor	10V	0805	GRM21BR61A475KA73L
		Input Capacitor	6.3V	0603	GRM188R60J475KE19D
	10µF	Output Capacitor	10V	0805	GRM21BR61A106K
TDK www.tdk.com	4.7µF	Output or Input Capacitor	10V	0805	C2012X5R1A475K
		Input Capacitor	6.3V	0603	C1608X5ROJ475K
	10µF	Output Capacitor	10V	0805	C2012X5R1A106K
Taiyo Yuden www.t-yuden.com	4.7µF	Output or Input Capacitor	10V	0805	LMK212BJ475MG
		Input Capacitor	6.3V	0603	JMK107BJ475MA

Manufacturer	Value	Part Number	I_{SAT}	I_{RMS}	DCR	Case Size (mm)
Cooper Electronics	2.2µH	SD3118-2R2	1.12A	0.91A	140mΩ	3.1x3.1x1.2
www.cooperet.com	4.7µH	SD3112-4R7-R	0.8A	0.74A	246mΩ	3.1x3.1x1.2
Sumida	2.2µH	CDRH2D11/HP	1.1A	1.3A	96mΩ	3.2x3.2x1.2
www.sumida.com	4.7µH	CDRH2D11/HP	0.75A	0.85A	238mΩ	3.2x3.2x1.2
ABCO Electronics	2.2µH	LPF2010-2R2M		0.52A	200mΩ	2.0x2.0x1.0
www.abco.co.kr	2.2µH	LPF2010-2R2M		0.55A	110mΩ	2.0x2.0x1.4

Table 1: Suggested Component Selection.

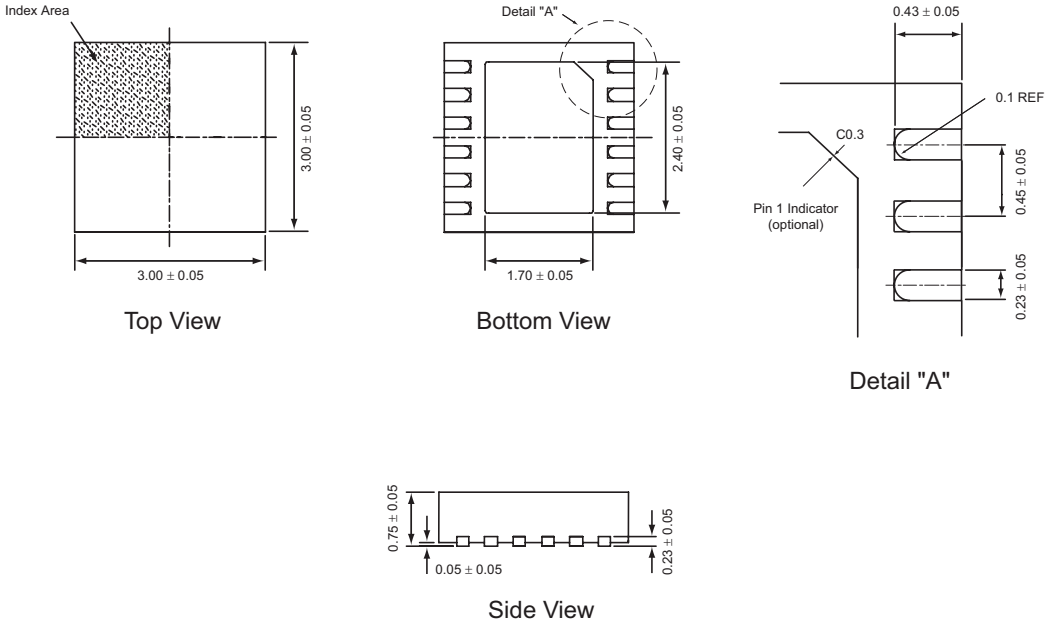
Ordering Information

Package	Marking[1]	Part Number (Tape and Reel)[2]
TDFN33-12	RXXYY	**AAT1171IWP-1-T1**
TDFN33-12	XCXYY	**AAT1171IWP-4-T1**
TDFN33-12	XDXYY	**AAT1171IWP-5-T1**

All AnalogicTech products are offered in Pb-free packaging. The term "Pb-free" means semiconductor products that are in compliance with current RoHS standards, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. For more information, please visit our website at http://www.analogictech.com/pbfree.

Package Information[3]

TDFN33-12



All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.
3. The leadless package family, which includes QFN, TQFN, DFN, TDFN and STDFN, has exposed copper (unplated) at the end of the lead terminals due to the manufacturing process. A solder fillet at the exposed copper edge cannot be guaranteed and is not required to ensure a proper bottom solder connection.

Advanced Analogic Technologies, Inc.
830 E. Arques Avenue, Sunnyvale, CA 94085
Phone (408) 737-4600
Fax (408) 737-4611