

# DABiC-5 32-Bit Serial Input Latched Sink Drivers

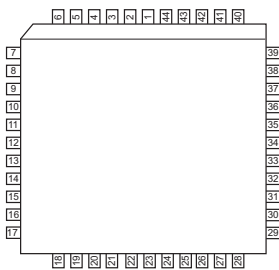
## Features and Benefits

- 3.3 to 5 V logic supply range
- To 10 MHz data input rate
- Schmitt trigger inputs for improved noise immunity
- Low-power CMOS logic and latches
- 40 V current sink outputs
- Low saturation voltage
- -40°C operation available

## Applications:

- Thermal printheads
- Multiplexed LED displays
- Incandescent lamps

## Package: 44-pin PLCC (suffix EP)



Not to scale

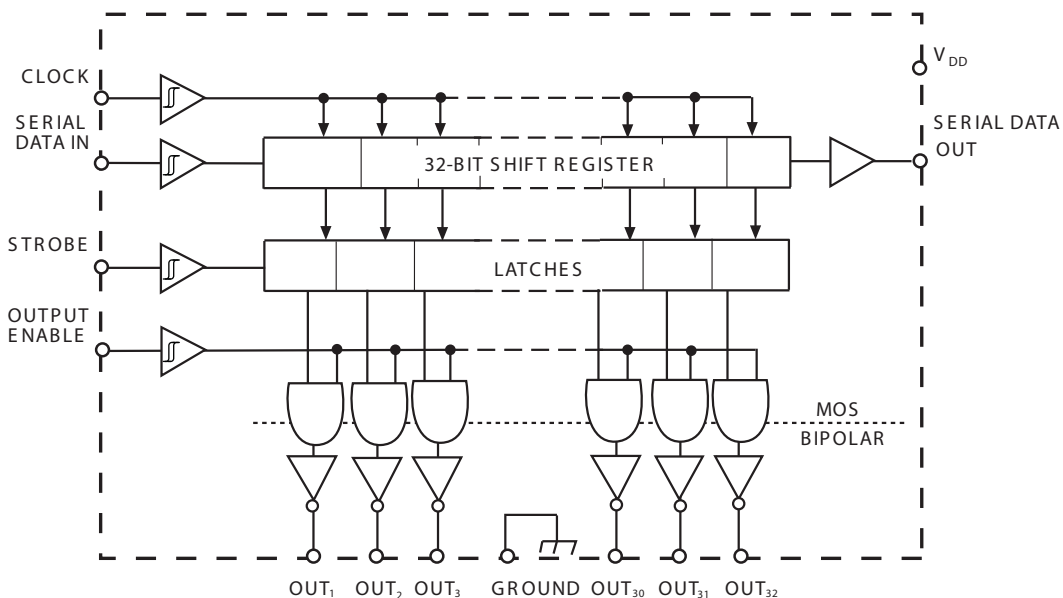
## Description

Intended originally to drive thermal printheads, the A6832 has been optimized for low output-saturation voltage, high-speed operation, and pin configurations that are the most convenient for the tight space requirements of high-resolution printheads. These integrated circuits can also be used to drive multiplexed LED displays or incandescent lamps at up to 125 mA peak current. The combination of bipolar and MOS technologies gives the A6832 arrays an interface flexibility beyond the reach of standard buffers and power driver circuits.

The devices each have 32 bipolar NPN open-collector saturated drivers, a CMOS data latch for each of the drivers, two 16-bit CMOS shift registers, and CMOS control circuitry. The high-speed CMOS shift registers and latches allow operation with most microprocessor-based systems. Use of these drivers with TTL may require input pull-up resistors to ensure an input logic high. MOS serial data outputs permit cascading for interface applications requiring additional drive lines.

The A6832 is supplied in a 44-lead plastic leaded chip carrier, for surface-mount applications requiring minimum area. These devices are lead (Pb) free, with 100% matte tin plated leadframes.

## Functional Block Diagram



## Selection Guide

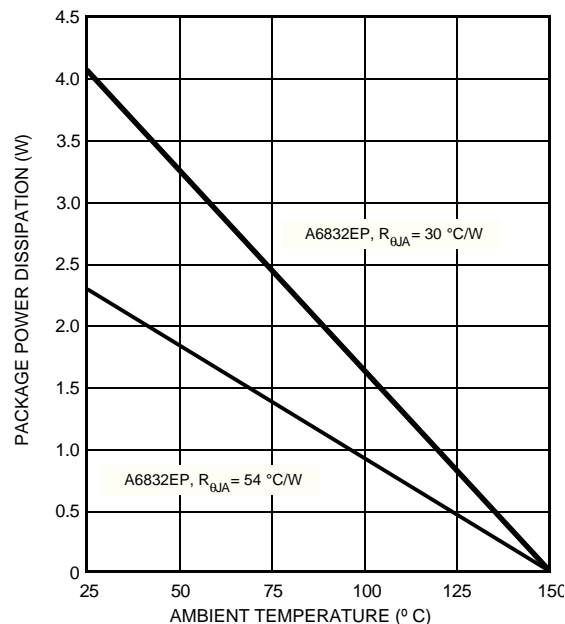
Part Number	Packing	Operating Temperature (°C)	Package
A6832EEPTR-T	450 pieces per reel	-20 to 85	44-pin PLCC
A6832SEPTR-T	450 pieces per reel	-40 to +85	



## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Logic Supply Voltage	$V_{DD}$		7	V
Input Voltage Range	$V_{IN}$	Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.	-0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{OUT}$		40	V
Continuous Output Current	$I_{OUT}$		125	mA
Package Power Dissipation	$P_D$	See Allowable Power Dissipation chart.	-	-
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C
		Range S	-20 to 85	°C
Maximum Junction Temperature	$T_{J(max)}$		150	°C
Storage Temperature	$T_{stg}$		-55 to 150	°C

## Allowable Power Dissipation, $P_D^*$



\*Additional thermal information is available on the Allegro Web site.

**ELECTRICAL CHARACTERISTICS**<sup>1</sup> Unless otherwise noted: T<sub>A</sub> = 25°C, logic supply operating voltage V<sub>dd</sub> = 3.0 V to 5.5 V

Characteristic	Symbol	Test Conditions	V <sub>dd</sub> = 3.3 V			V <sub>dd</sub> = 5 V			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I <sub>CEX</sub>	V <sub>OUT</sub> = 40 V	–	–	10	–	–	10	µA
Collector–Emitter Saturation Voltage	V <sub>CE(SAT)</sub>	I <sub>OUT</sub> = 50 mA	–	–	275	–	–	275	mV
		I <sub>OUT</sub> = 100 mA	–	–	550	–	–	550	mV
Input Voltage	V <sub>IN(1)</sub>		2.2	–	–	3.3	–	–	V
	V <sub>IN(0)</sub>		–	–	1.1	–	–	1.7	V
Input Current	I <sub>IN(1)</sub>	V <sub>IN</sub> = V <sub>DD</sub>	–	< 0.01	1.0	–	< 0.01	1.0	µA
	I <sub>IN(0)</sub>	V <sub>IN</sub> = 0 V	–	< –0.01	–1.0	–	< –0.01	–1.0	µA
Serial Data Output Voltage	V <sub>OUT(1)</sub>	I <sub>OUT</sub> = –200 µA	2.8	3.05	–	4.5	4.75	–	V
	V <sub>OUT(0)</sub>	I <sub>OUT</sub> = 200 µA	–	0.15	0.3	–	0.15	0.3	V
Maximum Clock Frequency <sup>2</sup>	f <sub>c</sub>		10	–	–	10	–	–	MHz
Logic Supply Current	I <sub>DD(1)</sub>	One output on, I <sub>OUT</sub> = 100 mA	–	–	6.0	–	–	6.0	mA
	I <sub>DD(0)</sub>	All outputs off	–	–	100	–	–	100	µA
Output Enable-to-Output Delay	t <sub>dis(BQ)</sub>	V <sub>CC</sub> = 50 V, R <sub>1</sub> = 500 Ω, C <sub>1</sub> ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	t <sub>en(BQ)</sub>	V <sub>CC</sub> = 50 V, R <sub>1</sub> = 500 Ω, C <sub>1</sub> ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Strobe-to-Output Delay	t <sub>p(STH-QL)</sub>	V <sub>CC</sub> = 50 V, R <sub>1</sub> = 500 Ω, C <sub>1</sub> ≤ 30 pF	–	–	1.0	–	–	1.0	µs
	t <sub>p(STH-QH)</sub>	V <sub>CC</sub> = 50 V, R <sub>1</sub> = 500 Ω, C <sub>1</sub> ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Fall Time	t <sub>f</sub>	V <sub>CC</sub> = 50 V, R <sub>1</sub> = 500 Ω, C <sub>1</sub> ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Output Rise Time	t <sub>r</sub>	V <sub>CC</sub> = 50 V, R <sub>1</sub> = 500 Ω, C <sub>1</sub> ≤ 30 pF	–	–	1.0	–	–	1.0	µs
Clock-to-Serial Data Out Delay	t <sub>p(CH-SQX)</sub>	I <sub>OUT</sub> = ±200 µA	–	50	–	–	50	–	ns

<sup>1</sup>Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.

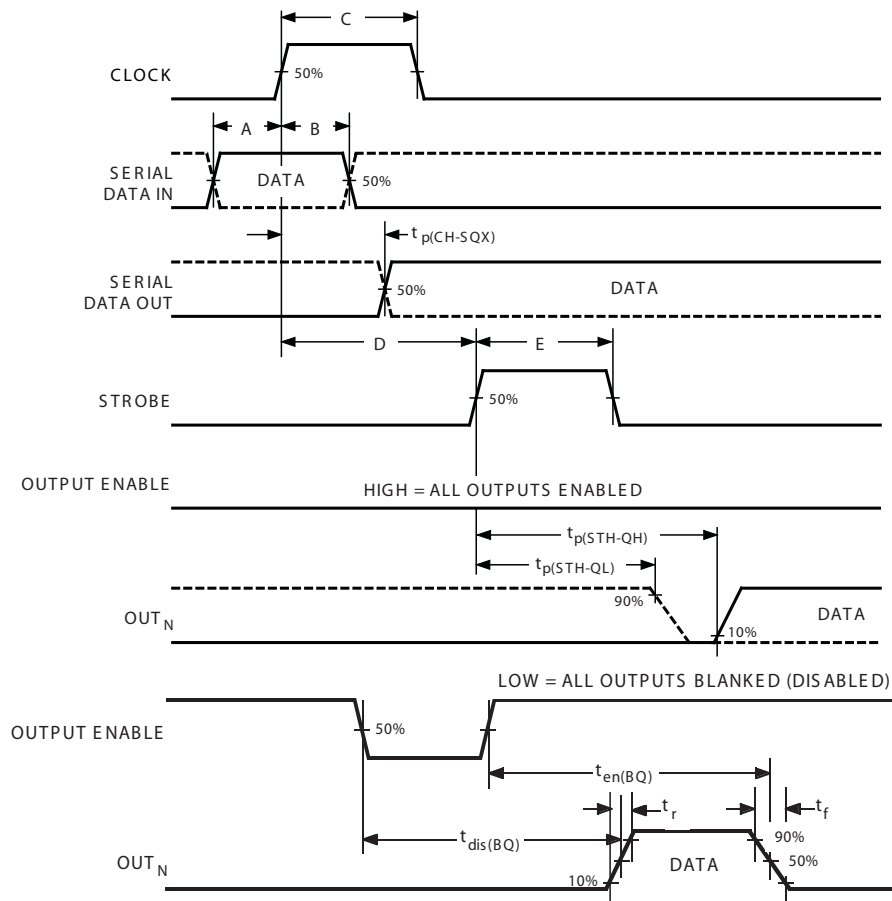
<sup>2</sup>Operation at a clock frequency greater than the specified minimum value is possible but not warranted.

Truth Table

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Strobe Input	Latch Contents						Output Enable Input	Output Contents					
		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>			I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>		I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	...	I <sub>N-1</sub>	I <sub>N</sub>
H	⌋	H	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
L	⌋	L	R <sub>1</sub>	R <sub>2</sub>	...	R <sub>N-2</sub>	R <sub>N-1</sub>	R <sub>N-1</sub>														
X	⌋	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>	R <sub>N</sub>														
		X	X	X	...	X	X	X	L	R <sub>1</sub>	R <sub>2</sub>	R <sub>3</sub>	...	R <sub>N-1</sub>	R <sub>N</sub>							
		P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	P <sub>N</sub>	H	P <sub>1</sub>	P <sub>2</sub>	P <sub>3</sub>	...	P <sub>N-1</sub>	P <sub>N</sub>	H						
					...					X	X	X	...	X	X	L	H	H	H	...	H	H

L = Low Logic Level  
H = High Logic Level  
X = Irrelevant  
P = Present State  
R = Previous State

Timing Requirements and Specifications  
(Logic Levels are  $V_{DD}$  and Ground)



Key	Description	Symbol	Time (ns)
A	Data Active Time Before Clock Pulse (Data Set-Up Time)	$t_{su(D)}$	25
B	Data Active Time After Clock Pulse (Data Hold Time)	$t_h(D)$	25
C	Clock Pulse Width	$t_w(CH)$	50
D	Time Between Clock Activation and Strobe	$t_{su(C)}$	100
E	Strobe Pulse Width	$t_w(STH)$	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

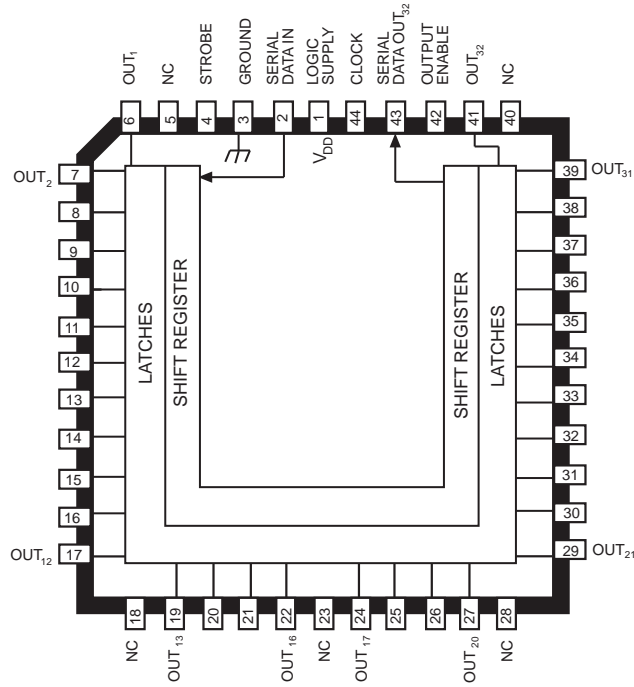
Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The

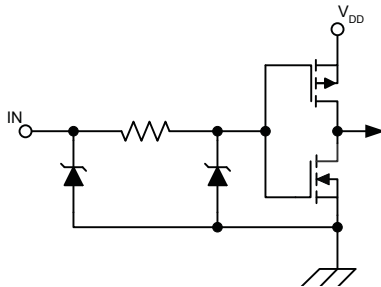
latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be low during serial data entry.

When the OUTPUT ENABLE input is low, the output sink drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input high, the outputs are controlled by the state of their respective latches.

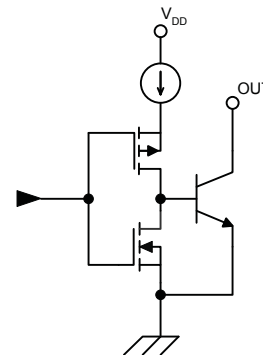
Pin-out Diagram



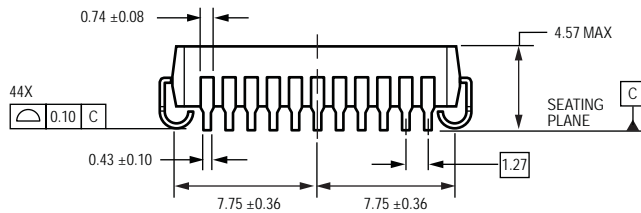
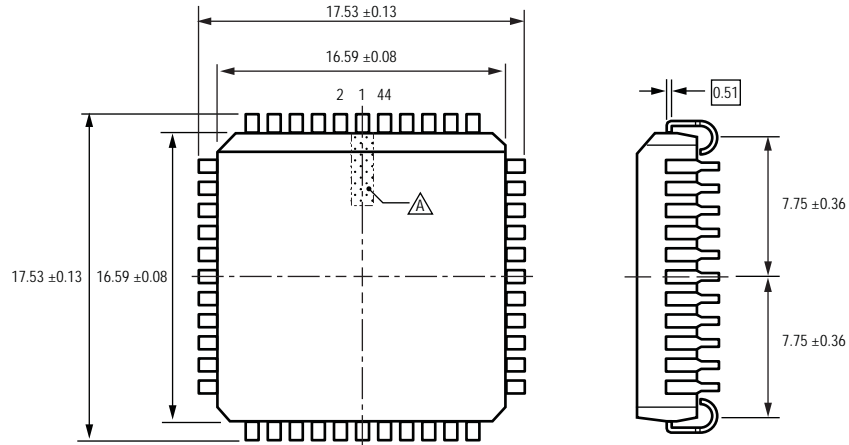
Typical Input Circuit



Typical Output Driver



Package EP, 44-pin PLCC



For Reference Only  
(reference JEDEC MS-018 AC)  
Dimensions in millimeters

Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

△ Terminal #1 mark area

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