SUMMARY
16-Bit Fixed-Point DSP Microprocessors with
On-Chip Memory
Enhanced Harvard Architecture for Three-Bus
Performance: Instruction Bus & Dual Data Buses
Independent Computation Units: ALU, Multiplier/
Accumulator, and Shifter
Single-Cycle Instruction Execution & Multifunction
Instructions
On-Chip Program Memory RAM or ROM
& Data Memory RAM
Integrated I/O Peripherals: Serial Ports, Timer,
Host Interface Port (ADSP-2111 Only)

FEATURES
25 MIPS, 40 ns Maximum Instruction Rate
Separate On-Chip Buses for Program and Data Memory
Program Memory Stores Both Instructions and Data
(Three-Bus Performance)
Dual Data Address Generators with Modulo and
Bit-Reverse Addressing
Efficient Program Sequencing with Zero-Overhead
Looping: Single-Cycle Loop Setup
Automatic Booting of On-Chip Program Memory from
Byte-Wide External Memory (e.g., EPROM)
Double-Buffered Serial Ports with Companding Hardware,
Automatic Data Buffering, and Multichannel Operation
ADSP-2111 Host Interface Port Provides Easy Interface
to 68000, 80C51, ADSP-21xx, Etc.
Automatic Booting of ADSP-2111 Program Memory
Through Host Interface Port
Three Edge- or Level-Sensitive Interrupts
Low Power IDLE Instruction
PGA, PLCC, PQFP, and TQFP Packages
MIL-STD-883B Versions Available

GENERAL DESCRIPTION
The ADSP-2100 Family processors are single-chip micro-
computers optimized for digital signal processing (DSP)
and other high speed numeric processing applications. The
ADSP-21xx processors are all built upon a common core. Each
processor combines the core DSP architecture—computation
units, data address generators, and program sequencer—with
differentiating features such as on-chip program and data
memory RAM, a programmable timer, one or two serial ports,
and, on the ADSP-2111, a host interface port.

This data sheet describes the following ADSP-2100 Family
processors:
ADSP-2101
ADSP-2103 3.3 V Version of ADSP-2101
ADSP-2105 Low Cost DSP
ADSP-2111 DSP with Host Interface Port
ADSP-2115
ADSP-2161/62/63/64 Custom ROM-programmed DSKs
The following ADSP-2100 Family processors are not included
in this data sheet:
ADSP-2100A DSP Microprocessor
ADSP-2165/66 ROM-programmed ADSP-216x processors
with powerdown and larger on-chip
memories (12K Program Memory ROM, 1K Program Memory RAM, 4K Data
Memory RAM)
ADSP-21msp5x Mix-Signal DSP Processors with
integrated on-chip A/D and D/A plus
powerdown
ADSP-2171 Speed and feature enhanced ADSP-2100
Family processor with host interface port,
powerdown, and instruction set extensions
for bit manipulation, multiplication, biased
rounding, and global interrupt masking
ADSP-2181 ADSP-21xx processor with ADSP-2171
features plus 80K bytes of on-chip RAM
configured as 16K words of program
memory and 16K words of data memory.

Refer to the individual data sheet of each of these processors for
further information.
ADSP-21xx

Fabricated in a high speed, submicron, double-layer metal CMOS process, the highest-performance ADSP-21xx processors operate at 25 MHz with a 40 ns instruction cycle time. Every instruction can execute in a single cycle. Fabrication in CMOS results in low power dissipation.

The ADSP-2100 Family’s flexible architecture and comprehensive instruction set support a high degree of parallelism. In one cycle the ADSP-21xx can perform all of the following operations:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computation

- Receive and transmit data via one or two serial ports
- Receive and/or transmit data via the host interface port (ADSP-2111 only)

The ADSP-2101, ADSP-2105, and ADSP-2115 comprise the basic set of processors of the family. Each of these three devices contains program and data memory RAM, an interval timer, and one or two serial ports. The ADSP-2103 is a 3.3 volt power supply version of the ADSP-2101; it is identical to the ADSP-2101 in all other characteristics. Table I shows the features of each ADSP-21xx processor.

The ADSP-2111 adds a 16-bit host interface port (HIP) to the basic set of ADSP-21xx integrated features. The host port provides a simple interface to host microprocessors or microcontrollers such as the 8031, 68000, or ISA bus.

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<thead>
<tr>
<th>Feature</th>
<th>2101</th>
<th>2103</th>
<th>2105</th>
<th>2115</th>
<th>2111</th>
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<tbody>
<tr>
<td>Data Memory (RAM)</td>
<td>1K</td>
<td>1K</td>
<td>½K</td>
<td>½K</td>
<td>1K</td>
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<tr>
<td>Program Memory (RAM)</td>
<td>2K</td>
<td>2K</td>
<td>1K</td>
<td>1K</td>
<td>2K</td>
</tr>
<tr>
<td>Timer</td>
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<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>Serial Port 0 (Multichannel)</td>
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<td>•</td>
<td>•</td>
<td>•</td>
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<tr>
<td>Serial Port 1</td>
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<td>•</td>
<td>•</td>
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<td>Host Interface Port</td>
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<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Speed Grades (Instruction Cycle Time)</td>
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<td>-</td>
<td>-</td>
<td>-</td>
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<td>10.24 MHz (76.9 ns)</td>
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<td>-</td>
<td>-</td>
</tr>
<tr>
<td>13.0 MHz (76.9 ns)</td>
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<td>-</td>
<td>-</td>
<td>•</td>
<td>-</td>
</tr>
<tr>
<td>13.824 MHz (72.3 ns)</td>
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<td>-</td>
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<td>-</td>
<td>-</td>
</tr>
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<td>16.67 MHz (60 ns)</td>
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<td>•</td>
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<td>-</td>
<td>•</td>
<td>•</td>
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<td>3.3 V</td>
<td>5 V</td>
<td>5 V</td>
<td>5 V</td>
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<td>Packages</td>
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<td>68-Lead PLCC</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>80-Lead PQFP</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>-</td>
<td>-</td>
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<tr>
<td>80-Lead TQFP</td>
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<td>-</td>
<td>-</td>
<td>•</td>
<td>-</td>
</tr>
<tr>
<td>100-Pin PGA</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>•</td>
</tr>
<tr>
<td>100-Lead PQFP</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>•</td>
</tr>
<tr>
<td>Temperature Grades</td>
<td>K Commercial</td>
<td>0°C to +70°C</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>B Industrial</td>
<td>-40°C to +85°C</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>T Extended</td>
<td>-55°C to +125°C</td>
<td>•</td>
<td>-</td>
<td>-</td>
<td>•</td>
</tr>
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</table>

### Table II. ADSP-216x ROM-Programmed Processor Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>2161</th>
<th>2162</th>
<th>2163</th>
<th>2164</th>
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<tr>
<td>Data Memory (RAM)</td>
<td>½K</td>
<td>½K</td>
<td>½K</td>
<td>½K</td>
</tr>
<tr>
<td>Program Memory (ROM)</td>
<td>8K</td>
<td>8K</td>
<td>4K</td>
<td>4K</td>
</tr>
<tr>
<td>Program Memory (RAM)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Timer</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>Serial Port 0 (Multichannel)</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>Serial Port 1</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>5 V</td>
<td>3.3 V</td>
<td>5 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Speed Grades (Instruction Cycle Time)</td>
<td>-</td>
<td>•</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>10.24 MHz (97.6 ns)</td>
<td>-</td>
<td>•</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>16.67 MHz (60 ns)</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>-</td>
</tr>
<tr>
<td>25 MHz (40 ns)</td>
<td>-</td>
<td>-</td>
<td>•</td>
<td>-</td>
</tr>
<tr>
<td>Packages</td>
<td>68-Lead PLCC</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>80-Lead PQFP</td>
<td>•</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>Temperature Grades</td>
<td>K Commercial</td>
<td>0°C to +70°C</td>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>B Industrial</td>
<td>-40°C to +85°C</td>
<td>•</td>
<td>•</td>
<td>•</td>
</tr>
</tbody>
</table>
The ADSP-216x series are memory-variant versions of the ADSP-2101 and ADSP-2103 that contain factory-programmed on-chip ROM program memory. These devices offer different amounts of on-chip memory for program and data storage. Table II shows the features available in the ADSP-216x series of custom ROM-coded processors.

The ADSP-216x products eliminate the need for an external boot EPROM in your system, and can also eliminate the need for any external program memory by fitting the entire application program in on-chip ROM. These devices thus provide an excellent option for volume applications where board space and system cost constraints are of critical concern.

Development Tools
The ADSP-21xx processors are supported by a complete set of tools for system development. The ADSP-2100 Family Development Software includes C and assembly language tools that allow programmers to write code for any of the ADSP-21xx processors. The ANSI C compiler generates ADSP-21xx assembly source code, while the runtime C library provides ANSI-standard and custom DSP library routines. The ADSP-21xx assembler produces object code modules which the linker combines into an executable file. The processor simulators provide an interactive instruction-level simulation with a reconfigurable, windowed user interface. A PROM splitter utility generates PROM programmer compatible files.

EZ-ICE® in-circuit emulators allow debugging of ADSP-21xx systems by providing a full range of emulation functions such as modification of memory and register values and execution breakpoints. EZ-LAB® demonstration boards are complete DSP systems that execute EPROM-based programs.

The EZ-K it Lite is a very low-cost evaluation/development platform that contains both the hardware and software needed to evaluate the ADSP-21xx architecture. Additional details and ordering information is available in the ADSP-2100 Family Software & Hardware Development Tools data sheet (ADDS-21xx-T OOL S). This data sheet can be requested from any Analog Devices sales office or distributor.

Additional Information
This data sheet provides a general overview of ADSP-21xx processor functionality. For detailed design information on the architecture and instruction set, refer to the ADSP-2100 Family User’s Manual, available from Analog Devices.

ARCHITECTURE OVERVIEW
Figure 1 shows a block diagram of the ADSP-21xx architecture. The processors contain three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be used as the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-21xx executes looped code with zero overhead—no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers to (and from) on-chip memory.

Efficient data transfer is achieved with the use of five internal buses:
- Program Memory Address (PM A) Bus
- Program Memory Data (PM D) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PM A, DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PM D, DMD) share a single external data bus. The BMS, DMS, and PMS signals indicate which memory space is using the external buses.

Program memory can store both instructions and data, permitting the ADSP-21xx to fetch two operands in a single cycle, one from program memory and one from data memory. The processor can fetch an operand from on-chip program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of the processor’s buses with the use of the bus request/grant signals (BR, BG).

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ADSP-21xx

One bus grant execution mode (GO Mode) allows the ADSP-21xx to continue running from internal memory. A second execution mode requires the processor to halt while buses are granted.

Each ADSP-21xx processor can respond to several different interrupts. There can be up to three external interrupts, configured as edge- or level-sensitive. Internal interrupts can be generated by the timer, serial ports, and, on the ADSP-2111, the host interface port. There is also a master RESET signal.

Booting circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, a 60 ns ADSP-2101 to use a 200 ns EPROM as external boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

The data receive and transmit pins on SPORT1 (Serial Port 1) can be alternatively configured as a general-purpose input flag and output flag. You can use these pins for event signalling to and from an external device. The ADSP-2111 has three additional flag outputs whose states are controlled through software.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every n cycles, where n-1 is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-21xx processors include two synchronous serial ports ("SPORTs") for serial communications and multiprocessor communication. All of the ADSP-21xx processors have two serial ports (SPORT0, SPORT1) except for the ADSP-2105, which has only SPORT1.

The serial ports provide a complete synchronous serial interface with optional companding in hardware. A wide variety of framed or frameless data transmit and receive modes of operation are available. Each SPORT can generate an internal programmable serial clock or accept an external serial clock.

Each serial port has a 5-pin interface consisting of the following signals:

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLK</td>
<td>Serial Clock (I/O)</td>
</tr>
<tr>
<td>RFS</td>
<td>Receive Frame Synchronization (I/O)</td>
</tr>
<tr>
<td>TFS</td>
<td>Transmit Frame Synchronization (I/O)</td>
</tr>
<tr>
<td>DR</td>
<td>Serial Data Receive</td>
</tr>
<tr>
<td>DT</td>
<td>Serial Data Transmit</td>
</tr>
</tbody>
</table>

The ADSP-21xx serial ports offer the following capabilities:

**Bidirectional**—Each SPORT has a separate, double-buffered transmit and receive function.

**Flexible Clocking**—Each SPORT can use an external serial clock or generate its own clock internally.

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Figure 1. ADSP-21xx Block Diagram